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Key Steps to Design a Multimode PFC Stage Using the NCP1618A

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APPLICATION NOTE

This paper describes the key steps and provides the main equations useful to rapidly design a multimode PFC stage driven by the NCP1618A. The process is illustrated by a practical 500 W, universal−mains application:

- Maximum output power: 500 W
- Input voltage range: from 90 Vrms to 265 Vrms
- Regulation output voltage: 390 V
- CCM frequency: 65 kHz
- Clamp Frequency: 130 kHz

Introduction

Forward or half−bridge converters take a significant advantage of a narrow input voltage range. In such applications, the PFC stage is wished to start first and to keep on as long as the power supply is plugged in. Optimally, the downstream converter should turn on when the output of the PFC stage is nominal. The NCP1618A is an innovative controller optimized for these applications. It features a high−voltage start−up current source to promptly pre−charge the V_{CC} capacitor and a "*pfcOK*" pin to enable the downstream converter when the PFC stage is ready for operation. In addition, its soft−skip cycle mode minimizes the PFC stage losses in very−light−load conditions.

Furthermore, the NCP1618A multimode engine leads the PFC boost pre−converter to transition from one conduction mode to another depending on the line/load conditions for an optimized efficiency over the whole operating range. Housed in a SO−9 package, the circuit further incorporates the features necessary for robust and compact PFC stages, with a minimal number of external components. NCP1618A functions make it the ideal candidate in systems where cost−effectiveness, reliability, low stand−by power, high−level efficiency over the load range and near−unity power factor are key parameters:

Multimode Capability

The NCP1618A is a multimode controller. As detailed in the next section, it selects the operating mode (continuous, critical or discontinuous conduction mode) as a function of the inductor current cycle duration for an optimized operation over the line/load range. In light load, frequency foldback is engaged to further maximize the efficiency and the circuit can be driven in soft−SKIP mode where the output voltage swings between two levels to minimize the standby losses. In addition, valley turn on of the MOSFET is provided in both the critical and discontinuous conduction modes. Note that the NCP1618A multimode algorithm closely controls the switching frequency in all circumstances (65 kHz in continuous conduction mode with jittering and between 25 kHz and 130 kHz in the other modes), hence easing EMI filtering.

High−Voltage Capability

The circuit features a high−voltage (HV) pin that monitors the input voltage. The sensed information is the input for the line−range, line−sag and brownout detection circuitries. In addition, an internal high−voltage start−up circuit draws current from the HV pin to charge up the V_{CC} capacitor when the PFC stage is plugged in. Note that the start−up current source is reduced when the V_{CC} voltage is below $V_{CC(inhibit)}$ (0.8 V typically) to prevent the circuit from overheating if the V_{CC} pin happens to accidentally be grounded. Nevertheless a 100 μF V_{CC} capacitor can be charged up to its start level within about 200 ms.

Fast Line / Load Transient Compensation

The NCP1618A incorporates a digital transconductance error amplifier and a digital compensation setting the low bandwidth necessary for proper line current shaping. However, the NCP1618A dramatically narrows the output voltage range. First, the controller detects over−voltage (OVP) situations and interrupts the power delivery as long as the output voltage exceeds this OVP threshold. Also, the ***dynamic response enhancer*** (DRE) drastically speeds−up the regulation loop when the output voltage is 4.5% below its desired level. As a matter of fact, a PFC stage provides the downstream converter with a very narrow voltage range.

A “pfcOK” Signal

The circuit detects whether the PFC stage is in steady state or on the contrary, in a start−up or fault condition. In the first case, the “*pfcOK*” pin (pin 2) sources a current proportional to the feedback pin voltage and is grounded otherwise. When in high state, the external resistor to be placed between the *pfcOK* pin and ground, forms a voltage representative of the output voltage. Thus, the *pfcOK* signal provides the downstream converter with both an enable and a feedforward signal. On the other hand, the *pfcOK* pin turns low in the event of a major fault like a brown−out situation or the bulk voltage drop to too low a level (see BUV protection) so that, finally, the downstream converter can be optimally designed for the narrow voltage provided by the PFC stage when the *pfcOK* pin is high.

Safety Protections

The NCP1618A permanently monitors the input and output voltages, the input current and the die temperature to protect the system from possible over−stresses and make the PFC stage extremely robust and reliable. In addition to the aforementioned OVP protection, one can list:

- Over−Current and Overstress Protections: the circuit permanently senses the total input current and prevents it from exceeding the programmed current limit. In addition, the circuit enters a low duty−cycle operation mode in an overstress situation, that is, when the current reaches 150% of the current limit as this can happen if the inductor saturates
- In−rush detection: when in frequency−clamped critical conduction mode, the NCP1618A prevents the power switches from turning on in the presence of the large in−rush currents which typically take place when the power supply is plugged in
- Under−Voltage Protection: this feature prevents operation in case of a failure in the feedback monitoring network (e.g., accidental grounding of the FB pin)
- Bulk Under−Voltage Detection (BUV): The BUV function is implemented to prevent the downstream converter from operating when the buck voltage is too low. Practically, a BUV situation is detected when the feedback pin voltage drops below 1.8 V typically
- Line−Sag and Brown−Out Detection: the circuit prevents CCM operation and gradually reduces power delivery if too low a line magnitude is detected (line sag) to protect the PFC stage from the excessive stress possibly occurring in such conditions. If the mains interruption is long enough (650 ms typically), a brown−out fault is detected and pfcOK is grounded to disable the downstream converter
- Thermal Shutdown: the circuit stops pulsing when its junction temperature exceeds 145 °C typically and resumes operation once it drops below about 110°C (35°C hysteresis)

MULTIMODE CAPABILITY

The NCP1618A naturally transitions from one conduction mode to another depending on the conditions so that the operation is optimized over the line/load range:

- The circuit operates in critical conduction mode (CrM) by default. CrM is an efficient and popular mode of operation where the inductor current ramps up to twice the line instantaneous current, ramps down to zero then immediately ramps positive again. The input current ripple is large (2 times the line instantaneous current) but the MOSFET turn−on losses are minimized. This is because, the current being at a null when the MOSFET closes, there are no reverse−recovery losses of the boost diode to worry about but also, because valley turn−on of the MOSFET can be obtained. Zero voltage switching is even possible when the input voltage is less than 50% of the output voltage
- The CrM switching frequency is by essence variable and tends to increase near the line zero crossing and more generally at light load. The NCP1618A prevents the switching frequency from exceeding a maximum level (130 kHz typically) by generating a dead−time. This is the so−called frequency−clamped critical conduction mode (FCCrM). When the frequency is clamped, the PFC stage operates in discontinuous conduction mode (DCM) while keeping properly shaping the line current by appropriately compensating for dead−times. The system automatically transitions between DCM and CrM with no discontinuity in operation and with no power factor degradation
- In addition, when the load further decreases, the frequency clamp level decays, thus, lowering the DCM frequency (frequency foldback). This method is an effective solution to maintain the low−power range efficiency at a high level while otherwise it would sag because of the switching losses dramatic impact. However, the minimum frequency is firmly maintained above 25 kHz to stay outside the audible range
- In heavy−load and low−line conditions, the input current becomes high and the inductor current ripple, ΔI_L, can take too large a value, leading to an increased inductor size, excessive conduction losses and significant EMI filtering pains, if the PFC remains operated in CrM. In this case, the NCP1618A can enter the continuous conduction mode (CCM), which is more suitable in heavy load conditions
- In very light−load conditions, the circuit can be operated in a soft−SKIP mode where the output voltage swings between 103% and 98% of its nominal level. During the idle phase for which the bulk capacitor discharges, the NCP1618A consumption is minimized (250 μA). This mode is externally set using the pfcOK or V_M pins

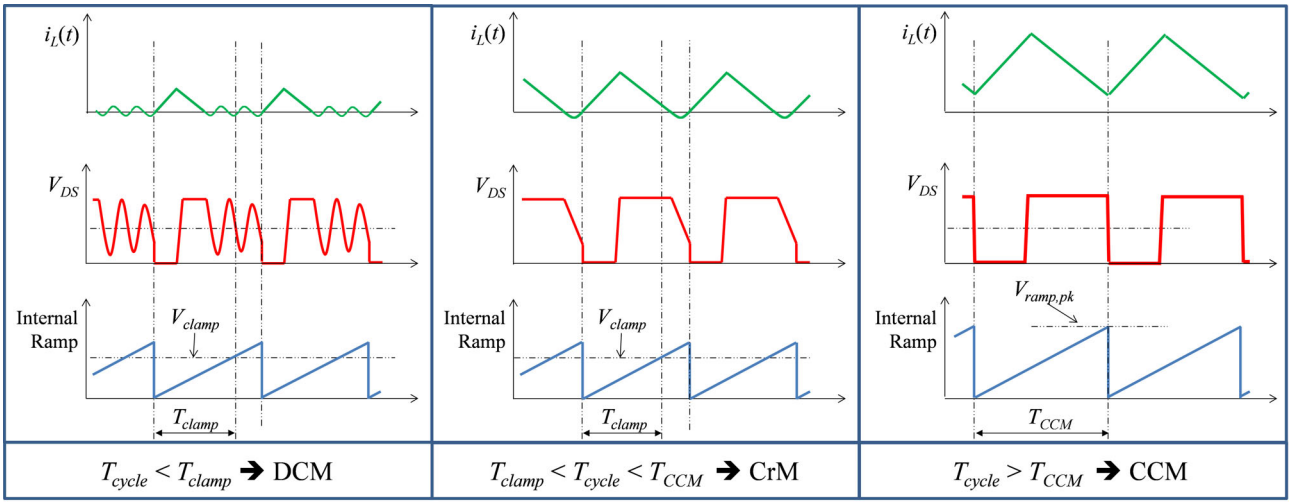


Figure 1. The Mode is Selected Based on the Current Cycle Duration (T_{clamp} is the DCM Period Clamp, T_{CCM} is the CCM Switching Period)

Figure 1 provides a simplified description of how the conduction mode is selected. This is based on the duration of the inductor current cycle.

- The circuit tends to operate in critical conduction mode as long as the current switching cycle is short enough not to enter the CCM mode. However, if the current cycle happens to be shorter than the frequency−clamp period (T_{clamp} which is about 7.7 μs typically leading to a 130 kHz DCM frequency), the circuit delays the next cycle until the T_{clamp} time has elapsed. Thus, the circuit enters DCM operation. The switching cycle is actually a bit longer than T_{clamp} since the next cycle is further delayed until the next valley is detected (left of Figure 1). Doing so, valley turn−on is obtained for minimized turn−on losses
- This is the frequency−Clamped Critical conduction Mode (FCCrM) where transitions between CrM and DCM are managed cycle−by−cycle so that the circuit can transition from DCM to CrM and vice versa within a half−line cycle. Practically, DCM is more likely to occur near the line zero crossing and CrM at the top of the sinusoid. As the load further decays, current cycles become too short to cause CrM cycles and DCM operation is obtained over the entire line sinusoid. At very light load, the DCM period clamp is increased (a longer minimum switching period is forced causing frequency foldback)
- In heavy−load conditions, the circuit enters CCM when the current cycle is longer than 112% of the CCM period (about 17 μs). The circuit cannot leave CCM on a cycle−by−cycle basis. It permanently operates in CCM until no current cycle longer than the CCM period is detected for a blanking time of several line cycles. In other words, the circuit remains in CCM over the entire half−line cycle until the load is decreased enough to recover the FCCrM mode

The inductor value sets the power above which the circuit will enter CCM. Equation 1 gives the CrM switching frequency at the top of the line sinusoid:

$$f_{SW}\Big|_{v_{in}(t)=\sqrt{2}\cdot V_{in,rms}} = \frac{V_{in,rms}^{\ 2}\cdot\left(V_{out}-\sqrt{2}\cdot V_{in,rms}\right)}{2\cdot L\cdot P_{in,avg}\cdot V_{out}} \quad \text{(eq. 1)}$$

We can then compute L leading the switching frequency (at the top of the line sinusoid) to become as low as the CCM one (f_{CCM}) when the power exceeds the wished level for CCM entering ($P_{in,transition}$). Practically, about 89% of f_{CCM} is actually to be targeted since the NCP1618A implements the hysteresis necessary to avoid repeated and unwanted transitions between modes:

$$L = \frac{V_{in,rms}^{\ 2}\cdot\left(V_{out}-\sqrt{2}\cdot V_{in,rms}\right)}{2\cdot 89\%\cdot f_{CCM}\cdot P_{in,transition}\cdot V_{out}} \quad \text{(eq. 2)}$$

As an example, if we target $P_{in,transition}$ = 275 W at low line (90 V), f_{CCM} being 65 kHz, a 175 μH inductor is to be chosen.

It comes from this that at low line (90 Vrms) and with a 175 μH inductor, the system will operate in FCCrM for powers below 275 W and in CCM for powers above 275 W. Also, whatever the full load is, the maximum input current ripple to be filtered by the EMI filter is the current ripple obtained at this FCCrM−to−CCM power threshold. In other words, the inductor value can be selected so that the circuit enters CCM when the FCCrM current ripple gets too high for optimal operation.

Selecting the Power Threshold for FCCrM to CCM Transition

The power for transition must be considered at the lowest−line level of the application. This threshold $(P_{in,transition})_{LL}$ is generally set in the range 300 W, that is, to a power level above which CCM is considered as the most appropriate conduction mode. However, the ratio $(P_{in,transition})_{LL}$ over $(P_{in,avg})_{max}$ must not be too low. First, a very deep CCM operation would lead to too large an inductor. Second, if too low, the control signal range may not be sufficient to provide the full power. Practically, $(P_{in,transition})_{LL}$ over $(P_{in,avg})_{max}$ must be set to 20% or above in a wide−mains application. More flexibility is possible in a reduced line range. In any cases, the computation of the V_M pin resistor which sets the CCM gain enables to check that the selection is correct. We will see that Eq. 27 gives the maximum V_M pin resistance enabling to provide the full power ($R_{M,max}$). Eq. 29 provides the V_M pin resistance for constant−power transition ($R_{M,CP}$). ($R_{M,CP}$) must be lower than ($R_{M,max}$) for full power delivery. Even, for the sake of margin, ($R_{M,CP}$) should be set lower than (80%*$R_{M,max}$). Thus, if ($R_{M,CP}$) is higher than (80%*$R_{M,max}$), it is recommended to increase $(P_{in,transition})_{LL}$.

DESIGN STEPS

Key Specifications

We must first identify the main specification points of the PFC stage:

- f_{line} : Line frequency. 50 Hz /60 Hz applications are targeted. Practically, they are often specified in a range of 47−63 Hz and for calculations such as hold−up time, one has to factor in the lowest specified value.
- $(V_{in,rms})_{LL}$: Lowest level of the line voltage. This is the minimum line rms voltage for which the PFC stage must operate nominally. Such a level is usually 10−12% below the minimum typical voltage which could be 100 V in many countries. We will take: $(V_{in,rms})_{LL} = 90\,V$. The circuit is however able to operate down to the thresholds of the NCP1618A brown−out and line sag protections:
  - $(V_{in,rms})_{boH} = V_{BO(start)} / \sqrt{2} \cong 78\,V$
  - $(V_{in,rms})_{boL} = V_{BO(stop)} / \sqrt{2} = 71\,V$
  - Where $V_{BO(start)}$ is the line−sag and BO upper threshold (111 V typically − see data sheet) and $V_{BO(stop)}$ is the line sag and BO lower threshold (100 V typically − see data sheet)
- $(V_{in,rms})_{HL}$: Highest rms level for the line voltage. It is usually 10% above the maximum typical voltage (240 V in many countries). We will use: $(V_{in,rms})_{HL} = 264\,V$.
- $V_{out,nom}$: Nominal output voltage. This is the regulation level for the PFC output voltage (also designated as bulk voltage). $V_{out,nom}$ must be higher than $(\sqrt{2} \cdot (V_{line,rms})_{HL})$. 390 V is our target value.
- $(\Delta V_{out})_{pk-pk}$: Peak−to−peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the over−voltage protection (softOVP) and/or the dynamic response enhancer (DRE) in normal operation.
- $t_{HOLD-UP}$: Hold−up time. This parameter specifies the amount of time the output will remain valid during a line dropout event. One line cycle is typically specified. This requirement requires knowing the minimum voltage on the PFC stage output necessary for the proper operation in your application $(V_{out,min})$. No hold−up time will be considered here.
- P_{out}: Output power. This is the power consumed by the PFC load.
- $P_{out,\,max}$: Maximum output power. This is the maximum output power level, that is, 500 W in our application.
- $(P_{in,\,avg})_{max}$: Maximum input power. This is the maximum power which can be absorbed from the mains in normal operation. This level is typically obtained at full load, lowest line. As a starting point, we will assume an efficiency of 92.5% which leads to: $(P_{in,avg})_{max} = \frac{500}{92.5\%} \cong 540$ W
- $(P_{in,\,transition})_{LL}$: Input power above which the circuit enters the CCM mode. This power threshold is considered at the lowest line of the application. We will set it to 300 W. Note that typically, it should be set to 20% of $(P_{in,avg})_{max}$ or above. See the “CCM Duty Ratio control” section for more details.

We can now compute the value of the components shown in the generic application schematic of Figure 2.

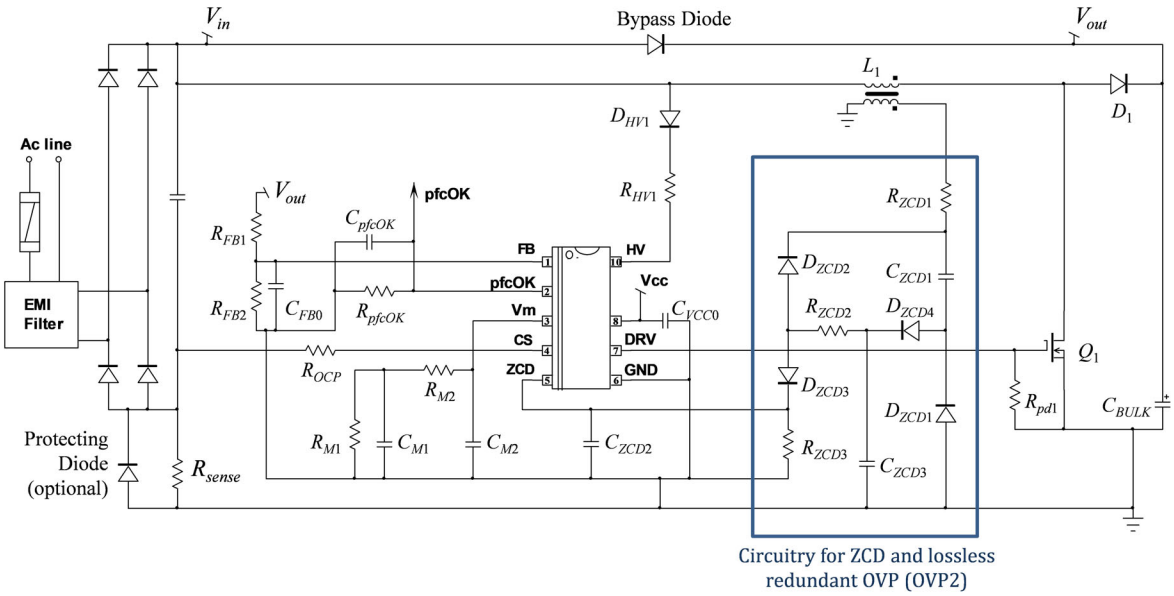


Figure 2. NCP1618A Generic Application Schematic

Inductor Selection

The inductance is the parameter which sets the power level above which the PFC stage enters the CCM mode of operation. Practically, The PFC stage will enter CCM when the CrM frequency will drop to (65 kHz / 112%), that is, 58 kHz.

The CrM witching frequency (at the top of the sinusoid) can be approximated as follows [1]:

$$f_{SW} = \frac{V_{in,rms}^{\ 2} \cdot \left(V_{out} - \sqrt{2} \cdot V_{in,rms}\right)}{2 \cdot L \cdot P_{in,avg} \cdot V_{out}} \quad \text{(eq. 3)}$$

We will target CCM for powers higher than 275 W at the lowest line (90 V rms). In other words, the CrM frequency @ 90 V rms, 275 W must be 58 kHz. This criterion leads to the following L expression:

$$L = \frac{\left(V_{in,rms}\right)_{LL}^{\ 2} \cdot \left(V_{out} - \sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}\right)}{2 \cdot \left(f_{SW}\right)_{th} \cdot \left(P_{in,transition}\right)_{LL} \cdot V_{out}} \quad \text{(eq. 4)}$$

Where $(f_{SW})_{th}$ is the 58 kHz frequency threshold, $(Vin,rms)_{LL}$ is the lowest−line rms voltage and $(P_{in,transition})_{LL}$ is the input average power above which the circuit must enter the CCM mode at $(Vin,rms = (Vin,rms)_{LL})$.

It comes:

$$L = \frac{90^2 \cdot \left(390 - \sqrt{2} \cdot 90\right)}{2 \cdot 58 \cdot 10^3 \cdot 300 \cdot 390} \cong 175\ \mu H \quad \text{(eq. 5)}$$

One can show that in CCM, the current peak−to−peak ripple at the top of the sinusoid, is given by:

$$\left(\Delta I_L\right)_{pp} = \frac{V_{out} - \sqrt{2} \cdot V_{in,rms}}{L \cdot f_{CCM}} \cdot \frac{\sqrt{2} \cdot V_{in,rms}}{V_{out}} \quad \text{(eq. 6)}$$

The inductor peak current will hence be:

$$I_{L,pk} = \frac{\sqrt{2} \cdot P_{in,avg}}{V_{in,rms}} + \frac{\left(\Delta I_L\right)_{pp}}{2} \quad \text{(eq. 7)}$$

Combining equations 7 and 6 leads to:

$$I_{L,pk} = \frac{\sqrt{2}\cdot P_{in,avg}}{V_{in,rms}} + \left(\frac{V_{out} - \sqrt{2}\cdot V_{in,rms}}{2\cdot L\cdot f_{CCM}} \cdot \frac{\sqrt{2}\cdot V_{in,rms}}{V_{out}} \right) \quad \text{(eq. 8)}$$

Computing at the lowest line level (90 V rms), the maximum inductor current is obtained:

$$\left(I_{L,pk}\right)_{\max} = \frac{\sqrt{2}\cdot\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}} + \left(\frac{V_{out} - \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}{2\cdot L\cdot f_{CCM}} \cdot \frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}{V_{out}} \right) \quad \text{(eq. 9)}$$

In our application, the maximum peak value and the lowest−line peak−to−peak ripple ($(\Delta I_L)_{pp-LL}$) of the inductor current will hence be:

$$\left(\Delta I_L\right)_{pp-LL} = \frac{390 - \sqrt{2}\cdot 90}{175\cdot 10^{-6}\cdot 65\cdot 10^{3}} \cdot \frac{\sqrt{2}\cdot 90}{390} \cong 7.5\ \text{A} \quad \text{(eq. 10)}$$

$$\left(I_{L,pk}\right)_{\max} = \frac{\sqrt{2}\cdot 540}{90} + \left(\frac{390 - \sqrt{2}\cdot 90}{2\cdot 175\cdot 10^{-6}\cdot 65\cdot 10^{3}} \cdot \frac{\sqrt{2}\cdot 90}{390} \right) \cong 12.2\ \text{A} \quad \text{(eq. 11)}$$

Finally, the following expression gives an estimate of the inductor rms current:

$$\left(I_{L,rms}\right)_{\max} = \sqrt{\left(\frac{\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}} \right)^2 + \left(\frac{\left(V_{in,rms}\right)_{LL}^2}{12\cdot\left(L\cdot f_{CCM}\right)^2} \cdot \left(1 - \frac{16\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}{3\pi\cdot V_{out}} + \frac{3\cdot\left(V_{in,rms}\right)_{LL}^2}{2\cdot {V_{out}}^2} \right) \right)} \cong 6.2\ \text{A} \quad \text{(eq. 12)}$$

PQ3230 inductor ref. 750317557 from Wurth Elektronik is selected. It exhibits an auxiliary winding ($n_{aux}/n_P = 10\%$) which is used to feed the NCP1618A V_{CC} voltage and to provide the zero current detection signal necessary for valley turn on in both critical and discontinuous conduction modes.

Note that if the PFC stage is designed so that the circuit permanently remains in frequency−clamped critical conduction mode (no CCM operation over the load/line range), the following equations would provide the electrical specification of the inductor:

$$I_{L,\max} = \frac{2\sqrt{2}\cdot\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}} \quad \text{(eq. 13)}$$

$$\left(\Delta I_L\right)_{pp-90V} = \frac{2\sqrt{2}\cdot\left(P_{in,avg}\right)_{\max}}{\left(V_{in,rms}\right)_{LL}} \quad \text{(eq. 14)}$$

$$\left(I_{L,rms}\right)_{\max} = \frac{I_{L,\max}}{\sqrt{6}} \quad \text{(eq. 15)}$$

This would happen for L lower than the value by returned by Eq.4 if the transition power ($P_{in,transition}$) was set above the maximum input power, that is, in our application, for $L < 90$ μH.

Current Sensing and CCM Control

The NCP1618A is designed to monitor a negative voltage proportional to the inductor current (I_L). As portrayed by Figure 3, a current sense resistor (R_{sense}) is inserted in the return path to generate a negative voltage (V_{Rsense}) proportional to I_L. The circuit uses V_{Rsense} to detect when I_L exceeds its maximum permissible level. Practically, the circuit incorporates an operational amplifier that sources the current necessary to maintain the CS pin voltage at a null. By inserting a resistor R_{OCP} between the *CS* pin and R_{sense}, we adjust the current that is sourced by the CS pin (I_{CS}) as follows:

$$-\left(R_{sense}\cdot I_L\right)+\left(R_{OCP}\cdot I_{CS}\right)=0 \quad \text{(eq. 16)}$$

Which leads to:

$$I_{CS}=\frac{R_{sense}}{R_{OCP}}I_L \quad \text{(eq. 17)}$$

In other words, the CS pin current (I_{CS}) is proportional to the inductor current. The following three protecting functions compare I_{CS} to internal current references for:

- Over current protection: if I_{CS} gets higher than internal threshold $I_{ILIMIT1}$ (200 μA typically), the MOSFET immediately turns off. This is the traditional cycle−by−cycle current limitation.
- Overstress protection: if I_{CS} exceeds a second internal threshold $I_{ILIMIT2}$ which is 50% higher than $I_{ILIMIT1}$, the circuit detects an abnormal condition. In this case, the circuit disables the CCM mode (if set) and stops operation for 800 μs. This protection can trip if the inductor happens to saturate or if its auxiliary winding is accidently shorted. It may also help protect the circuit if the MOSFET turns on during an in−rush sequence.
- In−rush current detection. When in frequency−clamped critical conduction mode, the circuit cannot restart a new cycle until I_{CS} has dropped below I_{inrush} (10 μA typically that is 5% of the maximum current threshold $I_{ILIMIT1}$). The inrush current detector stabilizes operation by providing a rough second ZCD signal, when (during the start−up phase and at very high line for instance), the auxiliary winding voltage is too low to provide an accurate ZCD signal. It also protects the circuit by preventing operation during the inrush phase (1).

Internal current I_{CS} is also used in CCM to control the power−switch duty−ratio.

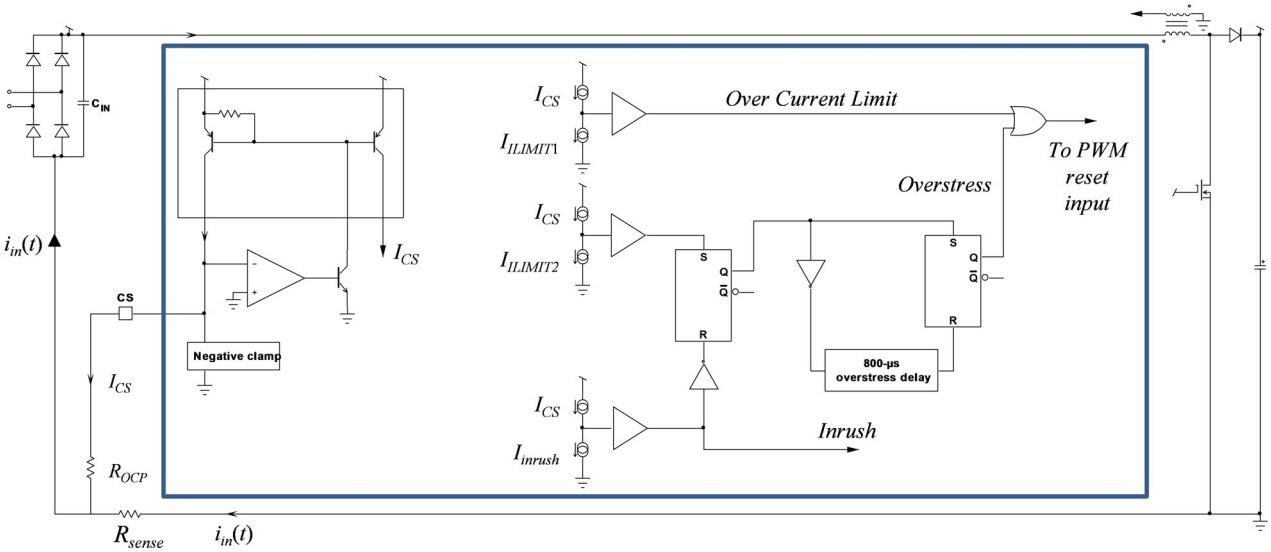


Figure 3. Current Sense Block

As we have two external components to set the current limit (R_{OCP} and R_{sense}), the current sense resistor can be optimized to have the *best trade−off between losses and noise immunity.*

The following equations give an estimate of the R_{sense} maximum losses:

$$P_{R_{sense}}=R_{sense}\cdot\left(I_{L,rms}\right)^2_{\max} \quad \text{(eq. 18)}$$

1. If an inrush sequence happens when the circuit operates, the overstress protection will trip (provided that the inrush current exceeds the overstress level) and stop operation for 800 μs. At the end of this delay, the inrush protection prevents operation until the inrush event is finished.

One can choose R_{sense} as a function of its relative impact on the PFC stage efficiency at low line and full power. If α is the relative percentage of the power that can be consumed by R_{sense}, this criterion leads to:

$$P_{R_{sense}} \leq \alpha \cdot P_{in,\max} \quad \text{(eq. 19)}$$

Finally:

$$R_{sense} \leq \frac{\alpha \cdot P_{in,\max}}{\left(I_{L,rms}\right)^2_{\max}} \quad \text{(eq. 20)}$$

In our application, we choose (α = 0.25 %),

$$R_{sense} \leq \frac{0.25\% \cdot 540}{6.2^2} \cong 35\ \text{m}\Omega \quad \text{(eq. 21)}$$

In practice, we will use R_{sense} = 30 mΩ and hence, since the maximum inductor current is 12.2 A (see inductor computation):

$$R_{OCP} = \frac{R_{sense} \cdot I_{L,\max}}{\left(I_{ILIMIT1(LL)}\right)_{\min}} = \frac{30 \cdot 10^{-3} \cdot 12.2}{190 \cdot 10^{-6}} \cong 1.9\ k\Omega \quad \text{(eq. 22)}$$

Since the CS pin is designed to source a current, it is not recommended to add a capacitor directly on the pin for filtering. Instead, the network of Figure 4 is actually used where the resistor R_{OCP} is split into 2 resistors R_{OCP1} and R_{OCP2} and a capacitor C_{CS} is placed between the R_{OCP1} and R_{OCP2} common node and ground. To offer some margin both R_{OCP1} and R_{OCP2} are set to 1 kΩ ($R_{OCP} = R_{OCP1} + R_{OCP1}$ = 2 kΩ) and a 220 pF capacitor is implemented for C_{CS}.

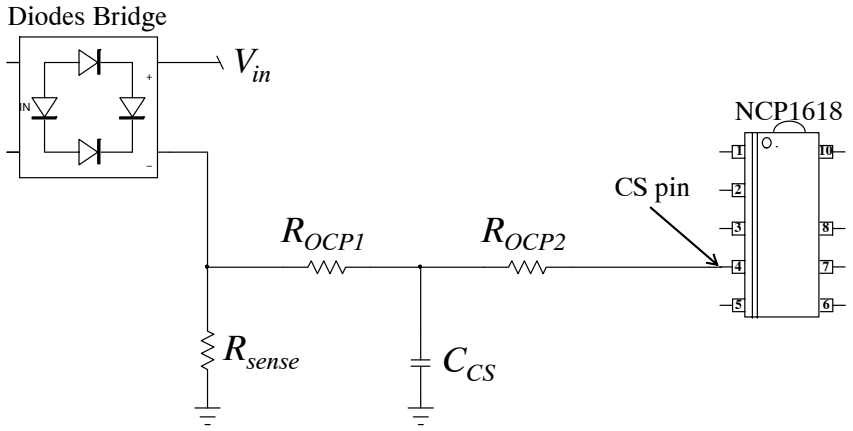


Figure 4. Filtering the CS Pin

Important notes:

- The current sense resistor sees the startup inrush current and must be able to sustain it in the worse conditions of the application. As shown by Figure 1, a diode may have to be placed across R_{sense} to divert a large part of the huge in−rush current which can take place during start−up or faulty phases. This diode is actually optional but should be added if the in−rush stress can damage R_{sense} or if the R_{sense} voltage may become large enough to cause I_{CS} to exceed the 2 mA maximum rating. The forward voltage of this diode must be high enough not to clamp the R_{sense} voltage to too low a value which may prevent the NCP1618A from detecting overcurrent or overstress situations. Practically, it should be higher than R_{OCP} times the overstress threshold ($I_{ILIMIT2}$ which is 330 μA maximum). In our application, R_{OCP} being 2 kΩ, the diode forward voltage must be higher than 660 mV.
- If a filtering capacitor (C_{CS} of Figure 4) is implemented, its negative terminal should be connected to the circuit ground rather than to the power ground
- The NCP1618A senses the CS pin impedance before starting operation (or before restarting operation after an interruption) and prevents MOSFET switching until it is high enough. The NCP1618A redoes it at the end of any switching cycle during which the CS pin current (I_{CS}) does not exceed the inrush level (5% of the overcurrent threshold) while the line instantaneous voltage is higher than its brown−out threshold. This impedance test is performed to detect and protect the PFC stage if the CS pin is accidentally grounded. *Not to improperly detect a CS fault, R_{OCP} or (R_{OCP1} + R_{OCP2}) should be higher than 1.5 kΩ*

- CCM Duty Ratio control

For CCM control, the NCP1618A re−uses the proven “predictive method” scheme implemented in the NCP1653 and NCP1654 CCM PFC controllers. In other words, it directly computes the power switch on−time as a function of the inductor current. Practically, as shown by Figure 5, the I_{CS} current is modulated by the control signal and sourced by the V_M pin to build the CCM current information. The V_M pin signal is:

$$V_M = 0.4 \cdot R_M \cdot \frac{V_{RAMP,pk}}{V_{REGUL}} \cdot I_{CS} \quad \text{(eq. 23)}$$

Where $V_{RAMP,pk}$ and R_M respectively are the peak value of the CCM PWM ramp and the V_M pin resistor value. The CCM regulation voltage (V_{REGUL}) is proportional to the regulation control signal provided by the internal regulation block ($V_{CONTROL}$) as follows for line feedforward:

- ($V_{CONTROL}$) in low−line conditions (2)
- ($V_{CONTROL}$ / 4) in high−line conditions (2)

As detailed in the data sheet [2], this leads to the following input power expressions:

- Low−line conditions:

$$P_{in,avg} = \frac{2.5 \cdot R_{OCP} \cdot V_{in,rms}^{\ 2}}{R_M \cdot R_{sense}} \cdot \frac{V_{CONTROL}}{V_{out}} \quad \text{(eq. 24)}$$

- High−line conditions:

$$P_{in,avg} = \frac{0.625 \cdot R_{OCP} \cdot V_{in,rms}^{\ 2}}{R_M \cdot R_{sense}} \cdot \frac{V_{CONTROL}}{V_{out}} \quad \text{(eq. 25)}$$

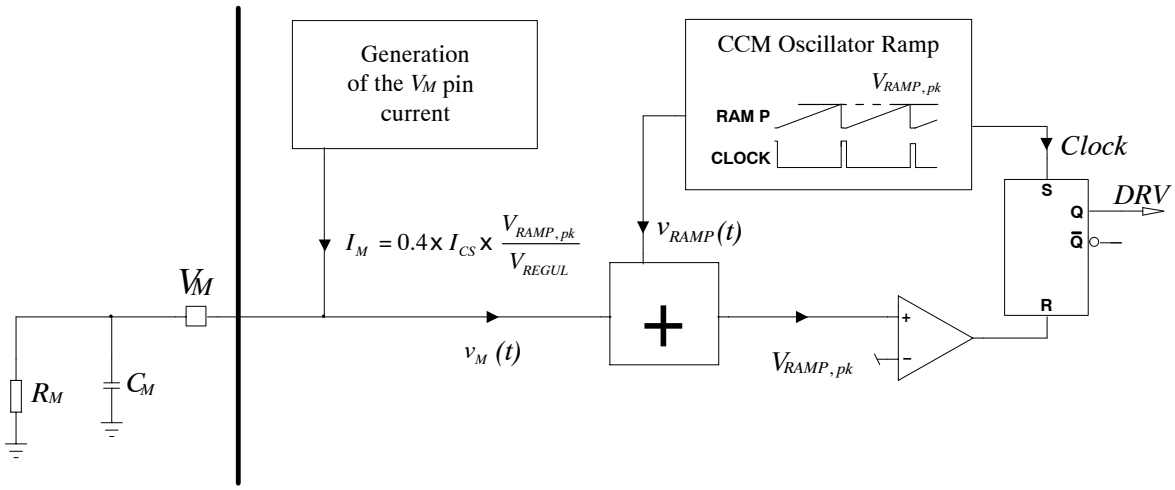


Figure 5. CCM Duty Ratio Control

2. The circuit detects low−line conditions if the HV pin voltage remains below 222 V for 25 ms or more (typical values − see data sheet) and it remains in low−line conditions until the HV pin voltage exceeds 236 V typically. At that moment, it enters the high−line mode.

As highlighted by above equations, resistor R_M adjusts the PFC stage power capability, leading to the two following R_M selection criteria:

– This resistance must be low enough for full−power delivery: $P_{in,avg}\left(V_{CONTROL,\max}\right) > \frac{P_{out,\max}}{\eta}$ whatever the line magnitude is. Due to the CCM gain change in high−line conditions, we need to check that the full power can be delivered at the lowest rms voltage of both the low−line and high−line ranges:

$$R_M \le R_{M,\max} = MIN\left(\frac{2.5\cdot R_{OCP}}{\left(P_{in,avg}\right)_{\max}}\frac{V_{CONTROL,\max}}{R_{sense}}\cdot\frac{\left(V_{in,rms}\right)_{LL}^{2}}{V_{out}}, \frac{0.625\cdot R_{OCP}}{\left(P_{in,avg}\right)_{\max}}\frac{V_{CONTROL,\max}}{R_{sense}}\cdot\frac{\left(\frac{V_{lineselect(LL)}}{\sqrt{2}}\right)^{2}}{V_{out}}\right) \quad \text{(eq. 26)}$$

Where $V_{lineselect(LL)}$ is the lowest line peak voltage for high−line operation ($V_{lineselect(LL)}$ is the threshold for low−line detection − 222 V typically). Note that if the line lowest level of the application was within the high−line range $\left(\sqrt{2}\left(V_{in,rms}\right)_{LL} \ge V_{lineselect(LL)}\right)$, the max value for R_M simplifies as follows:

$$R_{M,\max} = \frac{0.625\cdot R_{OCP}}{\left(P_{in,avg}\right)_{\max}}\frac{V_{CONTROL,\max}}{R_{sense}}\cdot\frac{\left(V_{in,rms}\right)_{LL}^{2}}{V_{out}} \quad \text{(eq. 27)}$$

– This resistance should preferably be selected so that there is no power discontinuity (constant−power transition) when the PFC stage transitions between FCCrM and CCM. In low−line conditions, $V_{CONTROL}$ is abruptly discharged to ($V_{CONTROL}$ / 4) at the FCCrM to CCM transition (and charged to 4×$V_{CONTROL}$ at the CCM to FCCrM transition), in order to provide a large CCM $V_{CONTROL}$ range. Due to this $V_{CONTROL}$ division by four at low line and the change in gain for feed−forward at high line (division by four), the constant−power constraint leads to one single equation where the left side is the instantaneous power delivered in FCCrM and the right side the instantaneous power delivered in CCM just after the transition:

$$\frac{v_{in}^{2}(t)}{2\cdot L\cdot f_{CCM}}\cdot\frac{V_{CONTROL}}{V_{CONTROL,\max}} = 2.5\cdot\frac{R_{OCP}}{R_M}\frac{\frac{V_{CONTROL}}{4}}{R_{sense}}\cdot\frac{v_{in}^{2}(t)}{V_{out}} \quad \text{(eq. 28)}$$

From Eq. 28, we can deduce the following equation which provides the R_M resistance for constant−power transition:

$$R_{M,CP} = 1.25\cdot L\cdot f_{CCM}\cdot\frac{R_{OCP}}{R_{sense}}\cdot\frac{V_{CONTROL,\max}}{V_{out}} \quad \text{(eq. 29)}$$

In our application, the maximum R_M value to meet the full−power delivery constraint ($R_{M,max}$) is:

$$R_{M,\max} = MIN\left(\frac{2.5\cdot 2\cdot 10^{3}}{540}\frac{3.75}{0.03}\cdot\frac{90^{2}}{390}, \frac{0.625\cdot 2\cdot 10^{3}}{540}\frac{3.75}{0.03}\cdot\frac{157^{2}}{390}\right) \cong 18.3\,k\Omega \quad \text{(eq. 30)}$$

The R_M value to meet the constant−power transition criterion is:

$$R_{M,CP} = 1.25\cdot 175\cdot 10^{-6}\cdot 65\cdot 10^{3}\cdot\frac{2\cdot 10^{3}}{30\cdot 10^{-3}}\cdot\frac{3.75}{390} \cong 9.1\,k\Omega \quad \text{(eq. 31)}$$

As aforementioned, for the sake of margin, we want ($R_{M,CP}$) to be 20% below ($R_{M,max}$). This is the case here ($R_{M,CP}$<80%×$R_{M,max}$). Our ($P_{in,transition}$)$_{LL}$ selection is hence correct since with $\left(R_M = R_{M,CP} = 9.1\,k\Omega\right)$, the PFC stage can provide the full power (since ($R_{M,CP}$) is less than (80%×$_{M,max}$)) and can smoothly transition between the FCCrM and CCM modes.

NOTE: Note that if ($R_{M,CP}$) was higher than (80%×$R_{M,max}$), we should increase ($P_{in,transition}$)$_{LL}$ to be able to provide the full power and ensure a constant−power transition.

Also note that if ($R_{M,CP}$) provides the optimal value for smooth transition, a power step in the range of ±50% when transitioning can be managed by the circuit without a risk of erratic operation (repeated transitions between the two modes).

No need hence to look for the exact computed value (as long as it remains below (80%×$R_{M,max}$)). In addition, a different resistance can be wished to meet some application constraints. For instance, you may want to reduce the CCM gain (using R_M closer $R_{M,max}$) to reduce the gap between the power capability of the PFC stage and the power actually needed in your application. To that extend, using $\left(R_M = \sqrt{0.8 \cdot R_{M,\max} \cdot R_{M,CP}}\right)$ can be a good option too.

In our case, we select $\left(R_M = 7.8\,k\Omega\right)$.

A capacitor C_M is to be placed across the V_M pin to filter out the switching ripple. The time constant (R_M×C_M) should be selected in the range of 50 μs or 100 μs, that is, sufficiently large to filter the switching ripple but low enough not to distort the low frequency component (that is the 100 or 120 Hz rectified sinusoid). Thus:

$$C_M \cong \frac{75 \cdot 10^{-6}}{R_M} \qquad \text{(eq. 32)}$$

In our application, this criterion leads to the following C_M value: 9 nF. We take the closest standard value: C_M = 10 nF.

As discussed in [3], dividing the V_M resistors in two resistors as shown by Figure 2, is recommended to clean the operation at very high line where the V_M voltage is close to the threshold of the internal comparator for MOSFET turn off (3.75 V typically). If not, due to the V_M resistors inertia, the circuit may skip cycles at the top of the sinusoid.

Practically, R_{M1} and R_{M2} are selected so that the sum of them equals the computed R_M value and R_{M2} is chosen in the range of 15% of R_M. C_{M1} is computed similarly to C_M as follows:

$$C_{M1} \cong \frac{75 \cdot 10^{-6}}{R_{M1}} \qquad \text{(eq. 33)}$$

A small capacitor C_{M2} is generally recommended to filter out possible surrounding noise but it is low enough to keep a low−inertia signal across R_{M2}.

In our case, we finally opt for:

- R_{M1} = 6.8 kΩ
- R_{M2} = 1 kΩ
- C_{M1} = 10 nF
- C_{M2} not connected

NOTE: The R_M resistance must be selected higher than 4.5 kΩ. If not, the circuit may not be able to charge the V_M pin to SKIP threshold ($V_{SKIP(th)}$).

Power Components

- Diodes bridge

The diodes bridge is mainly selected based on the voltage it must sustain and on the power it must dissipate. [5] shows that a good approximate value of the maximum power loss is given by:

$$P_{bridge} = \frac{4\sqrt{2}}{\pi} \cdot V_f \cdot \frac{\frac{(P_{out})_{\max}}{\eta}}{(V_{in,rms})_{LL}} \cong 1.8 \cdot V_f \cdot \frac{\frac{500}{0.92}}{90} \cong 11 \cdot V_f \qquad \text{(eq. 34)}$$

Assuming a 0.85−V forward voltage per diode (V_f = 0.85 V), the bridge approximately dissipates 9.4 W. Diodes bridge GSIB1580 from Vishay is implemented. A 4.5°C/W heatsink (SK481−50 from Fischer Elektronik) limits the temperature rise to about 45°.

- Boost diode

As discussed in [5], the boost diode selection is critical in CCM applications. The diode current at its turn−off being non−zero, there is significant reverse recovery phenomenon that leads to dissipation in the diode and in the MOSFET. For best efficiency ratios, SiC diodes are to be preferred even if its higher forward voltage offsets some of the gains of reduced switching losses. In this application, SiC diode FFSPF0865 from ON Semiconductor is selected.

The output diode conduction losses can be roughly approximated to ($I_{out,max} \times V_f$), where $I_{out,max}$ is the load maximum current and V_f the diode forward voltage. The maximum output current being nearly 1.3 A (500 W / 390 V), the diode conduction losses are roughly estimated in the range of 2.6 W (assuming V_f = 2.0 V – max instantaneous forward voltage @ 125°C and 8 A specified in the FFSPF0865 data sheet).

A more precise computation could however consist of considering the resistive contribution in the total losses:

$$P_D = (V_{T0} \cdot I_{LOAD}) + (r_D \cdot I_{D,rms}^2) \quad \text{(eq. 35)}$$

where V_{T0} is the threshold voltage, r_D is the dynamic resistance and $I_{D,rms}$ is the diode rms current which can be computed using:

$$I_{D(rms)} \cong I_{L,rms} \sqrt{\frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}}} \quad \text{(eq. 36)}$$

- Power MOSFETs

The MOSFET is selected based on the peak voltage stress ($V_{out,max}$ + margin) and on the maximum rms current flowing through it (($I_{Q(rms)}$)max) which can be approximated using the following equation:

$$(I_{Q,rms})_{max} \cong (I_{L,rms})_{max} \cdot \sqrt{1 - \frac{8\sqrt{2} \cdot (V_{in,rms})_{LL}}{3\pi \cdot V_{out,nom}}} \quad \text{(eq. 37)}$$

In our application, Eq. 37 leads to:

$$(I_{Q,rms})_{max} \cong 6.2 \cdot \sqrt{1 - \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 390}} \cong 5.3 \text{ A} \quad \text{(eq. 38)}$$

Two FCPF165N65 MOSFETs from ON Semiconductor are placed in parallel. Each of them exhibits a maximum drain−to−source on−resistance ($r_{DS(on)}$) of 165 mΩ @ 25°C. Considering a 100% $r_{DS(on)}$ increase at high temperature, the maximum conduction losses are given by:

$$(P_{cond})_{max} \cong \frac{200\% \cdot (r_{DS(on)})_{25°C}}{2} \cdot 5.3^2 \cong \frac{2 \cdot 0.165}{2} \cdot 5.3^2 \cong 4.6 \text{ W} \quad \text{(eq. 39)}$$

As aforementioned, the MOSFETs switching losses are hard to predict. They highly depend on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbering circuitry. Hence, their prediction is a tough and inaccurate exercise that will not be made in this paper. Instead, we will place the MOSFETs and the boost diode on the same heat−sink and consider that as a rule of the thumb, the total power to be dissipated by the heatsink is 4% of the output power (3).

NOTE: Note that to further improve the efficiency, the MOSFET opening can be accelerated using the schematic of Figure 6, where Q_1, a small pnp transistor, amplifies the MOSFET turn off gate current.

3. We rather consider 6% of the output power if the diode bridge is placed on the heatsink. In a single−mains application, this figure could be halved.

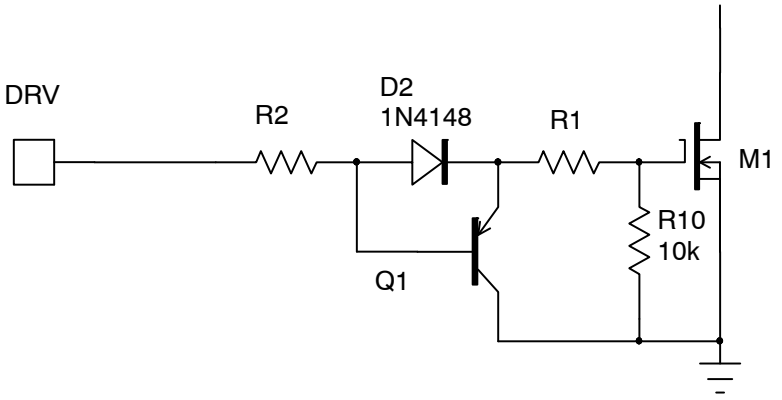


Figure 6. Q1 Speeds Up the MOSFET Turn Off

- Heatsinks

Like in [4], as a rule of thumb, one can estimate that the total power to be dissipated by heatsinks is around:
- 6% of the output power in wide−mains applications
- 3% of the output power in single−mains applications

Such a losses budget must be pessimistic. If experimental tests show that they are worse, the design and/or the components selection must be tweaked if it wished to meet a high efficiency.

No fan is implemented in our 500 W application. It is cooled down by the heatsinks as follows:
- The diodes bridge is fitted on a 4.5°C/W heatsink (SK481−50 from Fischer Elektronik) to limit its temperature rise to about 45°C (about 9.4 W are dissipated)
- The two MOSFETs and the boost diodes share a second heat−sink. Assuming that as a rule of thumb, it will have to dissipate 4% of P_{out} (4% × 500 W ≅ 20 W), a 2.8°C/W heat−sink (ref. SK481−50 from Fischer Elektronik) is implemented which limits the temperature rise to about 56 °C compared to the ambient temperature

- Bulk capacitor design

In addition to the rated voltage, the output capacitor is generally designed considering the 3 following factors:
- The maximum permissible low−frequency ripple of the output voltage. The input current and voltage being both sinusoidal, PFC stages deliver a squared sinusoidal power that matches the load power demand in average only. As a consequence, the output voltage exhibits a low frequency ripple (e.g., 120 Hz in USA) that is inherent to the PFC function
- The rms current flowing through the bulk capacitor. Based on this computation, one must estimate the maximal permissible ESR for an acceptable heating
- The hold−up time specification. The hold−up time is the time for which the power supply must keep providing the full power while the line is gone. The duration of the mains interruption (hold−up time) is generally in the range of 10 or 20 ms

The output voltage peak−to−peak ripple is given by:

$$\Delta V_{out(p-p)} = \frac{P_{out}}{2\pi \cdot f_{line} \cdot C_{bulk} \cdot V_{out,nom}} \quad \text{(eq. 40)}$$

This ripple must keep lower than ±4% of the output voltage (8% peak−to−peak) not to trigger the DRE and OVP functions in normal operation. Thus, we can derive the capacitance the bulk capacitor must exceed not to exhibit too large a low−frequency ripple:

$$C_{bulk} \geq \frac{P_{out,\max}}{2\pi \cdot (f_{line})_{\min} \cdot 8\% \cdot V_{out,nom}^{2}} \quad \text{(eq. 41)}$$

In our application, taking into account the line frequency minimum value (47 Hz), this leads to:

$$C_{bulk} \geq \frac{500}{2\pi \cdot 47 \cdot 8\% \cdot 390^2} \cong 139\,\mu F \quad \text{(eq. 42)}$$

The following equation gives an approximate value of the capacitor rms current:

$$I_{C(rms)} \cong \sqrt{\left(\left(I_{L,rms}\right)^2 \cdot \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}} \right) - \left(\frac{P_{out}}{V_{out,nom}} \right)^2} \quad \text{(eq. 43)}$$

We can derive from Eq. 43 the following estimate of the bulk capacitor maximum rms current:

$$I_{C(rms)_{max}} \cong \sqrt{\left((6.2)^2 \cdot \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 390} \right) - \left(\frac{500}{390} \right)^2} \cong 3.0\ A \quad \text{(eq. 44)}$$

Finally the following expression expresses the minimum bulk capacitance necessary to meet a specified hold−up time ($t_{hold-up}$), where $V_{out,min}$ is the minimum bulk voltage for proper operation of the downstream converter:

$$C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{hold-up}}{V_{out}^2 - V_{out,min}^2} \quad \text{(eq. 45)}$$

The hold−time being not considered here, a 330 μF / 450 V capacitor (861141486022 from Wurth Elektronik) is chosen to satisfy the two other above conditions.

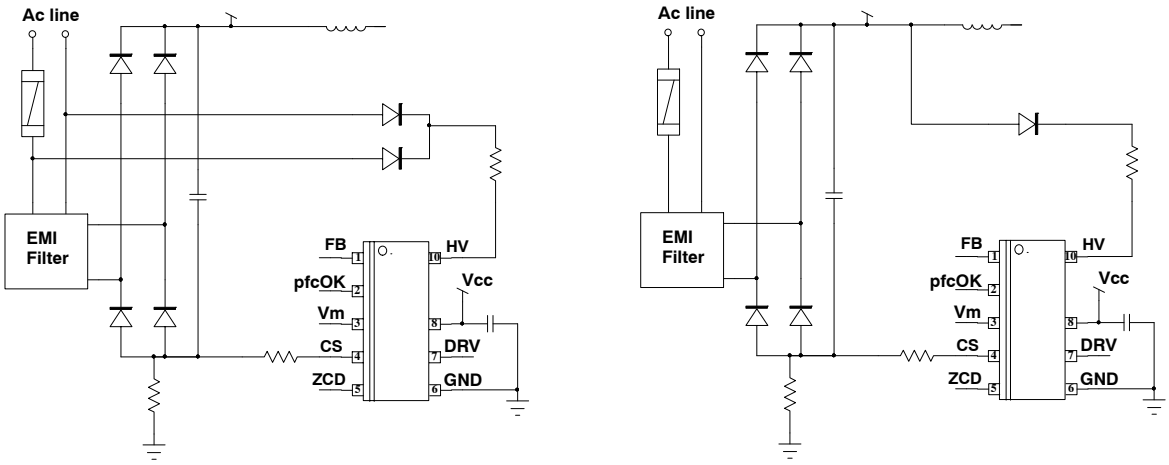
V_{CC} and Sequencing Management

Forward or half−bridge converters take a significant advantage of a narrow input voltage range. In such applications, the PFC stage is expected to start first and to keep on as long as the power supply is powered, the downstream converter being disabled when the output of the PFC stage is nominal. The NCP1618A is specially designed for these applications:

- It incorporates a start−up current source providing a fast charge of the V_{CC} capacitor, thus, easing the PFC stage start of operation
- It features a "*pfcOK*" pin to enable/disable the downstream converter. Practically, it is in high state when the PFC stage is in nominal state and low otherwise (fault or start−up condition). In particular, the *pfcOK* pin is grounded if a line brown−out or a bulk under−voltage is detected

- Input voltage sensing

The NCP1618A monitors the HV pin for line sag and brownout protections and for line range detection. The brownout and line−sag circuitry detects too low line levels and the line range detector determines the presence of either 110 V or 220 V ac mains. Depending on the detected input voltage range device parameters are internally adjusted to optimize the system performance. As shown by Figure 7, line and neutral can be diode "ORed" before connecting to the HV pin (Figure 7a) case) or the HV pin can be simply connected to the rectified voltage (Figure 7b) case). The diodes prevent the pin voltage from going below ground.



a) The line terminals are sensed **b) The input voltage is sensed**

Figure 7. High−Voltage Input Connection

A resistor in series with the diodes is recommended to limit the current during transient events. A low value resistor (5.6 kΩ or less) is generally used to reduce the voltage drop and thus allow more accurate measurement of the input voltage when the start−up circuit is enabled. Also, this resistor must be able to sustain the power dissipation the startup current source causes across it.

Computing the V_{CC} Capacitor Charge Time

The start−up current sourced by the V_{CC} pin (I_{start2}) is 12 mA typically. As detailed in the data sheet, the start−up current is limited to I_{start1} (1 mA typically) when the V_{CC} voltage is below $V_{CC(inhibit)}$ (0.8 V typically). This feature prevents the circuit from overheating if the V_{CC} pin is accidentally grounded.

Thus, the following equation provides the V_{CC} capacitor charge time:

$$t_{ch} = \frac{C_{V_{CC}} \cdot V_{CC(inhibit)}}{I_{start1}} + \frac{C_{V_{CC}} \cdot \left(V_{CC(on)} - V_{CC(inhibit)}\right)}{I_{start2}} \quad \text{(eq. 46)}$$

In our case, using the typical values for $V_{CC(on)}$,$V_{CC(inhibit)}$, I_{start1} and I_{start2}, it comes for a 100 µF V_{CC} capacitance:

$$t_{ch} = \frac{100 \cdot 10^{-6} \cdot 0.8}{10^{-3}} + \frac{100 \cdot 10^{-6} \cdot (17 - 0.8)}{12 \cdot 10^{-3}} \cong 215\ ms \quad \text{(eq. 47)}$$

Where:

- $V_{CC(on)}$ is the typical value of the V_{CC} start−up threshold (17 V)
- $V_{CC(inhibit)}$ is the typical value of the V_{CC} threshold below which the start−up current is reduced (0.8 V)

Using the maximum values for $V_{CC(inhibit)}$ (1.2 V) and $V_{CC(on)}$ (18.2 V) and the minimum values for I_{start1} (0.7 mA) and I_{start2} (6.5 mA), we obtain the following conservative, very worst−case charge time:

$$t_{ch_{WorstCase}} = \frac{100 \cdot 10^{-6} \cdot 1.2}{0.7 \cdot 10^{-3}} + \frac{100 \cdot 10^{-6} \cdot (18.2 - 1.2)}{12 \cdot 10^{-3}} \cong 313\ ms \quad \text{(eq. 48)}$$

- pfcOK

As aforementioned, the *pfcOK* pin is designed to control the operation of the downstream converter. It is in high state when the PFC stage is in nominal operation. On the contrary, the *pfcOK* pin is grounded when the PFC stage is in start−up phase or in a fault condition. Using the *pfcOK* signal to enable/disable it, the downstream converter can be optimally designed for the narrow voltage range nominally provided by the PFC stage in normal operation.

When in high state, the *pfcOK* pin sources a current proportional to the feedback voltage ($k \times V_{FB}$), where k is 10 µA/V typically. In other words, the *pfcOK* pin typically sources 25 µA when the FB voltage is 2.5 V (regulation level). An external resistor is to be placed between the *pfcOK* and GND pins to obtain a voltage V_{pfcOK} which is proportional to the bulk voltage and can serve as a feedforward signal for the downstream converter.

In our application, a 56 kΩ resistor is used so that the *pfcOK* voltage is ($56 \cdot 10^3 \times 25 \cdot 10^{-6} = 1.4$ V) when the output voltage is nominal. A capacitor should be placed between the *pfcOK* and ground pins for decoupling. The pin should not be too much filtered not to degrade the feedforward function. A good trade−off generally consists of setting the filter corner frequency about 5 times higher than the line frequency:

$$C_{pfcOK} \leq \frac{1}{10\pi \cdot R_{pfcOK} \cdot (f_{line})_{max}} \quad \text{(eq. 49)}$$

In our case, Eq. 49 leads to:

$$C_{pfcOK} \leq \frac{1}{10\pi \cdot 56 \cdot 10^3 \cdot 63} \cong 9 \text{ nF} \quad \text{(eq. 50)}$$

A 10 nF ceramic capacitor is placed between the *pfcOK* and *GND* pins for decoupling.

- Feedback network

The output voltage of the PFC stage is externally scaled−down by a resistors divider (R_{FB1} and R_{FB2} of Figure 2) and monitored by the feed−back input (pin1). The bias current of the feedback pin is minimized (less than 500 nA) to allow the use of a high−impedance feed−back network. It is neglected in below calculations. The feedback voltage must equate the internal reference voltage (V_{REF} = 2.5 V) when V_{out} is nominal. In other words:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot V_{out,nom} = V_{REF} \quad \text{(eq. 51)}$$

Or:

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{out,nom}}{V_{REF}} - 1 \quad \text{(eq. 52)}$$

Another constraint on the feedback resistors relates to the power R_{FB1} and R_{FB2} dissipate as they are biased by the V_{out} high−voltage rail (in the range of 390 V typically). If the impedance ($R_{FB1} + R_{FB2}$) is low, R_{FB1} and R_{FB2} can easily consume several hundreds of milliwatts and degrade the standby performance.

In steady−state, the feedback voltage is in the range of the 2.5 V regulation reference voltage (V_{REF}). The nominal feedback bias current can hence be defined as a function of feedback bottom resistor (R_{FB2}) as follows:

$$I_{FB} = \frac{V_{REF}}{R_{FB2}} \quad \text{(eq. 53)}$$

Trade−off between losses and noise immunity dictates the choice of this resistor. Resistors up to 56 kΩ ($I_{FB} \cong 50$ μA) generally give good results. Higher values can be considered if allowed by the board PCB layout and if the impedance remains compatible which the 250 nA sink current (500 nA max. on the −40°C to 125°C temperature range) built−in to ground the feedback pin and disable the driver if the pin is accidentally open. If I_{FB} is set below 50 μA, the regulation level may be significantly impacted by the 250 nA sink current. In our application, we target a bias current in the range of 100 μA which generally gives a good trade−off between losses and noise immunity. This criterion leads to:

$$R_{FB2} = \frac{V_{REF}}{100\,\mu A} = 25\ k\Omega \quad \text{(eq. 54)}$$

(R_{FB2} = 27 kΩ) is finally selected. Following Eq. 52, R_{FB1} is given by:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1 \right) \quad \text{(eq. 55)}$$

We target a 390 V regulation level, hence:

$$R_{FB1} = 27\ k\Omega \cdot \left(\frac{390}{2.5} - 1 \right) = 4185\ k\Omega \quad \text{(eq. 56)}$$

For safety reasons, several resistors should be placed in series instead of a single R_{FB1} resistor. In our application, we choose a (1800 kΩ + 1800 kΩ + 560 kΩ) network. This selection together with (R_{FB2} = 27 kΩ) leads to:

$$V_{out,nom} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot V_{REF} = \frac{1800 + 1800 + 560 + 27}{27} \cdot 2.5 \text{ V} \cong 388 \text{ V} \quad \text{(eq. 57)}$$

Zero Current Detection (ZCD)

The NCP1618A optimizes the efficiency by turning on the MOSFET at the very valley when operating in critical and discontinuous conduction modes. For this purpose, the circuit is designed to monitor the voltage of a small winding taken off of the boost inductor. This auxiliary winding (called the "zero current detector" or ZCD winding) gives a scaled version of the inductor voltage which is easily usable by the controller. The PFC stage being a boost converter, this auxiliary winding voltage provides:

- $-\left(\frac{N_{AUX}}{N_P}\cdot v_{in}(t)\right)$ during the MOSFET conduction time
- $\left(\frac{N_{AUX}}{N_P}(V_{out}-v_{in}(t))\right)$ during the demagnetization time. This voltage used to detect the zero current detection can be small when the input voltage is nearly the output voltage.
- A voltage oscillating around zero during dead−times

The NCP1618A embeds an internal comparator to monitor such a signal. Practically, during the off−time, it compares the ZCD pin voltage to an upper threshold V_{ZCDH} (1 V typically) and to a lower threshold V_{ZCDL} (0.5 V typically) to detect falling edges of the ZCD signal, these events being indicative of the end of the demagnetization phase and/or of the valleys of the MOSFET Drain−source voltage.

Several options are possible for an accurate ZCD and OVP2 as discussed in [7]. Among them, the circuitry of Figure 8 is recommended when the direct sensing of the output voltage rail may be too dissipative to meet standby low power requirements. In this circuit, R_1 being small (e.g. 22 Ω), capacitor C_1 is charged to $\left(\frac{N_{AUX}}{N_P}\cdot v_{in}(t)\right)$ during the on−time. If C_1 is lightly loaded, its voltage remains almost unchanged during the off−time and thus, the D_1 cathode voltage becomes $\left(\left(\frac{N_{AUX}}{N_P}(V_{out}-v_{in}(t))\right)+\left(\frac{N_{AUX}}{N_P}\cdot v_{in}(t)\right)\right)$, that is, $\left(\frac{N_{AUX}}{N_P}\cdot V_{out}\right)$ during the demagnetization time. This voltage is stored and clamped by D_7, C_2 so that the C_2 voltage is $(N \times V_{OUT})$ where $\left(N=\frac{N_{AUX}}{N_P}\right)$. C_2 delays the OVP2 activation. This is particularly useful when the system restarts after an interruption. In this case, it prevents that an incorrect initial value of the C_2 voltage causes OVP2 spurious tripping. Note that as the rule of thumb, C_2 can be selected 10 times higher than C_1 ($C_2 \cong 10 \times C_1$). Note that capacitor C_2 can also be referenced to V_{CC} instead of ground so that a voltage for proper ZCD immediately exists whenever the circuit enters operation.

This circuitry hence provides a voltage representative of the output is obtained for a redundant over−voltage protection. As detailed in [8], a good starting point for the time constants could be in the following range for a 50− or 60−Hz line:

$$R_1 \cdot C_1 \cong 100\ ns \qquad \text{(eq. 58)}$$

$$(R_2 + R_3)\cdot C_1 \cong 600\ \mu s \qquad \text{(eq. 59)}$$

Diode D_2 ensures that the ZCD/OVP2 pin gets below the ZCD internal threshold, when the auxiliary winding drops to zero.

NOTE: Time constant ($R_1 \times C_1$) can actually be increased to 500 ns or 1 μs. This can help avoid charging C_1 on spikes and limit the impact of the input voltage ripple on the generated image of the output voltage. R_1 must however remain low enough to properly force the ZCD pin voltage below $V_{ZCD(th)L}$ (0.5 V typically) when the auxiliary winding voltage is zero

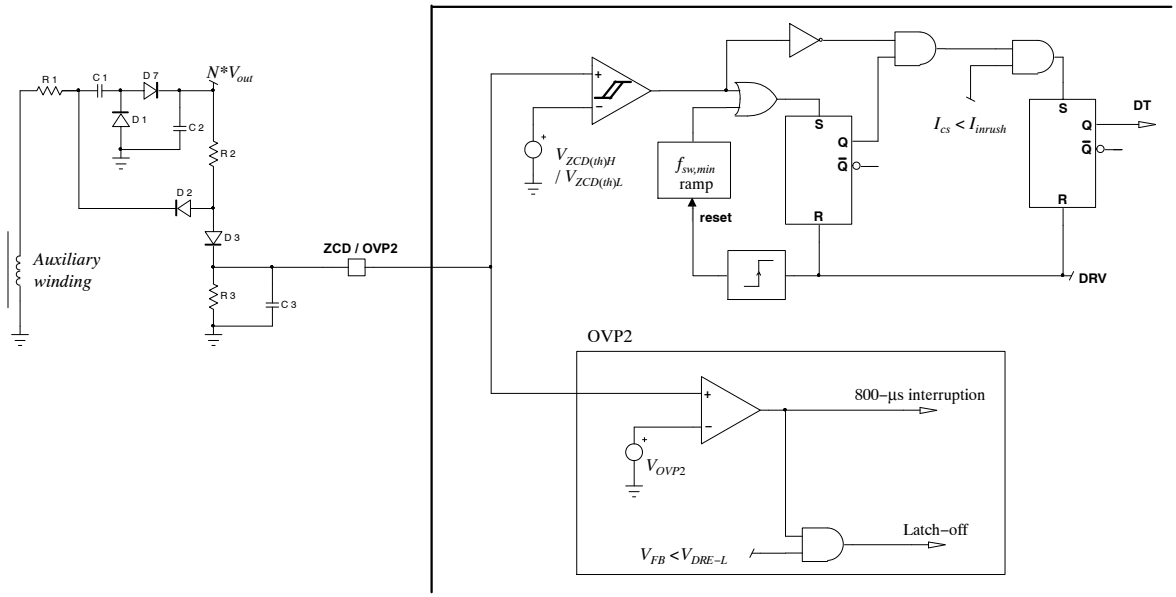


Figure 8. Zero Current Detection Block

As shown by Figure 8, the ZCD signal is compared to V_{OVP2} (4 V typically) for OVP2 detection (4). The ratio (R_2/R_3) will set the OVP2 threshold. During the demagnetization phase, the ZCD voltage is:

$$V_{ZCD} = \frac{R_3}{R_2 + R_3}\left(\left(\frac{N_{AUX}}{N_P}\cdot V_{out}\right) - V_{D_3}\right) \quad \text{(eq. 60)}$$

Thus, if $V_{out,OVP2}$ is the output voltage level above which an OVP2 fault is detected, replacing V_{ZCD} by the OVP2 threshold V_{OVP2}, we obtain:

$$\frac{R_2 + R_3}{R_3} = \left(\frac{N_{AUX}}{N_P}\cdot\frac{V_{out,OVP2}}{V_{OVP2}}\right) - \frac{V_{D_3}}{V_{OVP2}} \quad \text{(eq. 61)}$$

The R_3 value is generally selected equal to 10 kΩ.

$$R_3 \cong 10\ k\Omega \quad \text{(eq. 62)}$$

If we target 440 V for $V_{out,OVP2}$, it comes:

$$R_2 \cong R_3 \cdot \left(\left(\frac{N_{AUX}}{N_P}\cdot\frac{V_{out,OVP2}}{V_{OVP2}}\right) - \frac{V_{D_3}}{V_{OVP2}} - 1\right) \cong 10\cdot 10^3 \cdot \left(\left(\frac{1}{10}\cdot\frac{440}{4}\right) - \frac{0.6}{4} - 1\right) \cong 98.5\ \text{k}\Omega \quad \text{(eq. 63)}$$

Finally, using 59 , we can compute C_1:

$$C_1 \cong \frac{600\cdot 10^{-6}}{R_2 + R_3} = \frac{600\cdot 10^{-6}}{100\cdot 10^3 + 10\cdot 10^3} \cong 5.5\,nF \quad \text{(eq. 64)}$$

A 4.7 nF capacitor was used.

4. (This function provides a redundant OVP protection for safety. If V_{ZCD} exceeds V_{OVP2}, the PFC stage stops operating for 800 µs. In addition, if when an OVP2 fault is detected, the dynamic response enhancer is engaged (indicating an undershoot being detected by the feedback pin), the circuit detects that one of the two networks for output voltage sensing is wrong. As a consequence, the circuit latches off. See Figure 8.

Layout and Noise Immunity Considerations

The NCP1618A is not particularly sensitive to noise. However, usual layout rules for power supply apply. Among them, let us remind the following ones:

- The loop area of the power train must be minimized
- Star configuration for the power ground that provides the current return path
- Star configuration for the circuit ground
- The circuit ground and the power ground should be connected by one single path
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{SENSE}).
- A 100 nF or 220 nF ceramic capacitor should be placed between the circuit V_{CC} and *GND* pins, with a minimized connection length
- If a filtering capacitor (C_{CS} of Figure 4) is implemented for current sensing, its negative terminal should be connected to the circuit ground rather than to the power ground
- The components (resistors or capacitors) that program the circuit operation must be placed as close as possible to the pin they drive.
- As aforementioned, it is furthermore recommended to filter the signal applied to the *FB*, *CS*, *pfcOK*, V_M and *ZCD* pins to protect them from possible surrounding noise. It must not be excessive however not to distort the voltage sensed by these pins. See the corresponding sections for more details.

APPLICATION SCHEMATICS

- Power Section

Some common PFC stage elements not discussed in the application note since nonspecific to the controller like the inrush current management or a circuitry for X2 capacitors discharge are not included in this schematic.

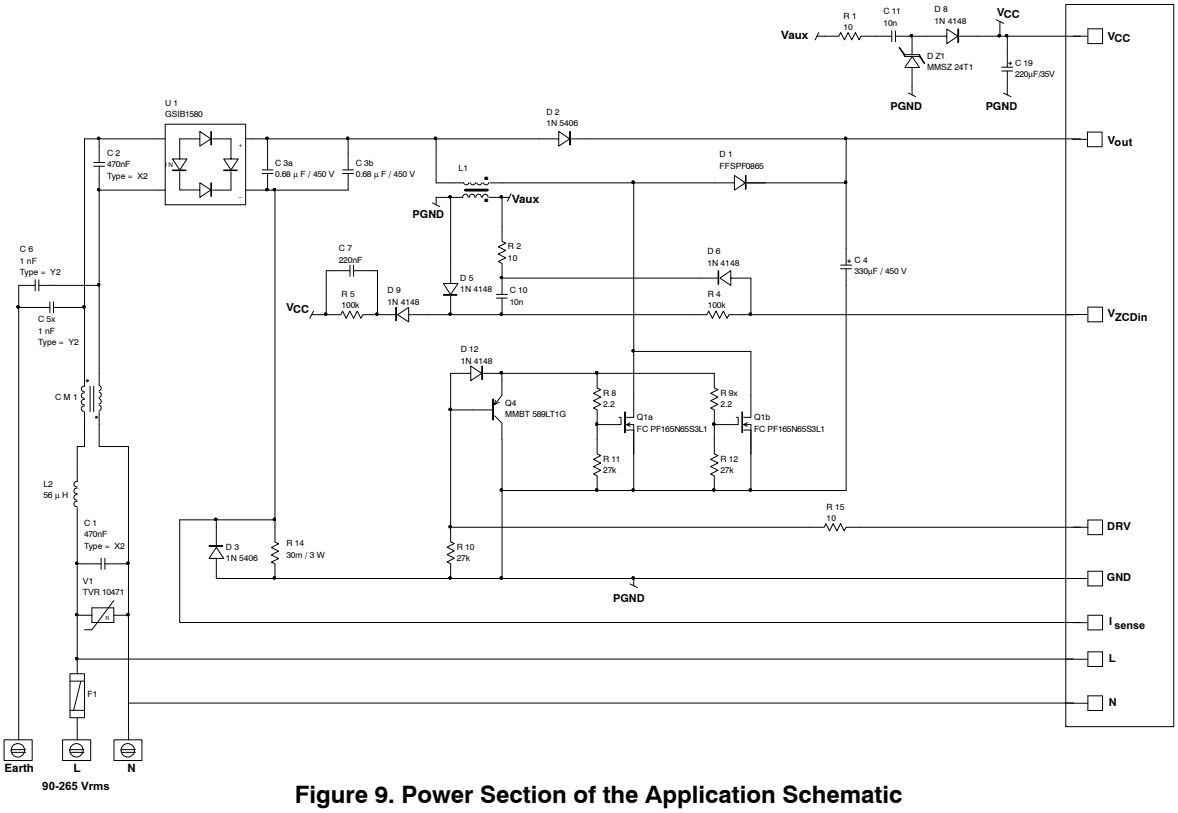


Figure 9. Power Section of the Application Schematic

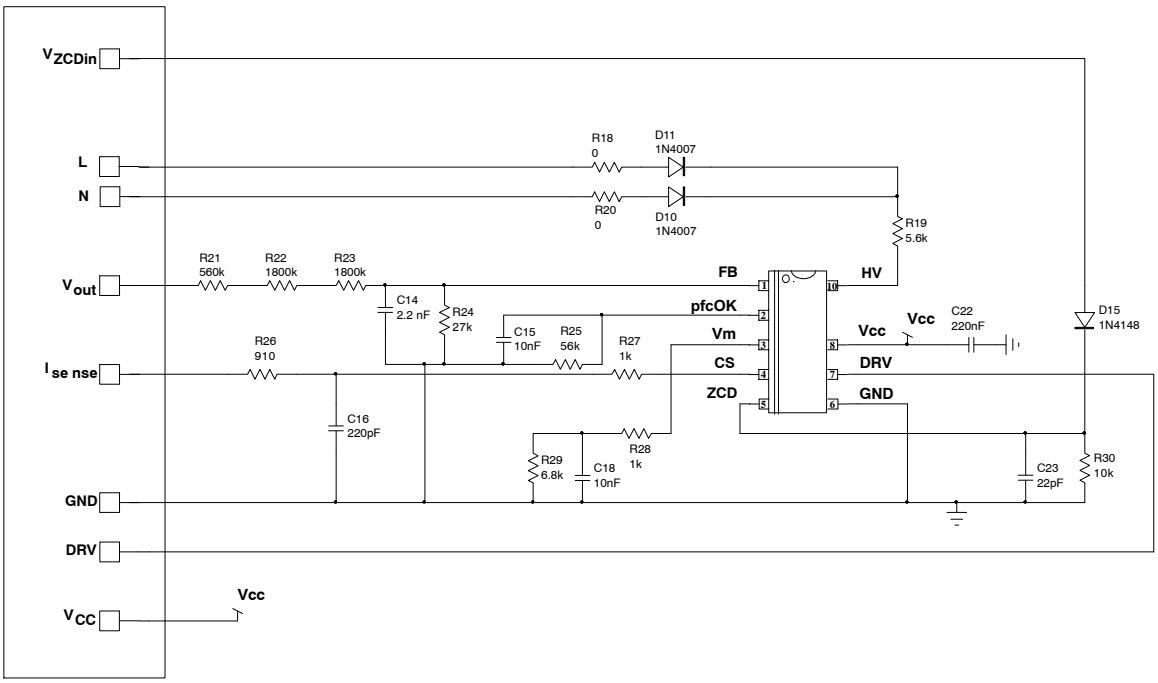


Figure 10. Control Section of the Application Schematic

Conclusion

This application note proposes a systematic process for the eased design of an efficient multimode PFC stage. More specifically, this paper provides the key equations and design criteria. This dimensioning process is illustrated by the practical example of the 500 W, wide−mains evaluation board [9]. Note that a design spreadsheet [10] automates the dimensioning process.

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