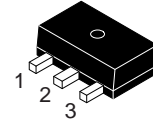


# Bipolar Transistor

(-)50 V, (-)7 A, Low VCE(sat), (PNP) NPN  
Single PCP

## 2SA2016, 2SC5569



SOT-89 / PCP-1  
CASE 419AU

### 特長

- FBET, MBIT プロセス採用
- コレクタ・エミッタ飽和電圧が低い
- 超小型パッケージのため、セットの小型化, 薄型化が可能である
- 許容損失が大きい
- 電流容量が大きい
- スイッチングスピードが速い

### 用途

- リレードライブ, ランプドライブ, モータドライブ, フラッシュ

( )内は 2SA2016 の場合を示す。

### 絶対最大定格 ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

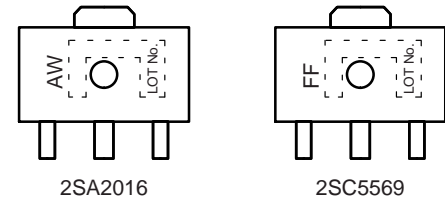
項目	記号	条件	定格値	Unit
コレクタ・ベース電圧	V <sub>CB0</sub>		(-50) 100	V
コレクタ・エミッタ電圧	V <sub>CES</sub>		(-50) 100	V
コレクタ・エミッタ電圧	V <sub>CEO</sub>		(-)50	V
エミッタ・ベース電圧	V <sub>EBO</sub>		(-)6	V
コレクタ電流	I <sub>C</sub>		(-)7	A
コレクタ電流 (パルス)	I <sub>CP</sub>		(-)10	A
ベース電流	I <sub>B</sub>		(-)1.2	A
コレクタ損失	P <sub>C</sub>	セラミック基板 (250 mm <sup>2</sup> x 0.8 mm) 装着時	1.3	W
		T <sub>c</sub> = 25°C	3.5	W
接合部温度	T <sub>j</sub>		150	°C
保存周囲温度	T <sub>stg</sub>		-55~+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

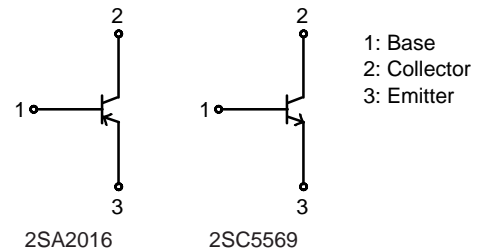
(参考訳)

最大定格を超えるストレスは、デバイスにダメージを与える危険性があります。これらの定格値を超えた場合は、デバイスの機能性を損ない、ダメージが生じ、信頼性に影響を及ぼす危険性があります。

### マーキング



### 電気的接続図



### ORDERING INFORMATION

Device	パッケージ名 (JEITA, JEDEC)	最小梱包単位†
2SA2016-TD-E	PCP (Pb-Free)	1000 / Tape & Reel
2SC5569-TD-E		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

電気的特性 ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

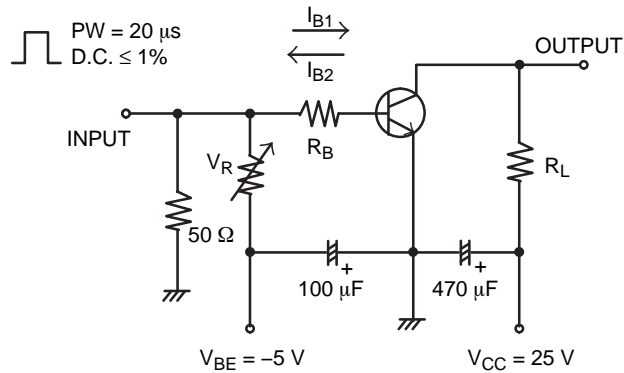
項目	記号	条件	定格値			Unit
			Min	Typ	Max	
コレクタシャ断電流	$I_{CBO}$	$V_{CB} = (-)40\text{ V}, I_E = 0\text{ A}$	-	-	(-)0.1	$\mu\text{A}$
エミッタシャ断電流	$I_{EBO}$	$V_{EB} = (-)4\text{ V}, I_C = 0\text{ A}$	-	-	(-)0.1	$\mu\text{A}$
直流電流増幅率	$h_{FE}$	$V_{CE} = (-)2\text{ V}, I_C = (-)500\text{ mA}$	200	-	560	
利得帯域幅積	$f_T$	$V_{CE} = (-)10\text{ V}, I_C = (-)500\text{ mA}$	-	(290) 330	-	MHz
出力容量	Cob	$V_{CB} = (-)10\text{ V}, f = 1\text{ MHz}$	-	(50) 28	-	pF
コレクタ・エミッタ飽和電圧	$V_{CE(sat)1}$	$I_C = (-)3.5\text{ A}, I_B = (-)175\text{ mA}$	-	(-230) 160	(-390) 240	mV
	$V_{CE(sat)2}$	$I_C = (-)2\text{ A}, I_B = (-)40\text{ mA}$	-	(-240) 110	(-400) 170	mV
ベース・エミッタ飽和電圧	$V_{BE(sat)}$	$I_C = (-)2\text{ A}, I_B = (-)40\text{ mA}$	-	(-)0.83	(-)1.2	V
コレクタ・ベース降伏電圧	$V_{(BR)CBO}$	$I_C = (-)10\text{ }\mu\text{A}, I_E = 0\text{ A}$	(-50) 100	-	-	V
コレクタ・エミッタ降伏電圧	$V_{(BR)CES}$	$I_C = (-)100\text{ }\mu\text{A}, R_{BE} = 0\text{ }\Omega$	(-50) 100	-	-	V
コレクタ・エミッタ降伏電圧	$V_{(BR)CEO}$	$I_C = (-)1\text{ mA}, R_{BE} = \infty$	(-)50	-	-	V
エミッタ・ベース降伏電圧	$V_{(BR)EBO}$	$I_E = (-)10\text{ }\mu\text{A}, I_C = 0\text{ A}$	(-)6	-	-	V
ターンオン時間	$t_{on}$	指定回路において	-	(40) 30	-	ns
蓄積時間	$t_{stg}$		-	(225) 420	-	ns
下降時間	$t_f$		-	25	-	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(参考訳)

製品パラメータは、特別な記述が無い限り、記載されたテスト条件に対する電気的特性で示しています。異なる条件下で製品動作を行った時には、電気的特性で示している特性を得られない場合があります。

スイッチングタイム測定回路図



$I_C = 20I_{B1} = -20I_{B2} = 2.5\text{ A}$   
PNP の場合極性逆

図 1. スwitchingタイム測定回路図

2SA2016, 2SC5569

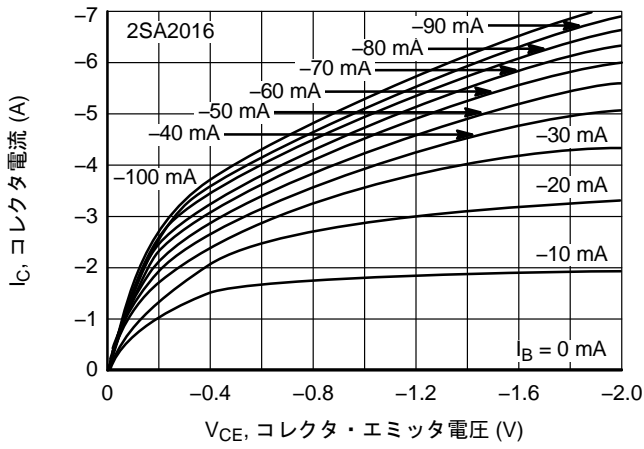


図 2.  $I_C - V_{CE}$

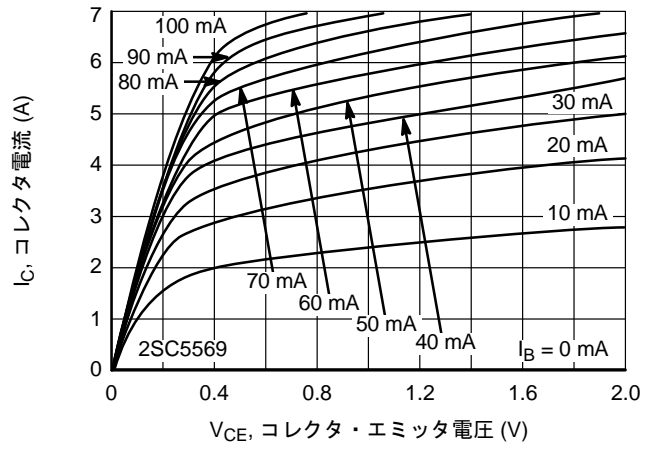


図 3.  $I_C - V_{CE}$

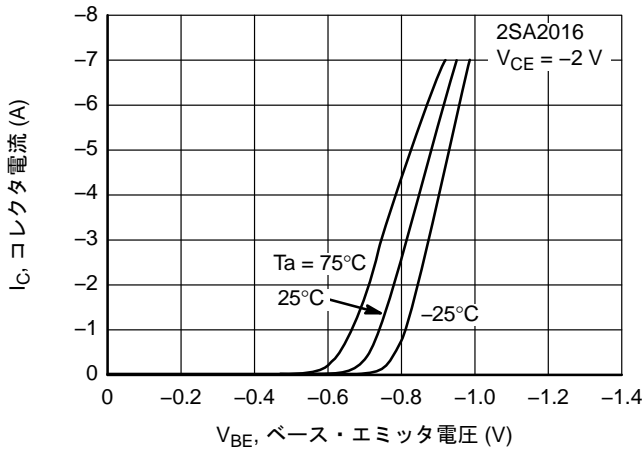


図 4.  $I_C - V_{BE}$

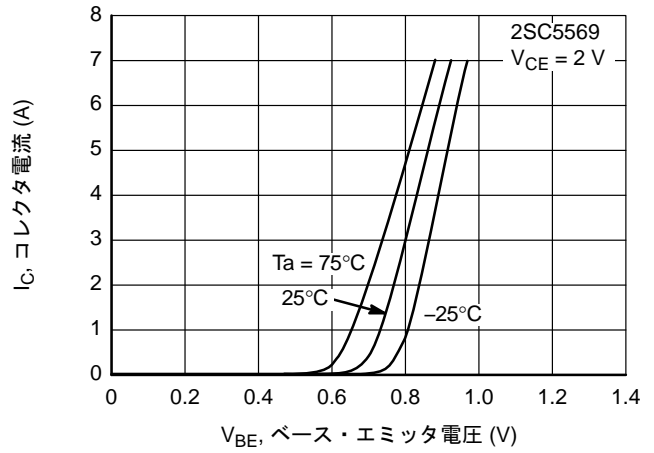


図 5.  $I_C - V_{BE}$

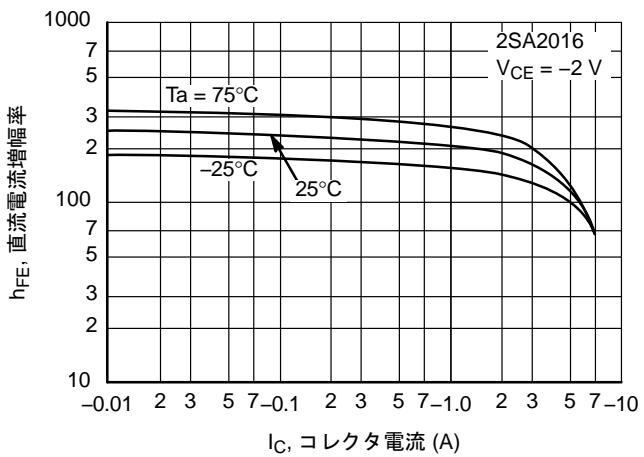


図 6.  $h_{FE} - I_C$

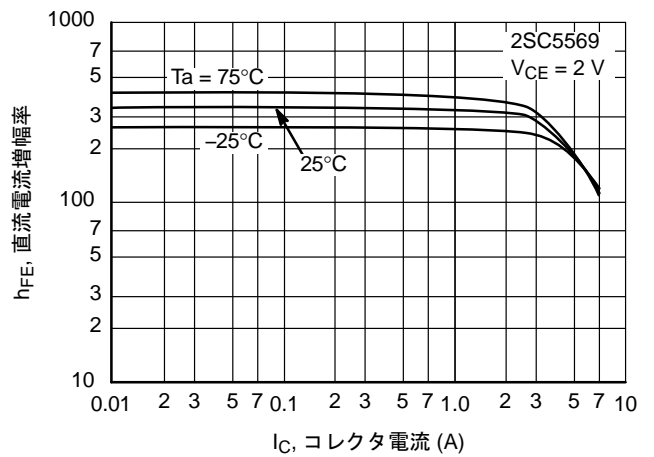


図 7.  $h_{FE} - I_C$

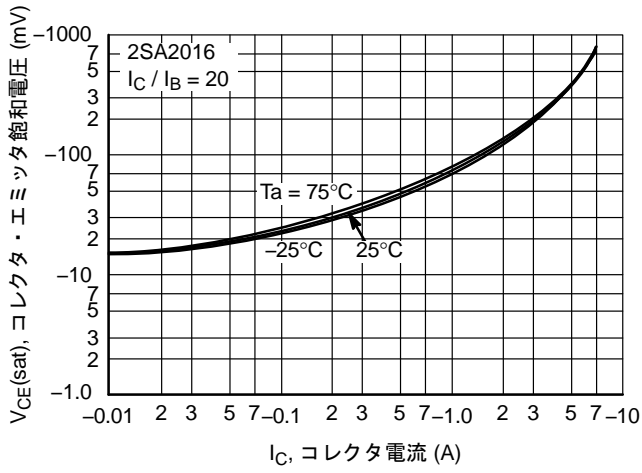


図 8.  $V_{CE(sat)} - I_C$

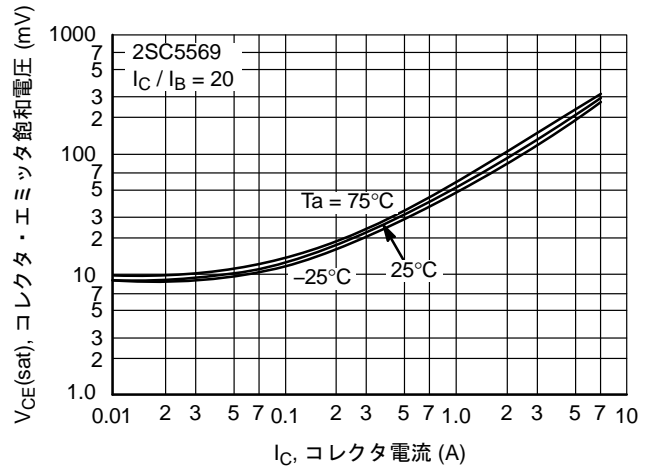


図 9.  $V_{CE(sat)} - I_C$

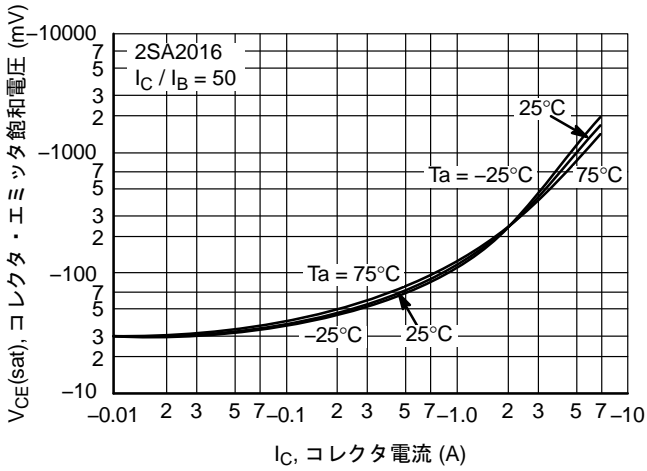


図 10.  $V_{CE(sat)} - I_C$

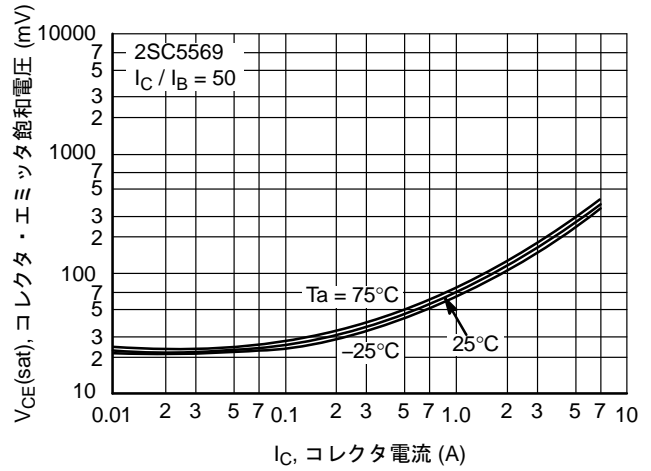


図 11.  $V_{CE(sat)} - I_C$

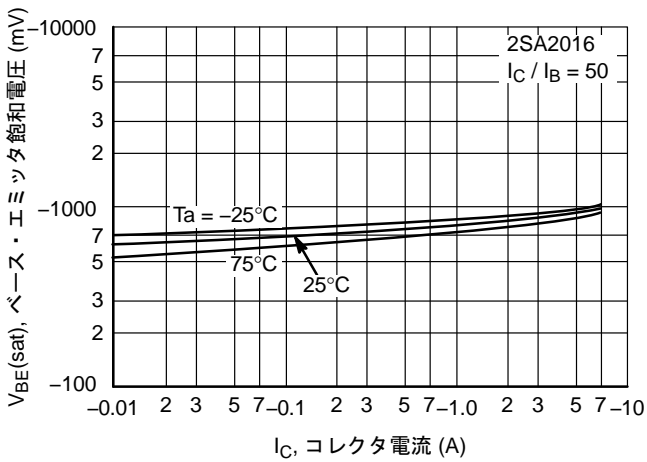


図 12.  $V_{BE(sat)} - I_C$

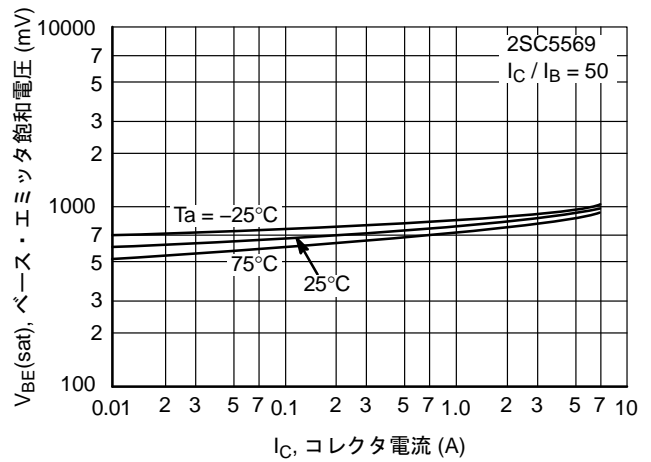


図 13.  $V_{BE(sat)} - I_C$

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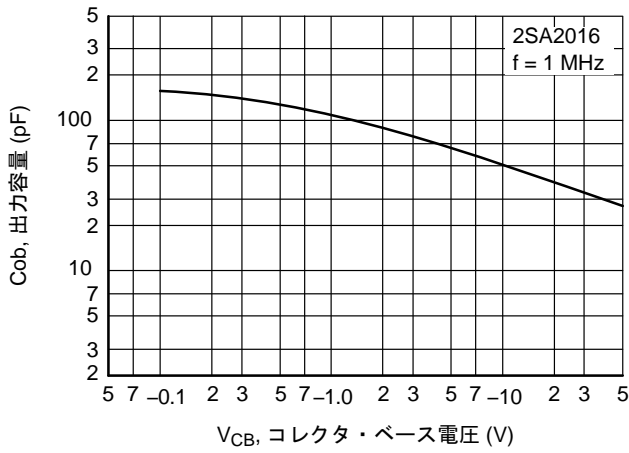


図 14. Cob -  $V_{CB}$

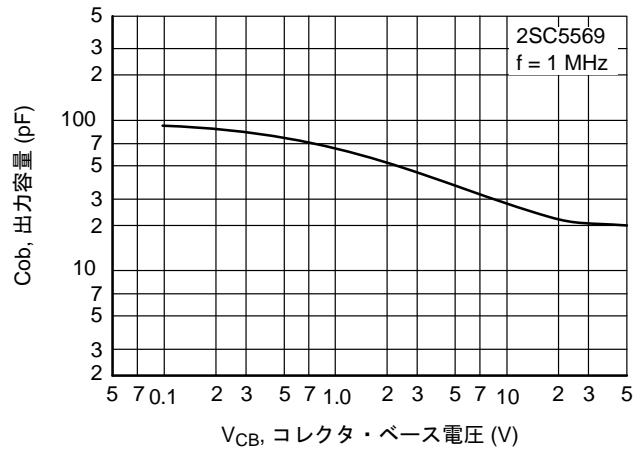


図 15. Cob -  $V_{CB}$

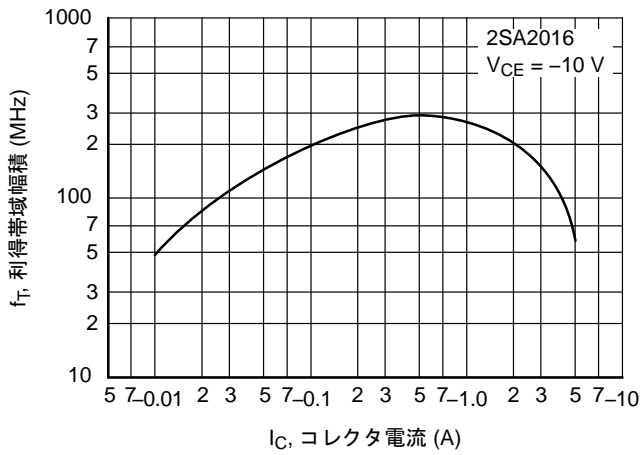


図 16.  $f_T - I_C$

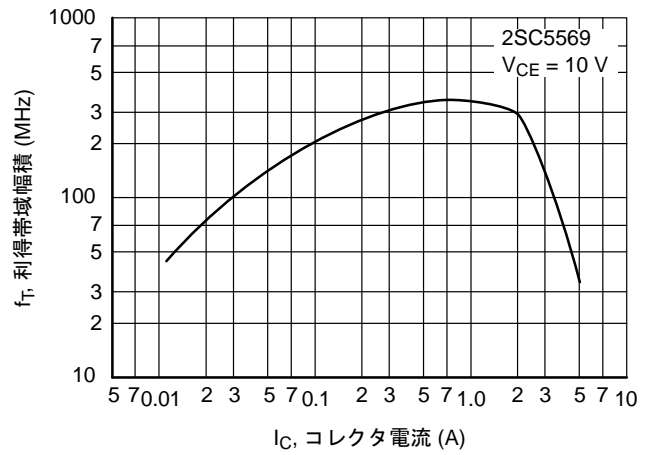


図 17.  $f_T - I_C$

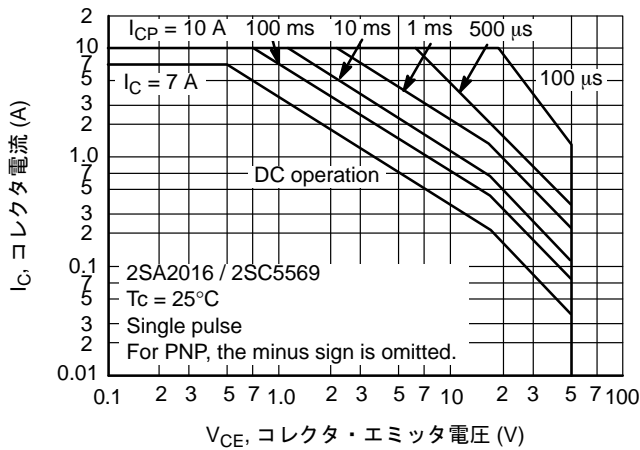


図 18. ASO

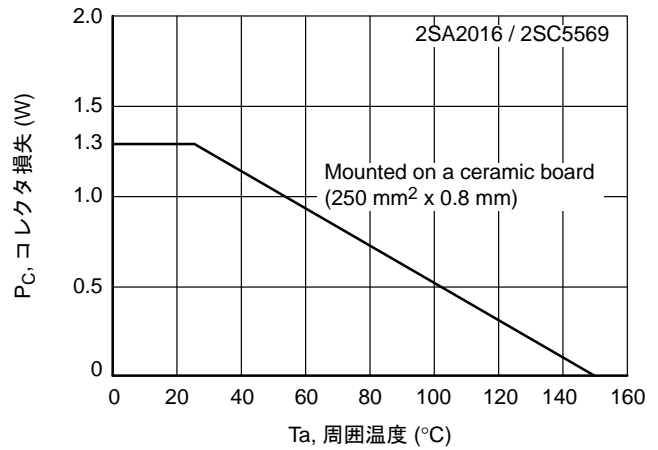


図 19.  $P_C - T_a$

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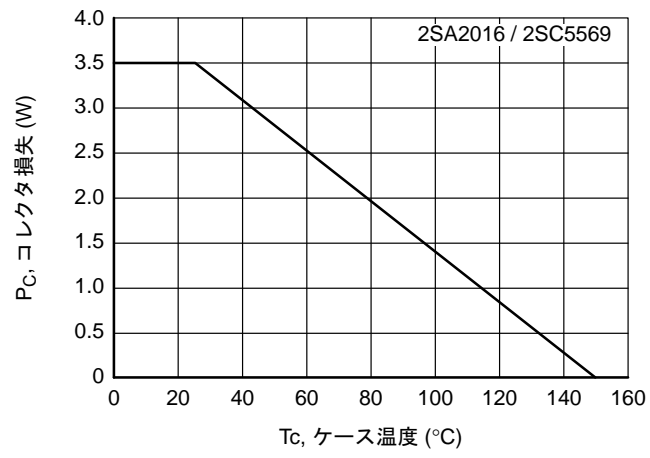


図 20.  $P_C - T_C$

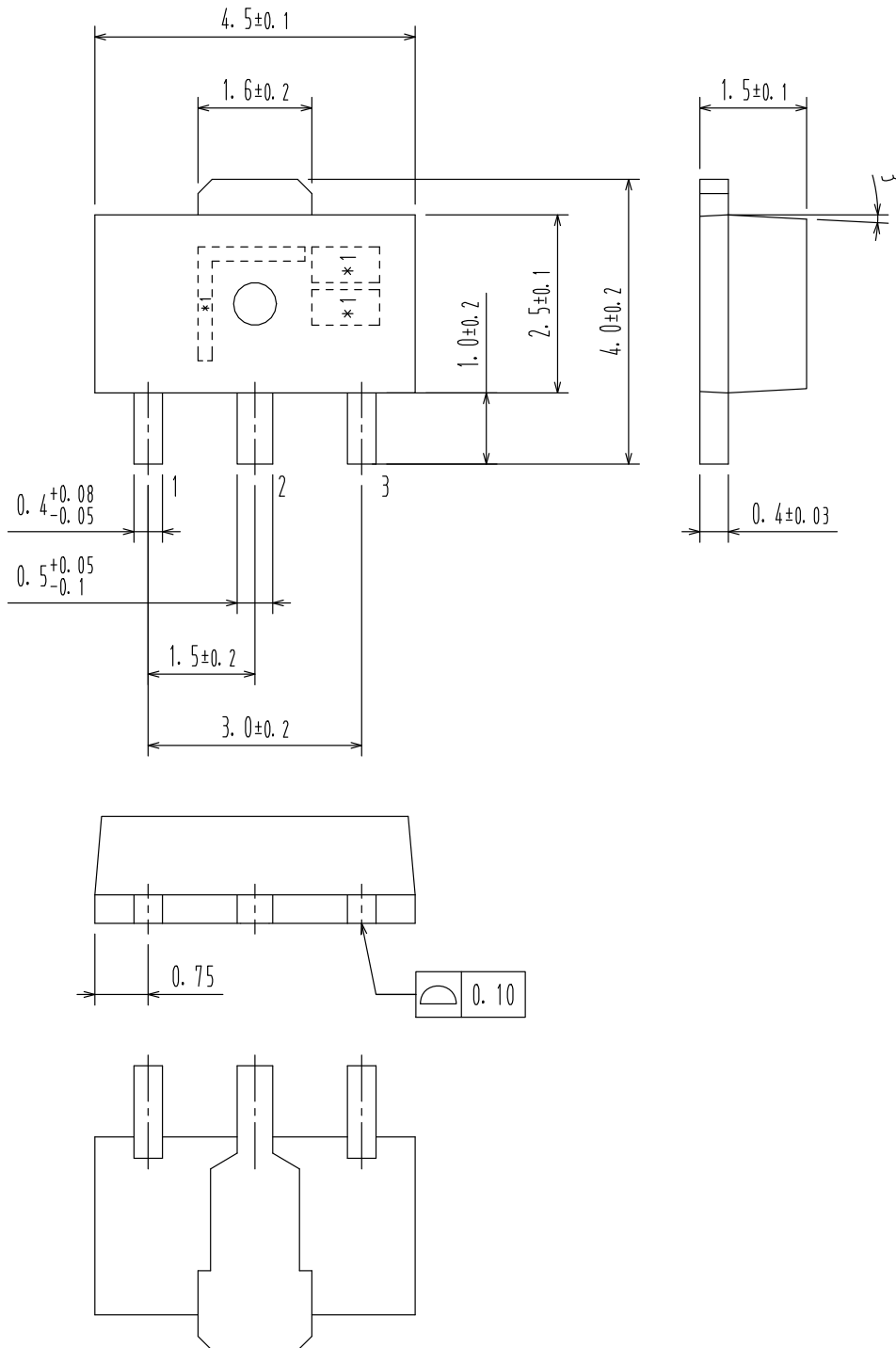
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®



**SOT-89 / PCP-1**  
**CASE 419AU**  
**ISSUE O**

DATE 30 APR 2012



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