## ADM1025，ADM1025A

## Product Preview <br> Low Cost PC Hardware Monitor ASIC

The ADM1025／ADM1025A1 is a complete system hardware monitor for microprocessor－based systems，providing measurement and limit comparison of various system parameters．Five voltage measurement inputs are provided for monitoring $2.5 \mathrm{~V}, 3.3 \mathrm{~V}, 5 \mathrm{~V}$ ，and 12 V power supplies and the processor core voltage．The ADM1025／ADM1025A can monitor a sixth power supply voltage by measuring its own $\mathrm{V}_{\mathrm{CC}}$ ．One input（two pins）is dedicated to a remote temperature－sensing diode，and an onchip temperature sensor allows ambient temperature to be monitored．The ADM1025A has open－drain VID inputs while the ADM1025 has on－chip $100 \mathrm{k} \Omega$ pull－ups on the VID inputs．

Measured values and in／out of limit status can be read out via an $I^{2} \mathrm{C}$ compatible serial System Management Bus．The device can be controlled and configured over the same serial bus．The device also has a programmable $\overline{\mathrm{INT}}$ output to indicate undervoltage，overvoltage， and overtemperature conditions．

The ADM1025／ADM1025A＇s 3．0 V to 5．5 V supply voltage range， low supply current，and $\mathrm{I}^{2} \mathrm{C}$ compatible interface make it ideal for a wide range of applications．These include hardware monitoring and protection applications in personal computers，electronic test equipment，and office electronics．

## Features

－Up to 8 Measurement Channels
－ 5 Inputs to Measure Supply Voltages
－ $\mathrm{V}_{\mathrm{CC}}$ Monitored Internally
－External Temperature Measurement with Remote Diode
－On－chip Temperature Sensor
－ 5 Digital Inputs for VID Bits
－Integrated $100 \mathrm{k} \Omega$ Pull－ups on VID Pins（ADM1025 Only）
－LDCM Support
－ $\mathrm{I}^{2} \mathrm{C}$ Compatible System Management Bus（SMBus）
－Programmable RST Output Pin
－Programmable INT Output Pin
－Configurable Offset for Internal／External Channel
－Shutdown Mode to Minimize Power Consumption
－Limit Comparison of All Monitored Values

## Applications

－Network Servers and Personal Computers
－Microprocessor－based Office Equipment
－Test Equipment and Measuring Instruments

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QSOP－16
CASE 492

PIN ASSIGNMENT


MARKING DIAGRAM
日月 日明
1025A
RQZ
O \＃YYWW
昭昭昭昭

| 1025ARQZ | $=$ Special Device Code |
| :--- | :--- |
| $\#$ | $=$ Pb－Free Package |
| YY | $=$ Year |
| WW | $=$ Work Week |

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet．

This document contains information on a product under development．ON Semiconductor reserves the right to change or discontinue this product without notice．


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

| Rating | Value | Unit |
| :--- | :---: | :---: |
| Positive Supply Voltage (VCC) | 6.5 | V |
| Voltage on $12 \mathrm{~V} \mathrm{VIN}_{\text {IN }}$ Pin | 20 | V |
| Voltage on Any Input or Output Pin | -0.3 to +6.5 | V |
| Input Current at Any Pin | $\pm 5$ | mA |
| Package Input Current | $\pm 20$ | mA |
| Maximum Junction Temperature (TJMAX) | 150 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| Lead Temperature, Soldering <br> Vapor Phase (60 sec) <br> Infrared (15 sec) | 215 | ${ }^{\circ} \mathrm{C}$ |
| ESD Rating All Pins | 200 |  |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.
Table 2. THERMAL CHARACTERISTICS

| Package Type | $\boldsymbol{\theta}_{\text {JA }}$ | $\boldsymbol{\theta}_{\text {Jc }}$ | Unit |
| :--- | :---: | :---: | :---: |
| 16-lead QSOP | 105 | 39 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

## ADM1025, ADM1025A

Table 3. PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic | Description |
| :---: | :---: | :---: |
| 1 | SDA | Digital I/O. Serial bus bidirectional data. Open-drain output. |
| 2 | SCL | Digital Input. Serial bus clock. |
| 3 | GND | System Ground |
| 4 | $\mathrm{V}_{\mathrm{CC}}$ | Power. Can be powered by 3.3 V standby power if monitoring in low power states is required. This pin also serves as the analog input to monitor $\mathrm{V}_{\mathrm{CC}}$. |
| 5 | VIDO | Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0-VID3 Status Register. It has an on-chip $100 \mathrm{k} \Omega$ pull-up resistor (ADM1025 only). |
| 6 | VID1 | Digital Input. Core voltage ID readouts from the processor. This value is read into the VIDO-VID3 Status Register. It has an on-chip $100 \mathrm{k} \Omega$ pull-up resistor (ADM1025 only). |
| 7 | VID2 | Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0-VID3 Status Register. It has an on-chip $100 \mathrm{k} \Omega$ pull-up resistor (ADM1025 only). |
| 8 | VID3 | Digital Input. Core voltage ID readouts from the processor. This value is read into the VID0-VID3 Status Register. It has an on-chip $100 \mathrm{k} \Omega$ pull-up resistor (ADM1025 only). |
| 9 | D-/NTI | Analog/Digital Input. Connected to cathode of external temperature sensing diode. If held high at power-up, it initiates NAND tree test mode. |
| 10 | D+ | Analog Input. Connected to anode of external temperature sensing diode. |
| 11 | $12 \mathrm{~V}_{\text {IN }} / \mathrm{VID} 4$ | Programmable Analog/Digital Input. Defaults to $12 \mathrm{~V}_{\mathrm{IN}}$ analog input at power-up but may be programmed as VID4 Core Voltage ID readout from the processor. This value is read into the VID4 Status Register. In analog 12 VIN mode, it has an on-chip voltage attenuator. In VID4 mode, it has an on-chip $300 \mathrm{k} \Omega$ pull-up resistor. |
| 12 | $5 \mathrm{~V}_{\text {IN }}$ | Analog Input. Monitors 5 V supply. |
| 13 | $3.3 \mathrm{~V}_{\mathrm{IN}}$ | Analog Input. Monitors 3.3 V supply. |
| 14 | $2.5 \mathrm{~V}_{\text {IN }}$ | Analog Input. Monitors 2.5 V supply. |
| 15 | $\mathrm{V}_{\text {CCPIN }}$ | Analog Input. Monitors processor core voltage ( 0 V to 3.0 V ). |
| 16 | ADD/RST/INT/NTO | Programmable Digital I/O. The lowest order programmable bit of the SMBus Address, sampled on SMB activity as a three-state input. Can also be configured to give a minimum 20 ms low reset output pulse. Alternatively, it can be programmed as an interrupt output for temperature/voltage interrupts. Functions as the output of the NAND tree in NAND tree test mode. |

## Table 4. ELECTRICAL CHARACTERISTICS

( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}, \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {MIN }}$ to $\mathrm{V}_{\text {MAX }}$, unless otherwise noted)

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| POWER SUPPLY |  |  |  |  |  |
| Supply Voltage, $\mathrm{V}_{\text {CC }}$ (Note 1) |  | 3.0 | 3.3 | 5.5 | V |
| Supply Current, ICC (Note 2) | Interface Inactive, ADC Active Standby Mode | - | $\begin{aligned} & 1.4 \\ & 32 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 500 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mu \mathrm{~A} \end{aligned}$ |

## TEMPERATURE-TO-DIGITAL CONVERTER

| Internal Sensor Accuracy |  | - | - | $\pm 3$ | ${ }^{\circ} \mathrm{C}$ |
| :--- | :--- | :--- | :--- | :---: | :---: |
| Resolution |  | - | 1 | - | ${ }^{\circ} \mathrm{C}$ |
| External Diode Sensor Accuracy | $60^{\circ} \mathrm{C}<\mathrm{T}_{\mathrm{A}}<100^{\circ} \mathrm{C} ; \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$ | - | - | $\pm 5$ | ${ }^{\circ} \mathrm{C}$ |
|  |  | - | - | $\pm 3$ |  |
| Resolution |  | - | 1 | - | ${ }^{\circ} \mathrm{C}$ |
| Remote Sensor Source Current | High Level <br>  <br>  Low Level | - | 180 | - | $\mu \mathrm{A}$ |

## ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)

| Total Unadjusted Error, TUE (Note 3) |  | - | - | $\pm 2$ | $\%$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Differential Nonlinearity, DNL |  | - | - | $\pm 1$ | LSB |
| Power Supply Sensitivity |  | - | $\pm 1$ | - | $\% / \mathrm{V}$ |
| Conversion Time (Analog Input or Internal <br> Temperature) (Note 4) |  | - | 11.6 | - | ms |
| Conversion Time (External Temperature) (Note 4) |  | - | 34.8 | - | ms |
| Input Resistance (2.5 V, 3.3 V, 5 V, 12 V, VCCPIN) |  | 80 | 140 | 250 | $\mathrm{k} \Omega$ |

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Table 4. ELECTRICAL CHARACTERISTICS (continued)
( $\mathrm{T}_{\mathrm{A}}=\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}, \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\text {MIN }}$ to $\mathrm{V}_{\text {MAX }}$, unless otherwise noted)

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OPEN-DRAIN DIGITAL OUTPUTS (ADD, $\overline{\text { RST, }}$ INT, NTO) |  |  |  |  |  |
| Output Low Voltage, $\mathrm{V}_{\text {OL }}$ | $\mathrm{I}_{\text {OUT }}=-6.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=3 \mathrm{~V}$ | - | - | 0.4 | V |
| High Level Output Current, $\mathrm{IOH}^{\text {O }}$ | $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {CC }}, \mathrm{V}_{\text {CC }}=3 \mathrm{~V}$ | - | 0.1 | 1.0 | $\mu \mathrm{A}$ |
| RST Pulsewidth | $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {CC }}, \mathrm{V}_{\text {CC }}=3 \mathrm{~V}$ | - | 20 | 45 | ms |

OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)

| Output Low Voltage, $\mathrm{V}_{\mathrm{OL}}$ | $\mathrm{I}_{\mathrm{OUT}}=-6.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=3 \mathrm{~V}$ | - | - | 0.4 | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| High Level Output Leakage Current, $\mathrm{I}_{\mathrm{OH}}$ | $\mathrm{V}_{\mathrm{OUT}}=\mathrm{V}_{\mathrm{CC}}$ | - | 0.1 | 1.0 | $\mu \mathrm{~A}$ |

SERIAL BUS DIGITAL INPUTS (SCL, SDA)

| Input High Voltage, $\mathrm{V}_{\mathrm{IH}}$ |  | 2.1 | - | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Voltage, $\mathrm{V}_{\mathrm{IL}}$ |  | - | - | 0.8 | V |
| Hysteresis |  | - | 500 | - | mV |

DIGITAL INPUT LOGIC LEVELS (ADD, VIDO-VID4, NTI) (Note 5)

| VID0-VID3 Input Resistance | ADM1025 Only | - | 100 | - | V |
| :--- | :--- | :---: | :---: | :---: | :---: |
| VID4 Input Resistance | ADM1025 <br>  <br>  <br> ADM1025A |  | - | 300 | - |

## DIGITAL INPUT LEAKAGE CURRENT

| Input High Current, $\mathrm{I}_{\mathrm{IH}}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}$ | -1.0 | - | - | $\mu \mathrm{A}$ |
| :--- | :--- | :---: | :---: | :---: | :---: |
| Input Low Current, $\mathrm{I}_{\mathrm{IL}}$ | $\mathrm{V}_{\mathrm{IN}}=0$ | - | - | 1.0 | $\mu \mathrm{~A}$ |
| Input Capacitance, $\mathrm{C}_{\mathrm{IN}}$ |  | - | 5 | - | pF |
| Conversion Cycle Time |  | - | 637 | - | ms |

SERIAL BUS TIMING

| Clock Frequency, f fclk | See Figure 2 for All Parameters. | - | - | 400 | kHz |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Glitch Immunity, tsw |  | - | 50 | - | ns |
| Bus Free Time, ${ }_{\text {t }}$ BUF |  | 1.3 | - | - | $\mu \mathrm{s}$ |
| Start Setup Time, t $^{\text {S }}$; STA |  | 600 | - | - | ns |
| Start Hold Time, thD; STA |  | 600 | - | - | ns |
| Stop Condition Setup Time, tsu; sto |  | 600 | - | - | ns |
| SCL Low Time, t Low |  | 1.3 | - | - | $\mu \mathrm{s}$ |
| SCL High Time, $\mathrm{t}_{\text {HIGH }}$ |  | 0.6 | - | - | $\mu \mathrm{S}$ |
| SCL, SDA Rise Time, $\mathrm{t}_{\mathrm{R}}$ |  | - | - | 300 | ns |
| SCL, SDA Fall Time, $\mathrm{t}_{\mathrm{F}}$ |  | - | - | 300 | ns |
| Data Setup Time, t $_{\text {SU; }}$ DAT |  | 100 | - | - | ns |
| Data Hold Time, thD; DAT |  | 300 | - | - | ns |

1. All voltages are measured with respect to GND, unless otherwise specified.
2. Typicals are at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and represent the most likely parametric norm. Shutdown current typ is measured with $\mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V}$.
3. TUE (Total Unadjusted Error) includes Offset, Gain, and Linearity errors of the ADC, multiplexer, and on-chip input attenuators, including an external series input protection resistor value between zero and $1 \mathrm{k} \Omega$.
4. Total monitoring cycle time is nominally 114.4 ms . Monitoring Cycle consists of 6 Voltage +1 Internal Temperature +1 External Temperature readings.
5. ADD is a three-state input that may be pulled high, low or left open-circuit.
6. Timing specifications are tested at logic levels of $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$ for a falling edge and $\mathrm{V}_{\mathrm{IH}}=2.1 \mathrm{~V}$ for a rising edge. NOTE: Specifications subject to change without notice.


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS


Figure 3. Temperature Error vs. PC Board Track Resistance


Figure 5. Temperature Error vs. Common-mode Noise Frequency


Figure 4. Temperature Error vs. Power Supply Noise Frequency


Figure 6. Pentium II ${ }^{\circledR}$ Temperature Measurement vs. ADM1025/ADM1025A Reading

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)


Figure 7. Temperature Error vs. Capacitance between D+ and D-


Figure 8. Temperature Error vs. Differential-mode Noise Frequency


Figure 9. Standby Current vs. Temperature

## General Description

The ADM1025/ADM1025A is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial System Management Bus. The serial bus controller has a hardwired address line for device selection (Pin 16), a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions of the ADM1025/ADM1025A are performed over the serial bus.

## Measurement Inputs

The device has six measurement inputs, five for voltage and one for temperature. It can also measure its own supply voltage and can measure ambient temperature with its on-chip temperature sensor.

Pins 11 through 15 are analog inputs with on-chip attenuators configured to monitor $12 \mathrm{~V}, 5 \mathrm{~V}, 3.3 \mathrm{~V}, 2.5 \mathrm{~V}$, and the processor core voltage, respectively. Pin 11 may alternatively be programmed as a digital input for Bit 4 of the processor voltage ID code.

Power is supplied to the chip via Pin 4, and the system also monitors the voltage on this pin.

Remote temperature sensing is provided by the $\mathrm{D}+$ and $\mathrm{D}-$ inputs, to which a diode-connected, external temperature-sensing transistor may be connected.

An on-chip band gap temperature sensor monitors system ambient temperature.

## Sequential Measurement

When the ADM1025/ADM1025A monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensors. Measured values from these inputs are stored in Value Registers. These can be read out over the serial bus or can be compared with programmed limits stored in the Limit Registers. The results of out-of-limit comparisons are stored in the Status Registers, which can be read over the serial bus to flag out of limit conditions.

## Processor Voltage ID

Five digital inputs (VID4 to VID0 - Pins 5 to 8 and 11) read the processor voltage ID code and store it in the VID registers, from which it can be read out by the management system over the serial bus. If Pin 11 is configured as a 12 V analog input (powerup default), the VID4 bit in the VID4 register will default to 0 .

The VID pins have internal $100 \mathrm{k} \Omega$ pull-up resistors (ADM1025 only).

## ADD/RST/INT/NTO

Pin 16 is a programmable digital I/O pin. After power-up, at the first sign of SMBus activity, it is sampled to set the lowest two bits of the serial bus address. During board-level, NAND tree connectivity testing, this pin functions as the output of the NAND tree. During normal operation, Pin 16 may be programmed as a reset output to provide a low going 20 ms reset pulse when enabled, or it may be programmed
as an interrupt output for out-of-limit temperature and/or voltage events. These functions are described in more detail later.

## Internal Register of the ADM1025/ADM1025A

A brief description of the ADM1025/ADM1025A's principal internal registers is given below. More detailed information on the function of each register is given in Table 9 to Table 19.
Configuration Register: Provides control and configuration.
Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1025/ADM1025A, the first byte of data is always a register address, which is written to the Address Pointer Register.
Status Registers: Two registers to provide status of each limit comparison.
VID Registers: The status of the VID0 to VID4 pins of the processor can read from these registers.
Value and Limit Registers: The results of analog voltage inputs and temperature measurements are stored in these registers, along with their limit values.
Offset Register: Allows either an internal or external temperature channel reading to be offset by a twos complement value written to this register.

## Serial Bus Interface

Control of the ADM1025/ADM1025A is carried out via the serial bus. The ADM1025/ADM1025A is connected to this bus as a slave device, under the control of a master device or master controller.
The ADM1025/ADM1025A has a 7-bit serial bus address.

When the device is powered up, it will do so with a default serial bus address. The five MSBs of the address are set to 01011; the two LSBs are determined by the logical states of Pin 16 at power-up. This is a three-state input that can be grounded, connected to $\mathrm{V}_{\mathrm{CC}}$, or left open-circuit to give three different addresses:

Table 5. ADDRESS SELECTION

| ADD Pin | A1 | A0 |
| :---: | :---: | :---: |
| GND | 0 | 0 |
| No Connect | 1 | 0 |
| $V_{C C}$ | 0 | 1 |

If ADD is left open-circuit, the default address will be 0101110. ADD is sampled only after power-up, so any changes made will have no effect, unless power is cycled.

The facility to make hardwired changes to A1 and A0 allows the user to avoid conflicts with other devices sharing the same serial bus if, for example, more than one ADM1025/ADM1025A is used in a system. However, as previously mentioned, the ADD pin may also function as a
reset output or interrupt output. Use of these functions may restrict the addresses that can be set. See the sections on $\overline{\mathrm{RST}}$ and $\overline{\mathrm{INT}}$ for further information.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an $R / \bar{W}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.
The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the $R / \bar{W}$ bit is a 0 , the master will write to the slave device. If the $R / \bar{W}$ bit is a 1 , the master will read from the slave device.
2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, STOP conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the Acknowledge Bit by pulling the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1025/ADM1025A, write operations contain either one or two bytes, and read operations contain one byte and perform the following functions.

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed; data can then be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the Address Pointer Register.

This is illustrated in Figure 10. The device address is sent over the bus followed by $\mathrm{R} / \overline{\mathrm{W}}$ set to 0 . This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.


Figure 10. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register


Figure 11. Writing to the Address Pointer Register Only


Figure 12. Reading Data from a Previously Selected Register

When reading data from a register there are two possibilities:

1. If the ADM1025/ADM1025A's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1025/ADM1025A as before, but only the data byte containing the register address is sent, since data should not be written to the register. This is shown in Figure 11.
A read operation is then performed consisting of the serial bus address, $\mathrm{R} / \mathrm{W}$ bit set to 1 , followed by the data byte read from the data register. This is shown in Figure 12.
2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so Figure 11 can be omitted.

## NOTES:

1. Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register because the first data byte of a write is always written to the Address Pointer Register.
2. In Figure 10 to Figure 12, the serial bus address is shown as the default value 01011 (A1)(A0), where A1 and A0 are set by the three-state ADD pin.
3. In addition to supporting the Send Byte and Receive Byte protocols, the ADM1025/ADM1025A also supports the Read Byte protocol (see System Management Bus specifications Rev. 1.1 for more information).
4. If Reset or interrupt functionality is required, the address pin cannot be strapped to GND, since this would keep the ADD/RST/INT/NTO pin permanently low.


Figure 13. Structure of Analog Inputs

## Measurement Inputs

The ADM1025/ADM1025A has six external measurement inputs, five for voltage and one (two pins) for temperature. Internal measurements are also carried out on $\mathrm{V}_{\mathrm{CC}}$ and the on-chip temperature sensor.

## A/D Converter

These inputs are multiplexed into the on-chip, successive-approximation, analog-to-digital converter. This has a resolution of eight bits. The basic input range is 0 V to 2.5 V , but the inputs have built-in attenuators to allow measurement of $2.5 \mathrm{~V}, 3.3 \mathrm{~V}, 5 \mathrm{~V}, 12 \mathrm{~V}$, and the processor core voltage $\mathrm{V}_{\mathrm{CCP}}$ without any external components. To

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allow for the tolerance of these supply voltages, the A/D converter produces an output of . full scale (decimal 192) for the nominal input voltage and so has adequate headroom to cope with overvoltages. Table 6 shows the input ranges of the analog inputs and output codes of the $\mathrm{A} / \mathrm{D}$ converter.

When the ADC is running, it samples and converts an input every 11.6 ms , except for the external temperature (D+ and $\mathrm{D}-$ ) input. This has special input signal conditioning and
is averaged over 16 conversions to reduce noise; a measurement on this input takes nominally 34.8 ms .

## Input Circuits

The internal structure for the analog inputs is shown in Figure 13. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first order low-pass filter that gives the input immunity to high frequency noise.

Table 6. A/D OUTPUT CODE VS. $\mathrm{V}_{\mathrm{IN}}$

| Input Voltage |  |  |  |  | A/D Output |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 12 Vin | 5 Vin | Vcc/3.3 Vin | 2.5 Vin | Vccpin | Decimal | Binary |
| <0.062 | <0.026 | <0.0172 | <0.013 | <0.012 | 0 | 00000000 |
| 0.062-0.125 | 0.026-0.052 | 0.017-0.034 | 0.013-0.026 | 0.012-0.023 | 1 | 00000001 |
| 0.125-0.188 | 0.052-0.078 | 0.034-0.052 | 0.026-0.039 | 0.023-0.035 | 2 | 00000010 |
| 0.188-0.250 | 0.078-0.104 | 0.052-0.069 | 0.039-0.052 | 0.035-0.047 | 3 | 00000011 |
| 0.250-0.313 | 0.104-0.130 | 0.069-0.086 | 0.052-0.065 | 0.047-0.058 | 4 | 00000100 |
| 0.313-0.375 | 0.130-0.156 | 0.086-0.103 | 0.065-0.078 | 0.058-0.070 | 5 | 00000101 |
| 0.375-0.438 | 0.156-0.182 | 0.103-0.120 | 0.078-0.091 | 0.070-0.082 | 6 | 00000110 |
| 0.438-0.500 | 0.182-0.208 | 0.120-0.138 | 0.091-0.104 | 0.082-0.093 | 7 | 00000111 |
| 0.500-0.563 | 0.208-0.234 | 0.138-0.155 | 0.104-0.117 | 0.093-0.105 | 8 | 00001000 |
| $\ldots$ |  |  |  |  |  |  |
| 4.000-4.063 | 1.666-1.692 | 1.100-1.117 | 0.833-0.846 | 0.749-0.761 | 64 (1/4 Scale) | 01000000 |
| ... |  |  |  |  |  |  |
| 8.000-8.063 | 3.330-3.560 | 2.200-2.217 | 1.667-1.680 | 1.499-1.511 | 128 (1/2 Scale) | 10000000 |
| $\ldots$ |  |  |  |  |  |  |
| 12.000-12.063 | 5.000-5.026 | 3.300-3.317 | 2.500-2.513 | 2.249-2.261 | 192 (3/4 Scale) | 11000000 |
| $\ldots$ |  |  |  |  |  |  |
| 15.312-15.375 | 6.380-6.406 | 4.210-4.230 | 3.190-3.203 | 2.869-2.881 | 245 | 11110101 |
| 15.375-15.437 | 6.406-6.432 | 4.230-4.245 | 3.203-3.216 | 2.881-2.893 | 246 | 11110110 |
| 15.437-15.500 | 6.432-6.458 | 4.245-4.263 | 3.216-3.229 | 2.893-2.905 | 247 | 11110111 |
| 15.500-15.563 | 6.458-6.484 | 4.263-4.280 | 3.229-3.242 | 2.905-2.916 | 248 | 11111000 |
| 15.625-15.625 | 6.484-6.510 | 4.280-4.300 | 3.242-3.255 | 2.916-2.928 | 249 | 11111001 |
| 15.625-15.688 | 6.510-6.536 | 4.300-4.314 | 3.255-3.268 | 2.928-2.940 | 250 | 11111010 |
| 15.688-15.750 | 6.536-6.562 | 4.314-4.330 | 3.268-3.281 | 2.940-2.951 | 251 | 11111011 |
| 15.750-15.812 | 6.562-6.588 | 4.331-4.348 | 3.281-3.294 | 2.951-2.964 | 252 | 11111100 |
| 15.812-15.875 | 6.588-6.615 | 4.348-4.366 | 3.294-3.307 | 2.964-2.975 | 253 | 11111101 |
| 15.875-15.938 | 6.615-6.640 | 4.366-4.383 | 3.307-3.320 | 2.975-2.987 | 254 | 11111110 |
| >15.938 | >6.640 | >4.383 | >3.320 | >2.988 | 255 | 11111111 |

## Temperature Measurement System

## Internal Temperature Measurement

The ADM1025/ADM1025A contains an on-chip band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the Local Temperature Value Register (Address 27h). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 7. Theoretically, the temperature sensor and ADC can measure temperatures from $-128^{\circ} \mathrm{C}$ to $+127^{\circ} \mathrm{C}$
with a resolution of $1^{\circ} \mathrm{C}$, although temperatures below $0^{\circ} \mathrm{C}$ and above $+100^{\circ} \mathrm{C}$ are outside the operating temperature range of the device.

## External Temperature Measurement

The ADM1025/ADM1025A can measure temperature using an external diode sensor or diode-connected transistor connected to Pins 9 and 10.
The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about $-2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$. Unfortunately,

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the absolute value of $\mathrm{V}_{\mathrm{BE}}$, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production.

The technique used in the ADM1025/ADM1025A is to measure the change in $\mathrm{V}_{\text {BE }}$ when the device is operated at two different currents.

This is given by:

$$
\begin{equation*}
\Delta \mathrm{V}_{\mathrm{BE}}=\mathrm{KT} / \mathrm{q} \times \ln (\mathrm{N}) \tag{eq.1}
\end{equation*}
$$

where:
$K$ is Boltzmann's constant
$q$ is charge on the carrier
$T$ is absolute temperature in Kelvins
$N$ is ratio of the two currents
Figure 14 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D - input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D - input and the base to the $\mathrm{D}+$ input.

Bit 6 of Status Register 2 (42h) is set if a remote diode fault is detected. The ADM1025/ADM1025A detects shorts from D+ to GND or supply, as well as shorts/opens between D+/D-.

Table 7. TEMPERATURE DATA FORMAT

| Temperature | Digital Output |
| :---: | :---: |
| $-128^{\circ} \mathrm{C}$ | 10000000 |
| $-125^{\circ} \mathrm{C}$ | 10000011 |
| $-100^{\circ} \mathrm{C}$ | 10011100 |
| $-75^{\circ} \mathrm{C}$ | 10110101 |
| $-50^{\circ} \mathrm{C}$ | 11001110 |
| $-25^{\circ} \mathrm{C}$ | 11100111 |
| $0^{\circ} \mathrm{C}$ | 00000000 |
| $+10^{\circ} \mathrm{C}$ | 00001010 |
| $+25^{\circ} \mathrm{C}$ | 00011001 |
| $+50^{\circ} \mathrm{C}$ | 00110010 |
| $+75^{\circ} \mathrm{C}$ | 01001011 |
| $+100^{\circ} \mathrm{C}$ | 01100100 |
| $+125^{\circ} \mathrm{C}$ | 01111101 |
| $+127^{\circ} \mathrm{C}$ | 01111111 |



Figure 14. Signal Conditioning for External Diode Temperature Sensors

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D - input.

If the sensor is used in a very noisy environment, a capacitor of value up to 1 nF may be placed between the $\mathrm{D}+$ and D - inputs to filter the noise.

To measure $\Delta \mathrm{V}_{\mathrm{BE}}$, the sensor is switched between operating currents of I and $\mathrm{N} \times \mathrm{I}$. The resulting waveform is
passed through a 65 kHz low-pass filter to remove noise, then to a chopperstabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to $\Delta \mathrm{V}_{\mathrm{BE}}$. This voltage is measured by the ADC to give a temperature output in 8 -bit twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement takes nominally 34.8 ms .

## Layout Considerations

Digital boards can be electrically noisy environments and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1025/ADM1025A as close as possible to the remote sensing diode. Provided that the worst noise sources, such as clock generators, data/address buses, and CRTs, are avoided, this distance can be four to eight inches.
2. Route the $\mathrm{D}+$ and $\mathrm{D}-$ tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.


Figure 15. Arrangement of Signal Tracks
4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the $\mathrm{D}+$ and D - path and at the same temperature.
Thermocouple effects should not be a major problem as $1^{\circ} \mathrm{C}$ corresponds to about $240 \mu \mathrm{~V}$, and thermocouple voltages are about $3 \mu \mathrm{~V} /{ }^{\circ} \mathrm{C}$ of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than $200 \mu \mathrm{~V}$.
5. Place $0.1 \mu \mathrm{~F}$ bypass and 1 nF input filter capacitors close to the ADM1025/ADM1025A.
6. If the distance to the remote sensor is more than eight inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet) use shielded twisted pair, such as Belden \#8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADM1025/ADM1025A. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. $1 \Omega$ series resistance introduces about $0.5^{\circ} \mathrm{C}$ error.

## Limit Values

High and low limit values for each measurement channel are stored in the appropriate limit registers. As each channel is measured, the measured value is stored and compared with the programmed limit.

## Status Registers

The results of limit comparisons are stored in Status Registers 1 and 2. The Status Register bit for a particular measurement channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding Status Register bit will be cleared to " 0 ." If the measurement is out of limits, the corresponding status register bit will be set to "1."

The state of the various measurement channels may be polled by reading the Status Registers over the serial bus. Reading the Status Registers does not affect their contents. Out-of-limit temperature/voltage events may also be used to generate an interrupt so that remedial action, such as turning on a cooling fan, may be taken immediately. This is described in the section on $\overline{\mathrm{RST}}$ and $\overline{\mathrm{INT}}$.

## Monitoring Cycle Time

The monitoring cycle begins when a 1 is written to the Start Bit (Bit 0) of the Configuration Register. The ADC measures each analog input in turn and as each measurement is completed the result is automatically stored in the appropriate value register. This "round-robin" monitoring cycle continues until it is disabled by writing a 0 to Bit 0 of the Configuration Register.

As the ADC will normally be left to free-run in this manner, the time taken to monitor all the analog inputs will normally not be of interest, since the most recently measured value of any input can be read out at any time.

## Input Safety

Scaling of the analog inputs is performed on-chip, so external attenuators are normally not required. However, since the power supply voltages will appear directly at the pins, it is advisable to add small external resistors in series with the supply traces to the chip to prevent damaging the traces or power supplies should an accidental short such as a probe connect two power supplies together.

As the resistors will form part of the input attenuators, they will affect the accuracy of the analog measurement if their value is too high. The analog input channels are calibrated assuming an external series resistor of $500 \Omega$, and the accuracy will remain within specification for any value from zero to $1 \mathrm{k} \Omega$, so a standard $510 \Omega$ resistor is suitable.

The worst such accident would be connecting 0 V to 12 V - a total of 12 V difference. With the series resistors, this would draw a maximum current of approximately 12 mA .

## Layout and Grounding

Analog inputs will provide best accuracy when referred to a clean ground. A separate, low impedance ground plane for analog ground, which provides a ground point for the voltage dividers and analog components, will provide best performance but is not mandatory.

The power supply bypass, the parallel combination of $10 \mu \mathrm{~F}$ (electrolytic or tantalum) and $0.1 \mu \mathrm{~F}$ (ceramic) bypass capacitors connected between Pin 9 and ground, should also be located as close as possible to the ADM1025/ADM1025A.

## RST/INT Output

As previously mentioned, Pin 16 is a multifunction pin. Its state after power-on is latched to set the lowest two bits of the serial bus address. During NAND tree board-level connectivity testing, it functions as the output of the NAND tree. It may also be used as a reset output, or as an interrupt output for out-of-limit temperature/voltage events.

Pin 16 is programmed as a reset output by clearing Bit 0 of the Test Register and setting Bit 7 of the VID Register. A low going, 20 ms , reset output pulse can then be generated by setting Bit 4 of the Configuration Register.

If Bit 7 of the VID Register is cleared, Pin 16 can be programmed as an interrupt output for out-of-limit temperature/voltage events ( $\overline{\mathrm{INT}})$. Desired interrupt operation is achieved by changing the values of Bits 1 and 0 of the Test Register as shown in Table 8. Note, however, that Bits 2 to 7 of the Test Register must be zeros (not don't cares). If, for example, $\overline{\text { INT }}$ is programmed for thermal and voltage interrupts, then if any temperature or voltage measurement goes outside its respective high or low limit, the $\overline{\mathrm{INT}}$ output will go low. It will remain low until Status

Register 1 is read, when it will be cleared. If the temperature or voltage remains out of limit, $\overline{\mathrm{INT}}$ will be reasserted on the next monitoring cycle. $\overline{\mathrm{INT}}$ can also be cleared by issuing an Alert Response Address Call.

Table 8. CONTROLLING THE OPERATION OF INT

| Test Register |  |  |
| :---: | :---: | :--- |
| Bit $\mathbf{1}$ | Bit 0 |  |
| 0 | 0 | Function |
| 0 | 1 | Therrupts Disabled |
| 1 | 0 | Voltage Interrupt Only Interrupt Only |
| 1 | 1 | Voltage and Thermal Interrupts |

Note that Bit 7 of VID register should be zero, and that Bits 2 to 7 of Test Register must be zeros.
When Pin 16 is used as a $\overline{\mathrm{RST}}$ or $\overline{\mathrm{INT}}$ output, it is open-drain and requires an external pull-up resistor. This will restrict the address function on Pin 16 to being high at power-up. If the $\overline{\mathrm{RST}}$ or $\overline{\mathrm{INT}}$ function is required and two ADM1025/ADM1025As are to be used on the same serial bus, A1/A0 can be set to 10 by using a high value pull-up on Pin 16 ( $100 \mathrm{k} \Omega$ or greater). This will not override the "floating" condition of ADD during power-up.
Note, however, that the RST/INT outputs of two or more devices cannot be wire-OR'd, since the devices would then have the same address. If the $\overline{\mathrm{RST}} / \overline{\mathrm{INT}}$ outputs need to be connected to a common interrupt line, they can be OR'd together using the circuit of Figure 16.
If the $\overline{\mathrm{RST}}$ or $\overline{\mathrm{INT}}$ functionality is not required, a third address may be used by setting A1/A0 to 00 by using a $1 \mathrm{k} \Omega$ pull-down resistor on Pin 16. Note that this address should not be used if $\overline{\mathrm{RST}}$ or $\overline{\mathrm{INT}}$ is required, since using this address will cause the device to appear to be generating resets or interrupts, since Pin 16 will be permanently tied low.


Figure 16. Using Two ADM1025/ADM1025As on the Same Bus with a Common Interrupt

## Generating an SMBALERT

The $\overline{\mathrm{INT}}$ output can be used as an interrupt output or can be used as an SMBALERT. One or more $\overline{\text { INT }}$ outputs can be connected to a common SMBALERT line connected to the master. If a device's $\overline{\mathrm{INT}}$ line goes low, the following procedure occurs:

1. SMBALERT is pulled low.
2. Master initiates a read operation and sends the Alert Response Address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\mathrm{INT}}$ output is low responds to the Alert Response Address, and the master reads its device address. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's $\overline{\mathrm{INT}}$ output is low, the one with the lowest device address will have priority, in accordance with normal SMBus arbitration.
5. Once the ADM1025/ADM1025A has responded to the Alert Response Address, it will reset its $\overline{\text { INT }}$ output; however, if the error condition that caused the interrupt persists, $\overline{\mathrm{INT}}$ will be reasserted on the next monitoring cycle.

## NAND Tree Tests

A NAND tree is provided in the ADM1025/ADM1025A for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND Test Mode by powering up with Pin 9 (D-/NTI) held high. This pin is automatically sampled after power-up, and if it is connected high, the NAND test mode is invoked.

In NAND test mode, all digital inputs may be tested as illustrated below. ADD/RST/INT/NTO will become the NAND test output pin.

To perform a NAND tree test, all pins are initially driven low. The test vectors set all inputs low, then one-by-one toggle them high (keeping them high). Exercising the test circuit with this "walking one" pattern, starting with the input closest to the output of the tree, cycling toward the farthest, causes the output of the tree to toggle with each input change. Allow for a typical propagation delay of 500 ns . The structure of the NAND tree is shown in Figure 17.


Figure 17. NAND Tree

NOTE: If any of the inputs shown in Figure 17 are unused, they should not be connected directly to ground but via a resistor such as $10 \mathrm{k} \Omega$. This will allow the ATE to drive every input high so that the NAND tree test can be properly carried out. Refer to Table 20 for Test Vectors.

## Using the ADM1025/ADM1025A

## Power-on Reset

When power is first applied, the ADM1025/ADM1025A performs a "power-on reset" on several of its registers. Registers whose power-on values are not shown have power-on conditions that are indeterminate. Value and limit registers are reset to 00 h on power-up. The ADC is inactive. In most applications, usually the first action after power-on would be to write limits into the Limit Registers.

Power-on reset clears or initializes the following registers (the initialized values are shown in Table 10):

- Configuration Register
- Status Registers \#1 and \#2
- VID0-3 Register
- VID4 Register
- Test Register


## Initialization

Configuration Register Initialization performs a similar, but not identical, function to power-on reset.

Configuration Register Initialization is accomplished by setting Bit 7 of the Configuration Register high. This bit automatically clears after being set.

## Using the Configuration Register

Control of the ADM1025/ADM1025A is provided through the configuration register. The Configuration Register is used to start and stop the ADM1025/ADM1025A, program the operating modes of Pins 11 and 16, and provide the initialization function described above.

Bit 0 of the Configuration Register controls the monitoring loop of the ADM1025/ADM1025A. Setting Bit 0 low stops the monitoring loop and puts the ADM1025/ADM1025A into a low power mode thereby reducing power consumption. Serial bus communication is still possible with any register in the ADM1025/ADM1025A while in low power mode. Setting Bit 0 high starts the monitoring loop.

Bit 4 of the Configuration Register causes a low going 20 ms (typ) pulse at the $\overline{\mathrm{RST}}$ pin (Pin 16) when set. This bit is self-clearing.

Bit 5 of the Configuration Register selects the operating mode of Pin 11 between the default of 12 V analog input (Bit $5=0$ ) and VID4 (Bit $5=1$ ).

Bit 7 of the Configuration Register is used to start a Configuration Register Initialization when it is set to 1 .

## Using the Offset Register

This register contains a twos complement value that is added (or subtracted if the number is negative) to either the internal or external temperature reading. Note that the default value in the offset register is zero, so zero is always added to the temperature reading. The offset register is configured for the external temperature channel by default. It may be switched to the internal channel by setting Bit 0 of

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the Test Register to 1, setting Bit 6 of the VID Register to 1, and clearing Bit 7 of the VID Register.

## Starting Conversion

The monitoring function of the ADM1025/ADM1025A is started by writing to the Configuration Register and setting Start (Bit 0) high. Limit values should be written into the Limit Registers before starting the ADC to avoid spurious out-of-limit conditions. The time taken to complete the analog measurements depends on how they are configured, as described elsewhere. Once the measurements have been completed, the results can be read from the Value Registers at any time.

## Reduced Power and Shutdown Mode

The ADM1025/ADM1025A can be placed in a low power mode by setting Bit 0 of the Configuration Register to 0 . This disables the internal ADC. Full shutdown mode may then be achieved by setting Bit 7 of the VID Register to 1 and Bit 0 of the Test Register to 1. This turns off power to all
analog circuits and stops the monitoring cycle, if running, but it does not affect the condition of any of the registers. The device will return to its previous state when these bits are reset to zero.

## 5 V Operation

The ADM1025/ADM1025A may be operated with $\mathrm{V}_{\mathrm{CC}}$ connected to any supply voltage between 3.0 V and 5.5 V , but it should be noted that the device has been optimized for 3.3 V operation. In particular, the internal voltage divider used to measure the supply voltage is optimized for 3.3 V . Powering the device from 5 V will cause the VCC Reading Register (Register 25h) to overrange. In this case, the 5 V measurement should be read from the 5 V Reading Register (Register 23h), instead of the $\mathrm{V}_{\mathrm{CC}}$ Reading Register. Note also that when the $12 \mathrm{~V}_{\mathrm{IN}} / \mathrm{VID} 4$ pin is programmed to read VID4, due to its internal voltage divider, it will only read $\mathrm{V}_{\mathrm{IH}}=2.1 \mathrm{~V}$ on the $12 \mathrm{~V}_{\mathrm{IN}} / \mathrm{VID} 4$ pin as logic high if the device is being powered from the 3.3 V supply.

## REGISTERS

Table 9. ADDRESS POINTER REGISTER

| Bit | Name | R/W | Description |
| :---: | :---: | :---: | :---: |
| $7-0$ | Address Pointer | Write | Address of ADM1025/ADM1025A Registers. See the tables below for detail. |

Table 10. LIST OF REGISTERS

| Register Name | Address A7-A0 in Hex | Power On Value of Registers: <7:0> |
| :---: | :---: | :--- |
| Configuration Register | 40 h | 00001000 |
| Status Register 1 | 41 h | 00000000 |
| Status Register 2 | 42 h | 00000000 |
| VID Register | 47 h | $<7: 4>=0000,<3: 0>=$ VID3-VID0 |
| VID4 Register | 49 h | $<0>=$ VID4; Default $=1000000$ (VID4) |
| Value and Limit Registers | $15-3 \mathrm{Dh}$ |  |
| Company ID | 3Eh | 01000001 |
| Stepping | 3Fh | 0010 (Bits 3:0 Version Number) |

Table 11. REGISTER 40h - CONFIGURATION REGISTER

| Bit | Name | R/W | Description |
| :---: | :---: | :---: | :--- |
| 0 | START | Read/Write | Logic 1 enables start-up of monitor ASIC, and Logic 0 places the ASIC in <br> standby mode. At start-up, limit checking functions and scanning begins. <br> Note, all HIGH and LOW LIMITS should be set into the <br> ADM1025/ADM1025A prior to turning on this bit. (Power-up Default $=0$. .) |
| 1 | Reserved | Read | - |
| 2 | Reserved | Read | - |
| 3 | Reserved | Read | - |
| 4 | RESET | Read/Write | Setting this bit generates a minimum 20 ms low pulse on Pin 16 if the <br> function is enabled. |
| 5 | $+12 /$ /ID4 Select | Read/Write | Selects whether Pin 11 acts as a 12 V analog input monitoring pin, or as a <br> VID[4] input. This pin defaults to the 12 V analog input. (Default = 0.) |
| 6 | Reserved | Read | - |
| 7 | Initialization | Read/Write | Logic 1 restores power-up default values to the Configuration Register and <br> Status Registers. This bit automatically clears itself and the power-on <br> default is zero. |

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Table 12. REGISTER 41h - STATUS REGISTER 1 (POWER-ON DEFAULT <7:0> = 00h)

| Bit | Name | R/W |  |
| :---: | :---: | :---: | :--- |
| 0 | $+2.5 \mathrm{~V} \_$Error | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 1 | V $_{\text {CCP_Error }}$ | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 2 | $+3.3 \mathrm{~V} \_$Error | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 3 | +5 V _Error | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 4 | Local Temp Error | Read-only | A 1 indicates a high or a low temperature limit has been exceeded. |
| 5 | Remote Temp Error | Read-only | A 1 indicates a high or low Remote temperature limit has been exceeded. |
| 6 | Reserved | - | - |
| 7 | Reserved | - | - |

Table 13. REGISTER 42h - STATUS REGISTER 2 (POWER-ON DEFAULT <7:0> = 00h)

| Bit | Name | R/W |  |
| :---: | :---: | :---: | :--- |
| 0 | +12 V Error | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 1 | V Cc_Error | Read-only | A 1 indicates a high or low limit has been exceeded. |
| 2 | Reserved | Read-only | Undefined |
| 3 | Reserved | Read-only | Undefined |
| 4 | Reserved | Read-only | Undefined |
| 5 | Reserved | Read-only | Undefined |
| 6 | Remote Diode Fault | Read-only | A one indicates either a short or open circuited fault on the remote thermal <br> diode inputs. |
| 7 | Reserved | Read-only | Undefined |

Table 14. REGISTER 47h - VID REGISTER (POWER-ON DEFAULT = 0000 (VID [3:0]))

| Bit | Name | R/ $\overline{\mathbf{W}}$ | Description |
| :---: | :---: | :---: | :--- |
| $0-3$ | VID[0:3] | Read-only | The VID[3:0] inputs from Pentium/PRO power supplies to indicate the <br> operating voltage (e.g., 1.3 V to 2.9 V ). |
| $4-5$ | Reserved | Read-only | Undefined |
| 6 | Offset Config | Read/Write | Configures offset register to be used with internal or external channel. If <br> Bit 0 of Test Register $=1$ and Bit 7 of VID Register $=0$, then setting this bit <br> to 1 configures the OOffet Register to the internal temperature channel. <br> Clearing this bit configures the Offset Register to the external temperature <br> channel. (Default $=0$. .) |
| 7 | RST ENABLE | Read/Write | When set to 1, enables the RST output function on Pin 16. This bit defaults <br> to 0 on power-up. (RST Disabled.) |

Table 15. REGISTER 49h - VID4 REGISTER (POWER-ON DEFAULT = 1000000 (VID4))

| Bit | Name | R/W |  |
| :---: | :---: | :---: | :--- |
| 0 | VID4 | Read | VID4 Input (If Selected) (Defaults to 0) |
| $1-7$ | Reserved | Read | - |

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Table 16. REGISTERS 15h-3Dh - VALUE AND LIMIT REGISTERS (Note 1)

| Address | R/W | Description |
| :---: | :---: | :---: |
| 15h | Read/Write | Manufacturers Test Register |
| 1Fh | Read/Write | Offset Register |
| 20h | Read-only | 2.5 V Reading |
| 21h | Read-only | $\mathrm{V}_{\text {CCP }}$ Reading |
| 22h | Read-only | 3.3 V Reading |
| 23h | Read-only | 5 V Reading |
| 24h | Read-only | 12 V Reading |
| 25h | Read-only | $\mathrm{V}_{\mathrm{CC}}$ Reading |
| 26h | Read-only | Remote Diode Temperature Reading |
| 27h | Read-only | Local Temperature Reading |
| 2Bh | Read/Write | 2.5 V High Limit |
| 2Ch | Read/Write | 2.5 V Low Limit |
| 2Dh | Read/Write | $V_{\text {CCP }}$ High Limit |
| 2Eh | Read/Write | $V_{\text {CCP }}$ Low Limit |
| 2Fh | Read/Write | 3.3 V High Limit |
| 30h | Read/Write | 3.3 V Low Limit |
| 31h | Read/Write | 5 V High Limit |
| 32h | Read/Write | 5 V Low Limit |
| 33h | Read/Write | 12 V High Limit |
| 34h | Read/Write | 12 V Low Limit |
| 35h | Read/Write | $\mathrm{V}_{\text {CC }}$ High Limit |
| 36h | Read/Write | $\mathrm{V}_{\mathrm{CC}}$ Low Limit |
| 37h | Read/Write | Remote Temperature High Limit |
| 38h | Read/Write | Remote Temperature Low Limit |
| 39h | Read/Write | Local Temperature High Limit |
| 3Ah | Read/Write | Local Temperature Low Limit |

1. For the high limits of the voltages, the device is doing a greater-than comparison. For the low limits, however, it is doing a less-than or equal comparison.

Table 17. REGISTER 15h - MANUFACTURERS TEST REGISTER

| Bit | Name | R/W |  |
| :---: | :---: | :---: | :--- |
| 0 | - | Read/Write | Used to select RST or INT functions. Refer to RST/INT Output section. |
| 1 | - | Read/Write | Used to select RST or INT functions. Refer to RST/INT Output section. |
| $2-7$ | Reserved | Read/Write | Reserved. Only values written to these bits should be zeros. |

Table 18. REGISTERS 3Eh - COMPANY ID

| Value (Bits 7:0) | R/W | Description |
| :---: | :---: | :--- |
| 01000001 | Read-only | This location contains the company identification number that may be used <br> by software to determine the manufacturer's device. This register is <br> read-only. |

Table 19. REGISTERS 3Fh - STEPPING

| Value (Bits 7:0) | R/W |  |
| :---: | :---: | :--- |
| 0010 [Version] | Read-only | Stepping ID Number and Version |

Table 20. NAND TREE TEST VECTORS

| Vector No. | SDA | SCL | VID0 | VID1 | VID2 | VID3 | ADD/RST/INT/NTO |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 4 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 5 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 21. ORDERING INFORMATION

| Device Order <br> Number* | Temperature <br> Range | Package <br> Type | Package <br> Option | Option | Shipping ${ }^{\dagger}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ADM1025ARQZ | $0^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$ | 16-lead QSOP | RQ-16 | Integrated $100 \mathrm{k} \Omega$ VID Pull-ups | 98/Tube |
| ADM1025ARQZ-REEL | $0^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$ | 16 -lead QSOP | RQ-16 | Integrated $100 \mathrm{k} \Omega$ VID Pull-ups | 2,500 Tape \& Reel <br> (13 Inch) |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Z = RoHS Compliant Part.


NOTES：
1．DIMENSIONING AND TOLERANCING PER ASME Y14．5M， 1994.
．CONTROLLING DIMENSION：MILLIMETERS．
3．DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION．
4．DIMENSION D DOES NOT INCLUDE MOLD FLASH， PROTRUSIONS，OR GATE BURRS．MOLD FLASH， PROTRUSIONS，OR GATE BURRS．MOLD FLASH，
PROTRUSIONS，OR GATE BURRS SHALL NOT EX PROTRUSIONS，OR GATE BURRS SHALL NOT EX－
CEED 0．005 PER SIDE．DIMENSION E1 DOES NOT CEED 0.005 PER SIDE．DIMENSION E1 DOES NOT
INCLUDE INTERLEAD FLASH OR PROTRUSION．IN INCLUDE INTERLEAD FLASH OR PROTRUSION．IN－
TERLEAD FLASH OR PROTRUSION SHALL NOT EX－ TERLEAD FLASH OR PROTRUSION SHALL NOT EX－
CEFD 0.005 PER SIDE．D AND E1 ARE DETERMINED CEED 0.005 PER SIDE．D AND E1 ARE DETERMINED AT DATUM H ．
5．DATUMS A AND B ARE DETERMINED AT DATUM H ．

|  |  |  | MILLII | TERS |
| :---: | :---: | :---: | :---: | :---: |
| DIM | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A2 | 0.049 | －－－－ | 1.24 | －－－－ |
| b | 0.008 | 0.012 | 0.20 | 0.30 |
| c | 0.007 | 0.010 | 0.19 | 0.25 |
| D | 0.193 BSC |  | 4．89 BSC |  |
| E | 0.237 BSC |  | 6.00 BSC |  |
| E1 | 0.154 BSC |  | 3.90 BSC |  |
| e | 0.025 BSC |  | 0.635 BSC |  |
| h | 0.009 | 0.020 | 0.22 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| L2 | 0.010 BSC |  | 0.25 BSC |  |
| M | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ |

GENERIC


MARKING DIAGRAM＊
наванан
XXXXXXX
XXXXXXX
OYYWWG
昭昭昭
XXXXX＝Specific Device Code
YY＝Year
WW＝Work Week
$\mathrm{G} \quad=\mathrm{Pb}-$ Free Package
＊This information is generic．Please refer to device data sheet for actual part marking．Pb－Free indicator，＂$G$＂，may or not be present．

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| ---: | :--- | :--- | :--- |
| DESCRIPTION： | QSOP16 | PAGE 1 OF 1 |

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