AMIS-41682, AMIS-41683

Fault Tolerant CAN Transceiver

ON Semiconductor®

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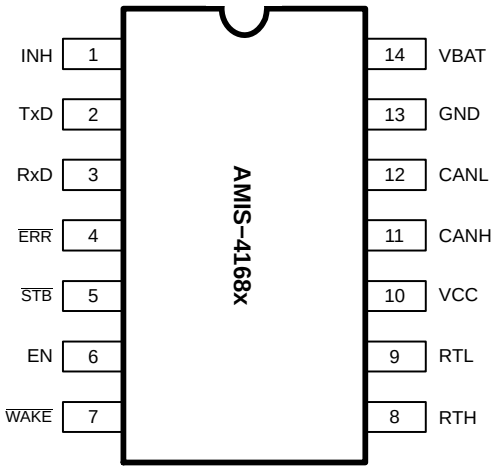
Description

The new AMIS−41682 and AMIS−41683 are interfaces between the protocol controller and the physical wires of the bus lines in a control area network (CAN). AMIS−41683 is identical to the AMIS−41682 but has a true 3.3 V digital interface to the CAN controller. The device provides differential transmit capability but will switch in error conditions to a single−wire transmitter and/or receiver. Initially it will be used for low speed applications, up to 125 kB, in passenger cars.

Both AMIS−41682 and AMIS−41683 are implemented in I2T100 technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

These products consolidate the expertise of ON Semiconductor for in−car multiplex transceivers and support together with 0REMX−002−XTP (VAN), AMIS−30660 and AMIS−30663 (CAN high speed) and AMIS−30600 (LIN) another widely used physical layer.

PIN ASSIGNMENT



(Top View) PC20041029.1

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

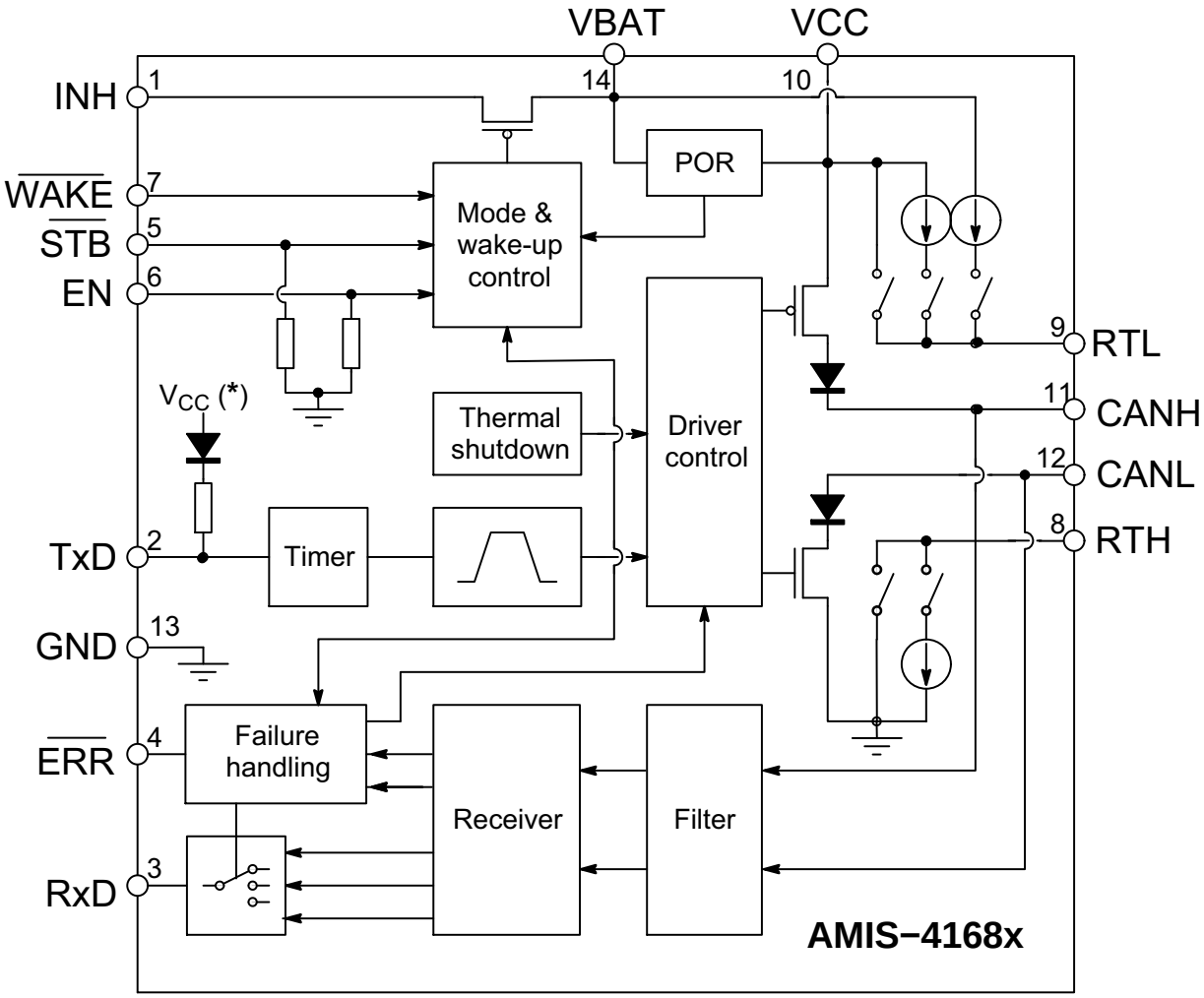
Features

- Fully Compatible with ISO11898−3 Standard
- Optimized for In−Car Low−speed Communication
  - Baud Rate up to 125 kB
  - Up to 32 Nodes can be Connected
  - Due to Built−in Slope Control function and a very Good Matching of the CANL and CANH bus outputs, this device realizes a very low electromagnetic emission (EME)
  - Fully Integrated Receiver Filters
  - Permanent Dominant Monitoring of Transmit Data Input
  - Differential Receiver with Wide Common−Mode Range for High Electromagnetic Susceptibility (EMS) in Normal− and Low−Power Modes
  - True 3.3 V Digital I/O Interface to CAN Controller for AMIS−41683 Only
- Management in Case of Bus Failure
  - In the Event of Bus Failures, Automatic Switching to Single−Wire Mode, even when the CANH Bus Wire is Short−Circuited to V_{CC}
  - The Device will Automatically Reset to Differential Mode if the Bus Failure is Removed
  - During Failure Modes There is Full Wake−up Capability
  - Unpowered Nodes do not Disturb Bus Lines
  - Bus Errors and Thermal Shutdown Activation is Flagged on $\overline{\text{ERR}}$ Pin
- Protection Issues
  - Short Circuit Proof to Battery and Ground
  - Thermal Protection
  - The Bus Lines are Protected Against Transients in an Automotive Environment
  - An Unpowered Node Does not Disturb the Bus Lines
- Support for Low Power Modes
  - Low Current Sleep and Standby Mode with Wake−up via the Bus Lines
  - Power−on Flag on the Output
  - Two−Edge Sensitive Wake−up Input Signal via Pin $\overline{\text{WAKE}}$
- I/Os
  - The unpowered chip cannot be parasitically supplied either from digital inputs or from digital outputs
- These are Pb−Free Devices*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 1. TECHNICAL CHARACTERISTICS

Symbol	Parameter	Condition	Max	Max	Unit
V_{CANH}	DC Voltage at Pin CANH, CANL	0 < V_{CC} < 5.25 V; No Time Limit	−40	+40	V
V_{BAT}	Voltage at Pin V_{bat}	Load−Dump		+40	V



(*) For AMIS-41682 pull up to V_{CC}.
For AMIS-41683 pull up to $V_{CC}/2$

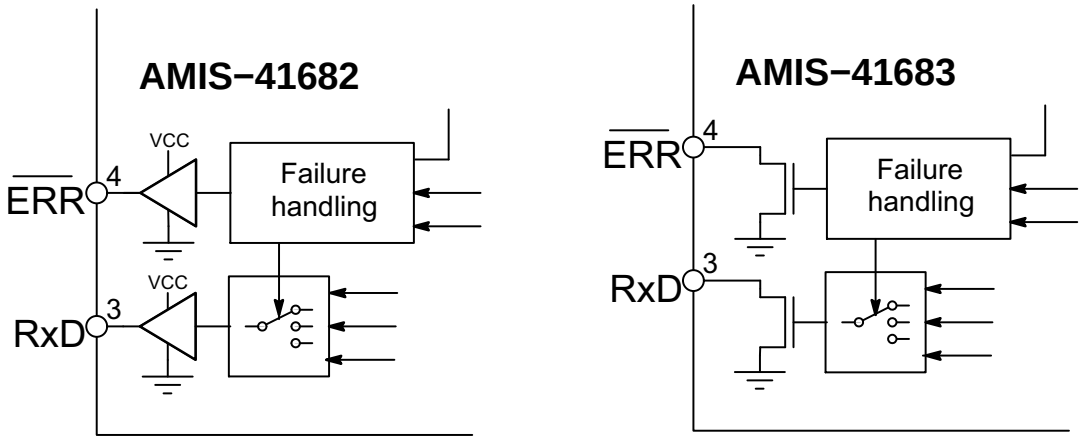


Figure 1. Block Diagram

Table 2. PIN DESCRIPTION

Pin	Name	Description
1	INH	Inhibit Output for External Voltage Regulator
2	TxD	Transmit Data Input; Internal Pullup Current
3	RxD	Receive Data Output
4	$\overline{ERR}$	Error; Wake−up and Power−on Flag; Active Low
5	$\overline{STB}$	Standby Digital Control Input; Active Low; Pulldown Resistor
6	EN	Standby Digital Control Input; Active High; Pulldown Resistor
7	$\overline{WAKE}$	Enable Digital Control Input; Falling and Rising Edges are Both Detected
8	RTH	Pin for External Termination Resistor at CANH
9	RTL	Pin for External Termination Resistor at CANL
10	V_{CC}	5 V Supply Input
11	CANH	Bus Line; High in Dominant State
12	CANL	Bus Line; Low in Dominant State
13	GND	Ground
14	V_{BAT}	Battery Supply

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage on Pin V_{CC}	−0.3	+6	V
V_{BAT}	Battery Voltage on Pin V_{BAT}	−0.3	+40	V
V_{dig}	DC Voltage on Pins EN, $\overline{STB}$, $\overline{ERR}$, TxD, RxD	−0.3	V_{CC} + 0.3	V
$V_{CANH−L}$	DC Voltage on Pin CANH, CANL	−40	+40	V
$V_{tran−CAN}$	Transient Voltage on Pins CANH and CANL (Figure 10) (Note 1)	−350	+350	V
V_{WAKE}	DC Input Voltage on Pin WAKE	−40	+40	V
V_{INH}	DC Output Voltage on Pin INH	−0.3	V_{BAT} + 0.3	V
$V_{RTH−L}$	DC Voltage on Pin RTH, RTL	−40	40	V
R_{RTH}	Termination Resistance on Pin RTH	500	16000	Ω
R_{RTL}	Termination Resistance on Pin RTL	500	16000	Ω
T_J	Maximum Junction Temperature	−40	+150	°C
V_{esd}	Electrostatic discharge voltage (CANH− and CANL Pin) Human Body Model (Note 2)	−6	+6	kV
	Electrostatic Discharge Voltage (Other Pins) Human Body Model (Note 2)	−2.0	+2.0	kV
	Electrostatic Discharge Voltage; CDM (Note 3)	−500	+500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. Class C operation
2. Human Body Model according Mil−Std−883C−Meth−3015.7
3. Charged Device Model according ESD−STM5.3.1−1999

Table 4. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj−a)}$	Thermal Resistance from Junction−to−Ambient in SSOP−14 Package (Two Layer PCB)	In Free Air	140	K/W
$R_{th(vj−s)}$	Thermal Resistance from Junction−to−Substrate of Bare Die	In Free Air	30	K/W

TYPICAL APPLICATION SCHEMATIC

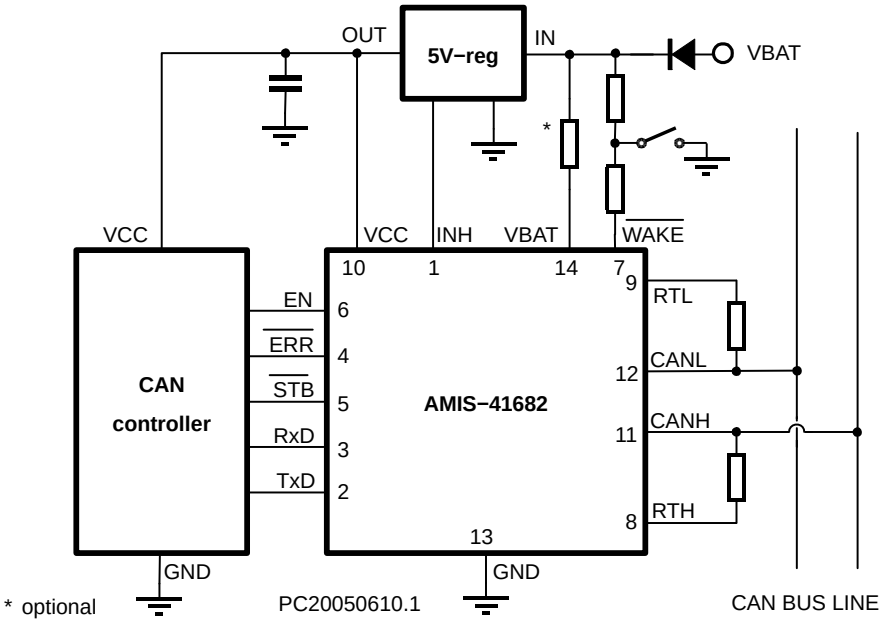


Figure 2. Application Diagram AMIS−41682

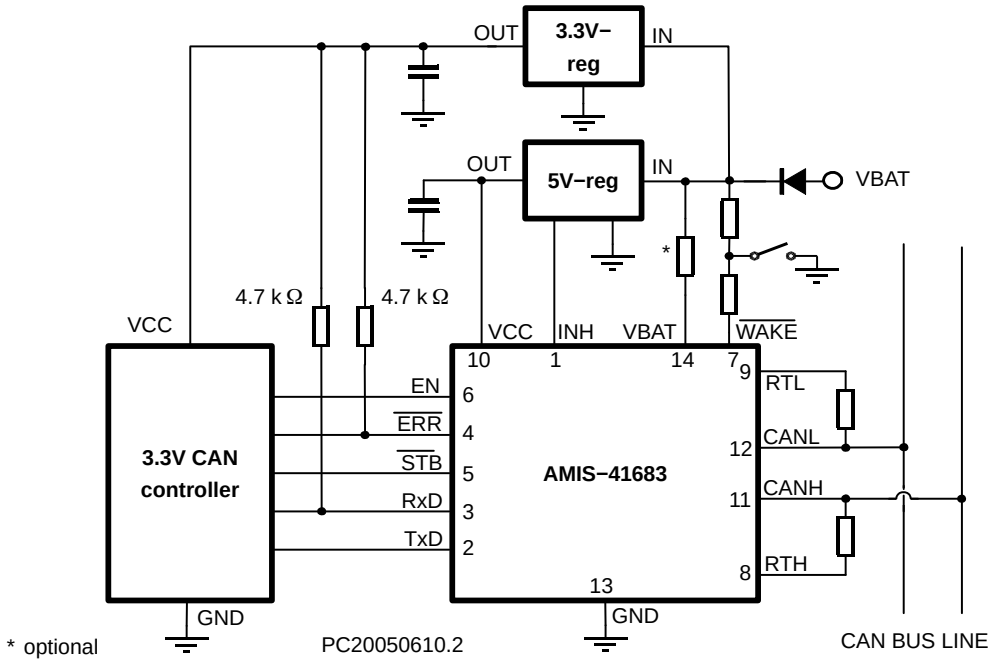


Figure 3. Application Diagram AMIS−41683

The functional description and characteristics are made for AMIS−41682 but are also valid for AMIS−41683. Differences between the two devices will be explicitly mentioned in the text.

FUNCTIONAL DESCRIPTION

Description

AMIS−41682 is a fault tolerant CAN transceiver which works as an interface between the CAN protocol controller and the physical wires of the CAN bus (see Figure 2). It is primarily intended for low speed applications, up to 125 kB, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

The AMIS−41683 has open−drain outputs (RXD and $\overline{\text{ERR}}$ Pins), which allow the user to use external pullup resistors to the required supply voltage; this can be 5 V or 3.3 V.

To reduce EME, the rise and fall slope are limited. Together with matched CANL and CANH output stages, this allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines.

The failure detection logic automatically selects a suitable transmission mode, differential or single−wire transmission. Together with the transmission mode, the failure detector will configure the output stages in such a way that excessive currents are avoided and the circuit returns to normal operation when the error is removed.

A high common−mode range for the differential receiver guarantees reception under worst case conditions and together with the integrated filter the circuit realizes an excellent immunity against EMS. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single−wire mode.

A timer has been integrated at Pin TXD. This timer prevents the AMIS−41682 from driving the bus lines to a permanent dominant state.

Failure Detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode. The different wiring failures are depicted in Figure 4. The figure also indicates the effect of the different wiring failures on the transmitter and the receiver. The detection circuit itself is not depicted.

The differential receiver threshold voltage is typically set at 3 V (V_{CC} = 5 V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 5, and 6a. These failures, or recovery from them, do not destroy ongoing transmissions. During the failure, reception is still done by the differential receiver and the transmitter stays fully active.

To avoid false triggering by external RF influences the single−wire modes are activated after a certain delay time. When the bus failure disappears for another time delay, the transceiver switches back to the differential mode. When one of the bus failures 3, 3a, 4, 6, and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and the respective output stage. A wake−up from sleep mode via the bus is possible either by way of a dominant CANH or CANL line. This ensures that a wake−up is possible even if one of the failures 1 to 7 occurs. If any of the wiring failure occurs, the output signal on pin $\overline{\text{ERR}}$ will become low. On error recovery, the output signal on pin $\overline{\text{ERR}}$ will become high again.

During all single−wire transmissions, the EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut−off frequency of these filters is a compromise between propagation delay and HF suppression. In the single−wire mode, LF noise cannot be distinguished from the required signal.

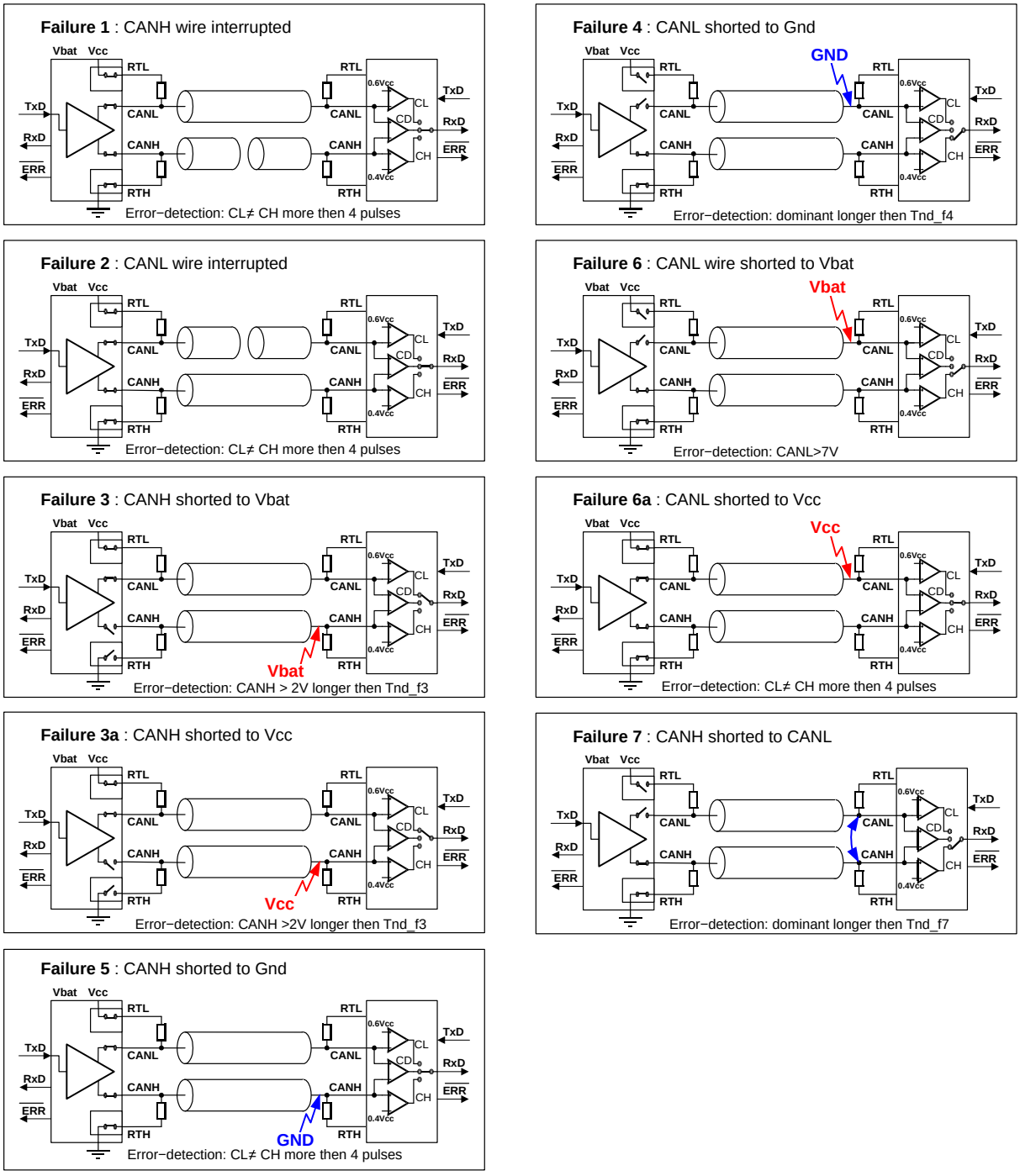


Figure 4. Different Types of Wiring Failure

Low Power Modes

The transceiver provides three low power modes, which can be entered and exited via Pins STBB and EN (see Figure 5). (Go−to−sleep mode is only a transition mode.)

The sleep mode is the mode with the lowest power consumption. Pin INH is switched to high−impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via Pin RTL. If the supply voltage is provided, Pins RXD and $\overline{\text{ERR}}$ will signal the wake−up interrupt signal.

The standby mode will react the same as the sleep mode but with a high−level on pin INH.

The power−on standby mode is the same as the standby mode with the battery power−on flag instead of the wake−up interrupt signal on Pin $\overline{\text{ERR}}$. The output on Pin RXD will show the wake−up interrupt. This mode is only for reading out the power−on flag.

Wake−up request is detected by the following events:

- Local Wake−up: Rising or falling edge on input $\overline{\text{WAKE}}$ (levels maintained for a certain period).
- Remote Wake−up from CAN Bus: A message with five consecutive dominant bits.

On a wake−up request the transceiver will set the output on Pin INH high which can be used to activate the external supply voltage regulator. Note: Pin INH is also set similarly as an after wake up event by V_{BAT} voltage being below the battery power on flag level. (See FLAG_VBAT in Figure 5)

If V_{CC} is provided, the wake−up request can be read on the $\overline{\text{ERR}}$ or RXD outputs so the external microcontroller can wake−up the transceiver (switch to normal operating mode) via Pins $\overline{\text{STB}}$ and EN.

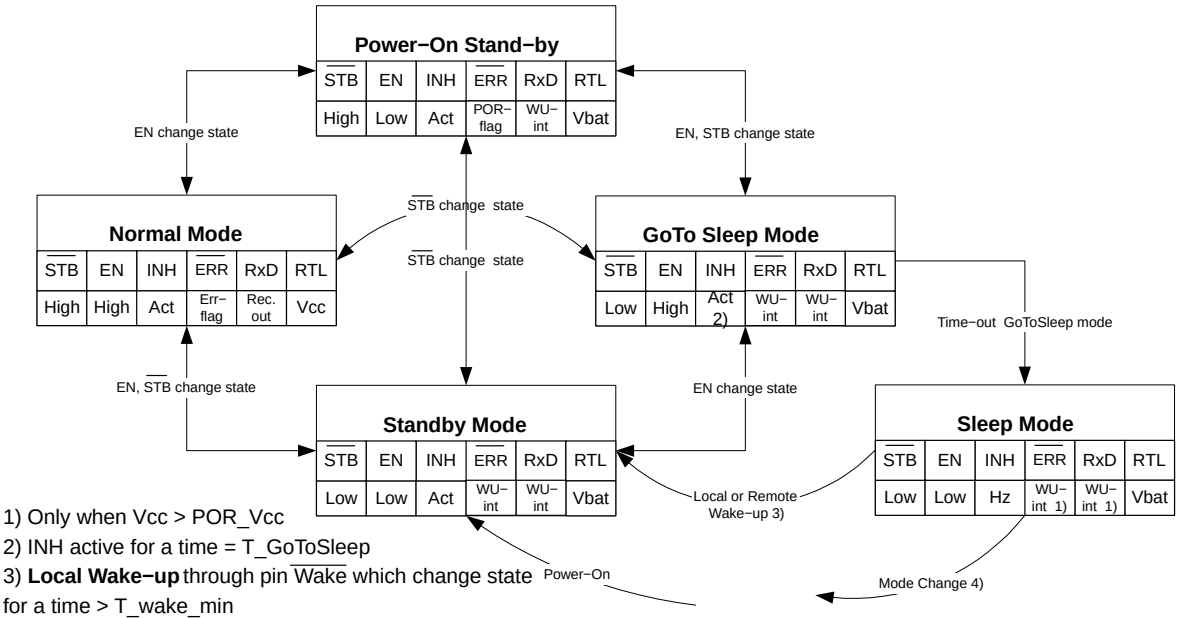
In the low power modes the failure detection circuit remains partly active to prevent increased power consumption in the event of failures 3, 3a, 4, and 7.

The go−to−sleep−mode is only a transition mode. The Pin INH stays active for a limited time. During this time the circuit can still go to another low−power mode. After this time the circuit goes to the sleep−mode. In case of a wake up request (from BUS or $\overline{\text{WAKE}}$ Pin) during this transition time, the wake−up request has higher priority than go−to−sleep and INH will not be deactivated.

Behavior in Case of Missing Supplies

If V_{CC} is below the threshold level FLAG_V_{CC}, the signals on pins $\overline{\text{STB}}$ and EN will internally be set to low-level to provide fail safe functionality. In this way, a low-power mode will be forced in case of missing/failing V_{CC} supply. Similarly, missing/failing V_{BAT} supply – i.e. V_{BAT} being below FLAG_V_{BAT} level - will lead to a fail-safe behavior of the transceiver by forcing a low-power mode.

A forced low-power in case of missing supplies guarantees that the transceiver will in no way disturb the other CAN nodes when the local electronic unit looses ground or battery connection.



1) Only when Vcc > POR_Vcc
2) INH active for a time = T_GoToSleep
3) **Local Wake−up** through pin $\overline{\text{Wake}}$ which change state for a time > T_wake_min
Remote Wake−up through pin CANL or CANH when dominant for a time >TCANH_min or TCANL_min
4) **Mode Change** through pins $\overline{\text{STB}}$ and EN is only possible if Vcc > POR_Vcc

Figure 5. Low Power Modes

Power−On

After power−on (V_{BAT} switched on) the signal on Pin INH will become high and an internal power−on flag will be set. This flag can be read in the power−on standby mode via pin $\overline{\text{ERR}}$ ($\overline{\text{STB}}$ = 1; EN = 0) and will be reset by entering the normal operating mode.

Protections

A current limiting circuit protects the transmitter output stages against short circuit to positive and negative battery voltage. If the junction temperature exceeds a maximum value, the transmitter output stages are disabled and flagged on the $\overline{\text{ERR}}$ pin. Because the transmitter is responsible for the major part of the power dissipation, this will result in reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operating.

The Pins CANH and CANL are protected against electrical transients that may occur in an automotive environment.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 13). Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

Table 5. CHARACTERISTICS AMIS−4168x V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 36 V, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES V_{CC} V_{BAT}						
I_{CC}	Supply Current	Normal Operating Mode; VTXD = V_{CC} (Recessive)	1	3.7	6.3	mA
		Normal Operating Mode; VTXD = 0 V (Dominant); No Load	1	8	12	mA
FLAG_V_{CC}	Forced Low Power Mode	V_{CC} Rising V_{CC} Falling	 2.45		4.5	V
I_{BAT}	Battery Current on Pin BAT	In All Modes of Operation; 500 V between RTL − CANL 500 V between RTH − CANH V_{BAT} = WAKE = INH = 5 V to 36 V	10	110	230	μA
		In Sleepmode V_{CC} = 0 V, V_{BAT} = 12.5 V T_A = 70°C		35	42	μA
I_{CC}+ I_{BAT}	Supply Current Plus Battery Current	Low power modes; V_{CC} = 5 V; T_A = −40°C to 100°C V_{BAT} = WAKE = INH = 5 to 36V		30	60	μA
I_{CC}+ I_{BAT}	Supply Current Plus Battery Current	Low power modes; V_{CC} = 5 V; T_A = 100°C to 150°C V_{BAT} = WAKE = INH = 5 V to 36 V			80	μA
FLAG_V_{BAT}	Power−on Flag−Level for Pin V_{BAT}	For Setting Power−on Flag For Not Setting Power−on Flag	 3.5	2.1 2.4	1	V
PINS $\overline{STB}$, EN AND TXD						
R_{PD}	Pulldown Resistor at Pin EN and $\overline{STB}$	1 V	190	360	600	kΩ
T_{DisTxD}	Dominant Time−out for TxD	Normal Mode; VtxD = 0 V	0.75		4	ms
$T_{GoToSleep}$	Minimum Hold−Time for Go−To−Sleep Mode		5		50	μs
PIN $\overline{WAKE}$						
I_{IL}	Low−Level Input Current	V_{WAKE} = 0 V; V_{BAT} = 27V	−10		−1	μA
$V_{th(WAKE)}$	Wake−up Threshold Voltage	$V_{\overline{STB}}$ = 0 V	2.5	3.2	3.9	V
$T_{WakeMin}$	Minimum Time on Pin Wake (De-bounce Time)	V_{BAT} = 12 V; Low Power Mode; for Rising and Falling Edge	7		38	μs
PIN INH						
ΔV_H	High−Level Voltage Drop	IINH = ±0.18 mA			0.8	V
I_{leak}	Leakage Current	Sleep mode; VINH = 0 V			1	μA

Table 6. CHARACTERISTICS AMIS−41682 (5 V Version) V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 36 V, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PINS $\overline{STB}$, EN AND TXD						
V_{IH}	High−level input voltage		0.7 x V_{CC}		6.0	V
V_{IL}	Low−level input voltage		−0.3		0.3 x V_{CC}	V
I−PU−H	High−level input current pin TXD	TXD = 0.7 * V_{CC}	−10		−200	μA
I−PU−L	Low−level input current pin TXD	TXD = 0.3 * V_{CC}	−80		−800	μA
PINS RXD AND $\overline{ERR}$						
V_{OH}	High−level output voltage	Isource = −1 mA	V_{CC} − 0.9		V_{CC}	V
V_{OL}	Low−level output voltage	Isink = 1.6 mA	0		0.4	V
		Isink = 7.5 mA	0		1.5	V

Table 7. CHARACTERISTICS AMIS−41683 (3.3 Version) V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 36 V, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PINS $\overline{STB}$, EN AND TXD						
V_{IH}	High−Level Input Voltage		2		6.0	V
V_{IL}	Low−Level Input Voltage		−0.3		0.8	V
I−PU−H	High−Level Input Current Pin TXD	TXD = 2 V		−10		μA
PINS RXD AND $\overline{ERR}$						
V_{OL}	Low−Level Output Voltage Open Drain	Isink = 3.2 mA			0.4	V
I_{leak}	Leakage When Driver is Off	V$\overline{ERR}$ = VRXD = 5 V			1	μA

Table 8. CHARACTERISTICS AMIS−4168x V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 36 V, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins CANH and CANL (Receiver)						
V_{diff}	Differential Receiver Threshold Voltage	No Failures and Bus Failures 1, 2, 4, and 6a (See Figure 4) V_{CC} = 5 V V_{CC} = 4.75 V to 5.25 V	−3.25 0.65 x V_{CC}	−3 0.6 x V_{CC}	−2.75 0.55 x V_{CC}	V
VseCANH	Single−Ended Receiver Threshold Voltage on Pin CANH	Normal Operating Mode and Failures 4, 6 and 7 V_{CC} = 5 V V_{CC} = 4.75 V to 5.25 V	1.6 0.32 x V_{CC}	1.775 0.355 x V_{CC}	1.95 0.39 x V_{CC}	V
VseCANL	Single−Ended Receiver Threshold Voltage on Pin CANL	Normal Operating Mode and Failures 3 and 3a V_{CC} = 5 V V_{CC} = 4.75 V to 5.25 V	3 0.61 x V_{CC}	3.2 0.645 x V_{CC}	3.4 0.68 x V_{CC}	V V
$V_{det(CANL)}$	Detection Threshold Voltage for Short Circuit to Battery Voltage on Pin CANL	Normal Operating Mode	6.5	7.3	8	V
$V_{th(wake)}$	Wake−up Threshold Voltage On Pin CANL On Pin CANH	Low Power Modes	 2.5 1.1	 3.2 1.8	 3. 9 2.25	V

Table 8. CHARACTERISTICS AMIS−4168x V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 36 V, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pins CANH and CANL (Receiver)						
$DV_{th(wake)}$	Difference of Wake−up Threshold Voltages	Low Power Modes	0.8	1.4		V
PINS CANH AND CANL (TRANSMITTER)						
$V_{O(reces)}$	Recessive Output Voltage On Pin CANH On Pin CANL	$V_{TXD} = V_{CC}$ R_{RTH} < 4 kΩ R_{RTL} < 4 kΩ	 V_{CC} − 0.2		 0.2	V
$V_{O(dom)}$	Dominant Output Voltage On Pin CANH On Pin CANL	V_{TXD} = 0V; $V_{EN} = V_{CC}$ 0 mA ≥ I_{CANH} ≥ −40 mA 0 mA ≤ I_{CANL} ≤ 40 mA	 V_{CC} − 1.4		 1.4	V
$I_{O(CANH)}$	Output Current on Pin CANH	Normal Operating Mode; V_{CANH} = 0V; VTXD = 0 V	−110	−80	−45	mA
		Low Power Modes; V_{CANH} = 0V; V_{CC} = 5 V	−1.6	0.5	1.6	μA
$I_{O(CANL)}$	Output Current on Pin CANL	Normal Operating Mode; V_{CANL} = 14 V; V_{TXD} = 0 V	45	80	110	mA
		Low Power Modes; V_{CANL} = 12 V; V_{BAT} = 12 V	−1	0.5	1	μA
PINS RTH AND RTL						
$R_{SW(RTL)}$	Switch−on Resistance Between Pin RTL and V_{CC}	Normal operating mode; I(RTL) > −10 mA			100	Ω
$R_{SW(RTH)}$	Switch−on Resistance Between Pin RTH and ground	Normal operating mode; I(RTH) < 10 mA			100	Ω
VO(RTH)	Output Voltage on Pin RTH	Low power modes; I_O = 1 mA			1.0	V
IO(RTL)	Output Current on Pin RTL	Low power modes; V_{RTL} = 0 V	−1.25		−0.3	mA
Ipu(RTL)	Pullup Current on Pin RTL	Normal operating mode and failures 4, 6 and 7; V_{RTL} = 0 V		−75		μA
Ipd(RTH)	Pulldown Current on Pin RTH	Normal operating mode and failures 3 and 3a		−75		μA
THERMAL SHUTDOWN						
T_J	Junction Temperature	For Shutdown	150		180	°C

Table 9. TIMING CHARACTERISTICS AMIS−4168x V_{CC} = 4.75 V to 5.25 V, V_{BAT} = 5 V to 27 V, $V_{\overline{STB}} = V_{CC}$, T_J = −40°C to +150°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(r-d)}$	CANL and CANH Output Transition Time for Recessive−to−Dominant	10 to 90%; C1 = 10 nF; C2 = 0; R1 = 125 Ω (See Figure 6)	0.35	0.60	1.4	μs
$t_{t(d-r)}$	CANL and CANH Output Transition Time for Dominant−to−Recessive	10 to 90%; C1 = 1 nF; C2 = 0; R1 = 125 Ω (See Figure 6)	0.2	0.3	0.7	μs
$t_{PD(L)}$	Propagation Delay TXD to RXD (LOW)	No Failures C1 = 1 nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3 nF; R1 = 125 Ω		 0.75 1.4	 1.5 2.1	μs
		Failures 1, 2, 5, and 6a (See Figures 4 and 6)		 1.2 1.4	 1.9 2.1	μs
		Failures 3, 3a, 4, 6, and 7 (See Figures 4 and 6) C1 = 1 nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3 nF; R1 = 125 Ω C1 = 1 nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3nF; R1 = 125 Ω		 1.2 1.5	 1.9 2.2	μs
$t_{PD(H)}$	Propagation Delay TXD to RXD (HIGH)	No Failures C1 = 1 nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3nF; R1 = 125 Ω		 0.75 2.5	 1.5 3.0	μs
		Failures 1, 2, 5, and 6a (See Figures 4 and 6) C1 = 1nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3nF; R1 = 125 Ω		 1.2 2.5	 1.9 3.0	μs
		Failures 3, 3a, 4, 6, and 7 (See Figures 4 and 6) C1 = 1 nF; C2 = 0; R1 = 125 Ω C1 = C2 = 3.3 nF; R1 = 125 Ω		 1.2 1.5	 1.9 2.2	μs
$t_{CANH(min)}$	Minimum Dominant Time for Wake−up on Pin CANH	Low Power Modes; V_{BAT} = 12 V	7		38	μs
$t_{CANL(min)}$	Minimum Dominant Time for Wake−up on Pin CANL	Low Power Modes; V_{BAT} = 12 V	7		38	μs
t_{det}	Failure Detection Time	Normal Mode Failure 3 and 3a Failure 4, 6 and 7	 1.6 0.3		 8.0 1.6	ms
		Low Power Modes; V_{BAT} = 12 V Failure 3 and 3a Failure 4 and 7	 1.6 0.1		 8.0 1.6	ms
t_{rec}	Failure Recovery Time	Normal Mode Failure 3 and 3a Failure 4 and 7 Failure 6	 0.3 7 125		 1.6 38 750	 ms μs μs
		Low Power Modes; V_{BAT} = 12 V Failures 3, 3a, 4, and 7	0.3		1.6	ms
D_{pc}	Pulse−Count Difference Between CANH and CANL	Normal Mode and Failures 1, 2, 5, and 6a Failure Detection (Pin $\overline{ERR}$ becomes LOW) Failure Recovery (Pin $\overline{ERR}$ becomes HIGH)		 4 4		−

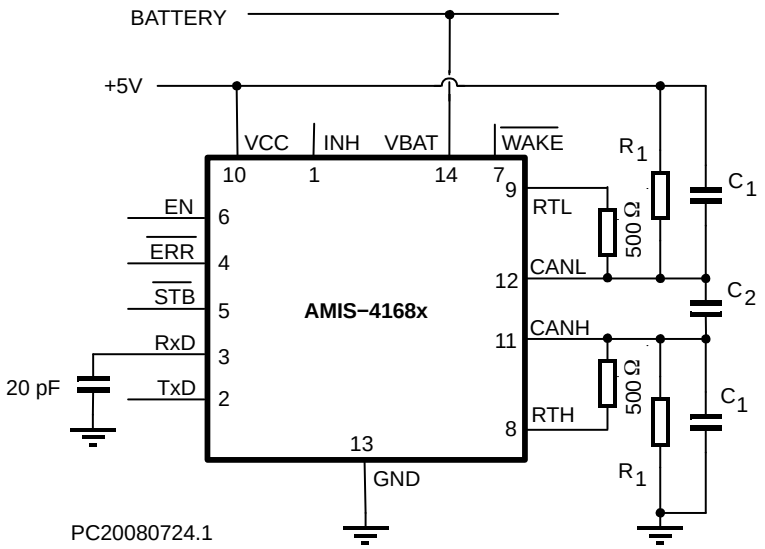


Figure 6. Test Circuit for Dynamic

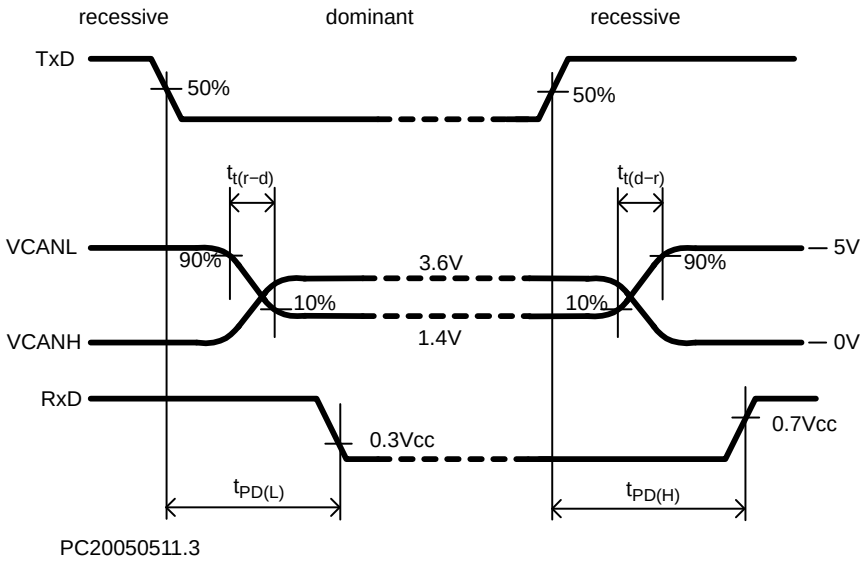


Figure 7. Timing Diagram for AC Characteristics

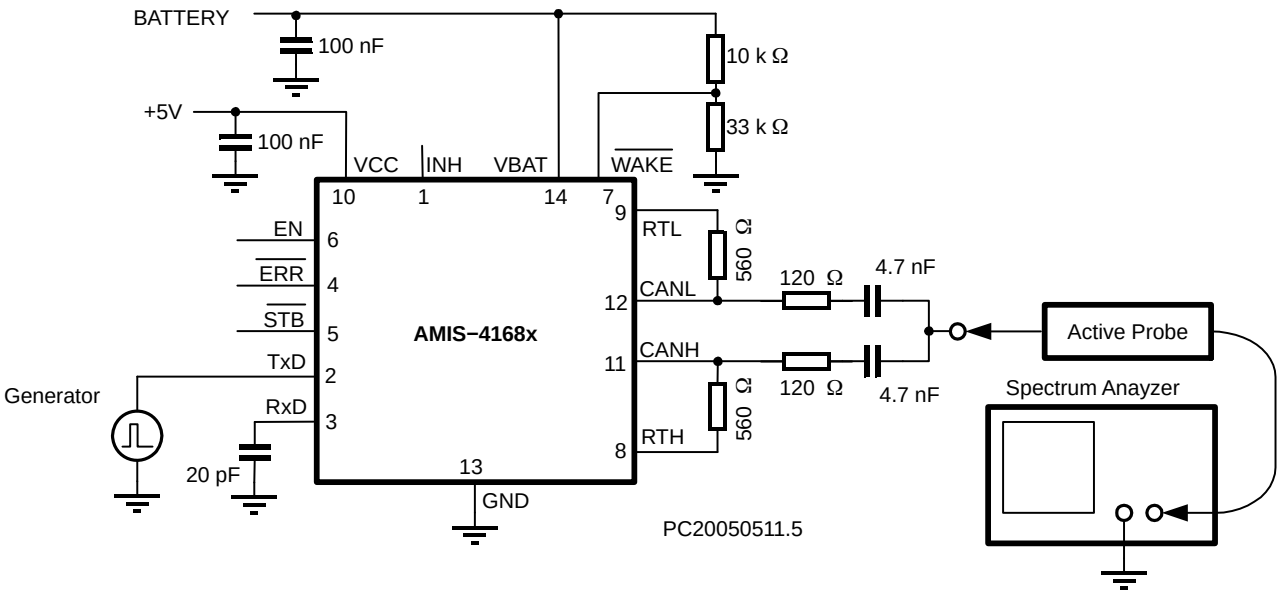


Figure 8. Test Set−up EME Measurements

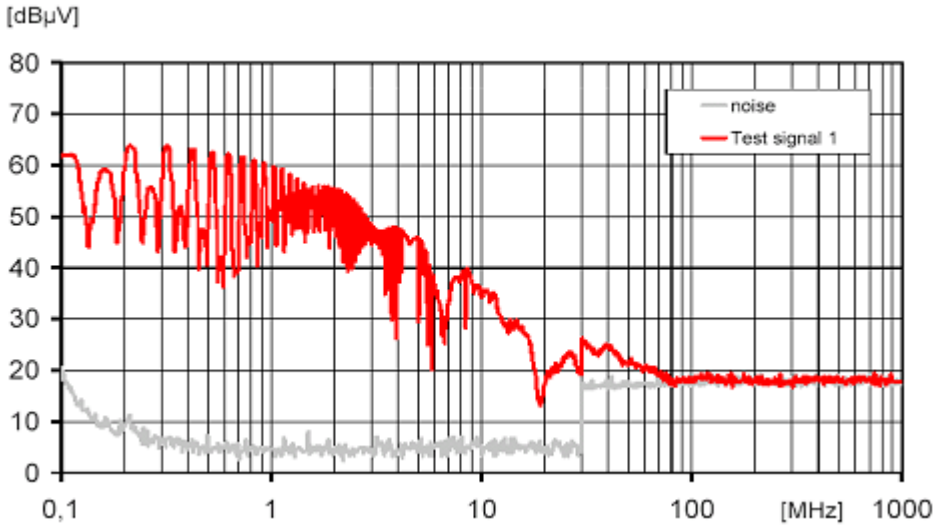


Figure 9. EME Measurements (See Figure 8)

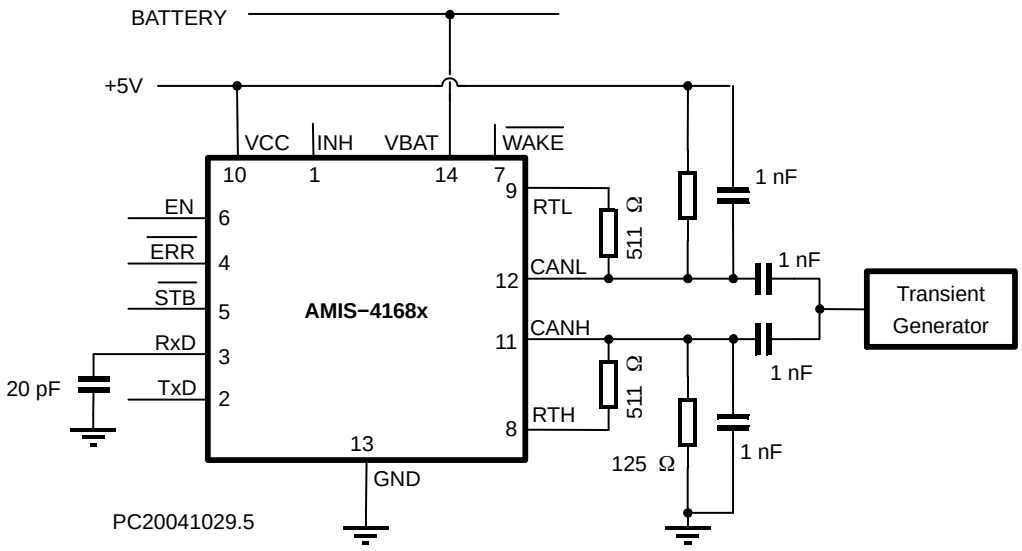


Figure 10. Test Circuit for Schaffner Tests (ISO 7637 part)

DEVICE ORDERING INFORMATION

Part Number	Voltage	Temperature Range	Package Type	Shipping†
AMIS41682CANM1G	5 V	−40°C − 125°C	SOIC−14 (Pb−Free)	55 Tube / Tray
AMIS41682CANM1RG	5 V	−40°C − 125°C	SOIC−14 (Pb−Free)	3000 / Tape & Reel
AMIS41683CANN1G	3.3 V	−40°C − 125°C	SOIC−14 (Pb−Free)	55 Tube / Tray
AMIS41683CANN1RG	3.3 V	−40°C − 125°C	SOIC−14 (Pb−Free)	3000 / Tape & Reel

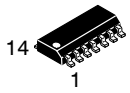
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

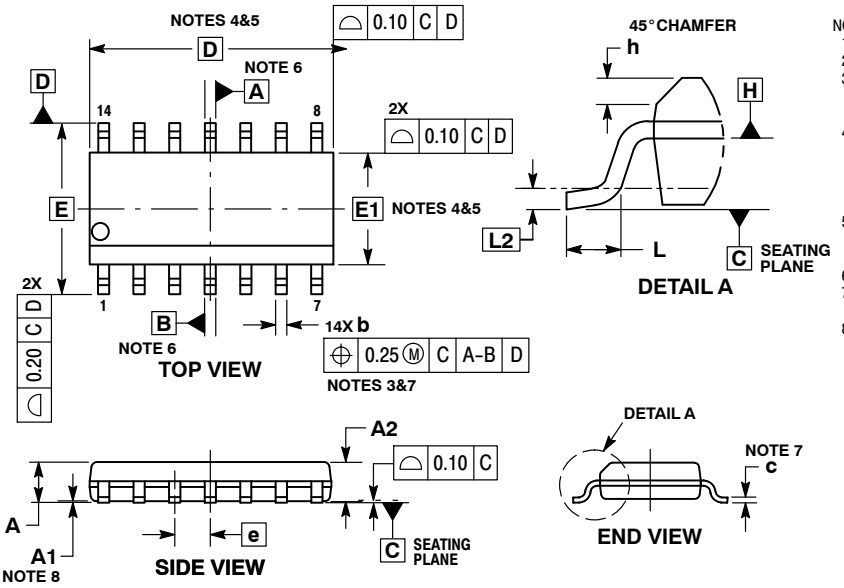
ON Semiconductor®

SOIC−14
CASE 751AP
ISSUE B

DATE 18 MAY 2015



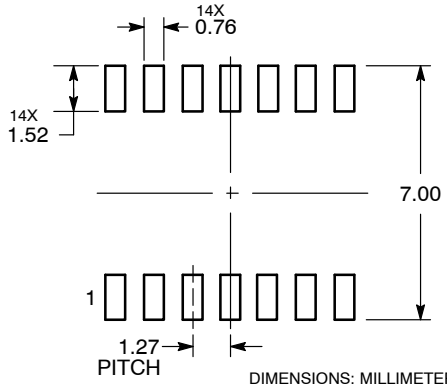
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

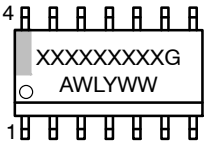
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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