CM2009

VGA Port Companion Circuit

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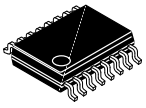
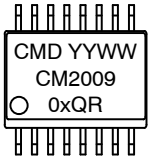


QSOP16
QR SUFFIX
CASE 492

MARKING DIAGRAM



CM2009 0xQR = Specific Device Code
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
CM2009−00QR	QSOP−16 (Pb−Free)	2500/Tape & Reel
CM2009−02QR	QSOP−16 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Product Description

The CM2009 connects between a video graphics controller embedded in a PC, graphics adapter card or set top box and the VGA or DVI−I port connector. The CM2009 incorporates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the video, DDC and SYNC lines is implemented with low−capacitance current steering diodes.

All ESD diodes are designed to safely handle the high current spikes specified by IEC−61000−4−2 Level 4 (±8 kV contact discharge if C_{BYP} is present, ±4 kV if not). The ESD protection for the DDC signal pins are designed to prevent "back current" when the device is powered down while connected to a monitor that is powered up.

Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs to provide design flexibility in multi−supply−voltage environments.

Two non−inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC_SYNC}, which is typically 5 V. Additionally, each driver has a series termination resistor (R_T) connected to the SYNC_OUT pin, eliminating the external termination resistors typically required for the HSYNC and VSYNC lines of the video cable. There are three versions with different values of R_T to allow termination at typically 65 Ω (CM2009−00) or 15 Ω (CM2009−02).

The 15 Ω (CM2009−02) version will typically require two external resistors which can be chosen to exactly match the characteristic impedance of the SYNC lines of the video cable.

Two N−channel MOSFETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. The gate terminals for these MOSFETS (V_{CC_DDC}) should be connected to the supply rail (typically 3.3 V) that supplies power to the transceivers of the DDC controller.

Features

- Includes ESD Protection, Level−Shifting, Buffering and Sync Impedance Matching
- 7 Channels of ESD Protection for all VGA Port Connector Pins Meeting IEC−61000−4−2 Level 4 ESD Requirements (±8 kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines (4 pF Maximum)
- 5 V Drivers for HSYNC and VSYNC Lines
- Integrated Impedance Matching Resistors on Sync Lines
- Bi−directional Level Shifting N−Channel FETs Provided for DDC_CLK & DDC_DATA Channels
- Backdrive Protection on DDC Lines
- Compact 16−Lead QSOP Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- VGA and DVI−I Ports in:
  - Desktop and Notebook PCs
  - Graphics Cards
  - Set Top Boxes

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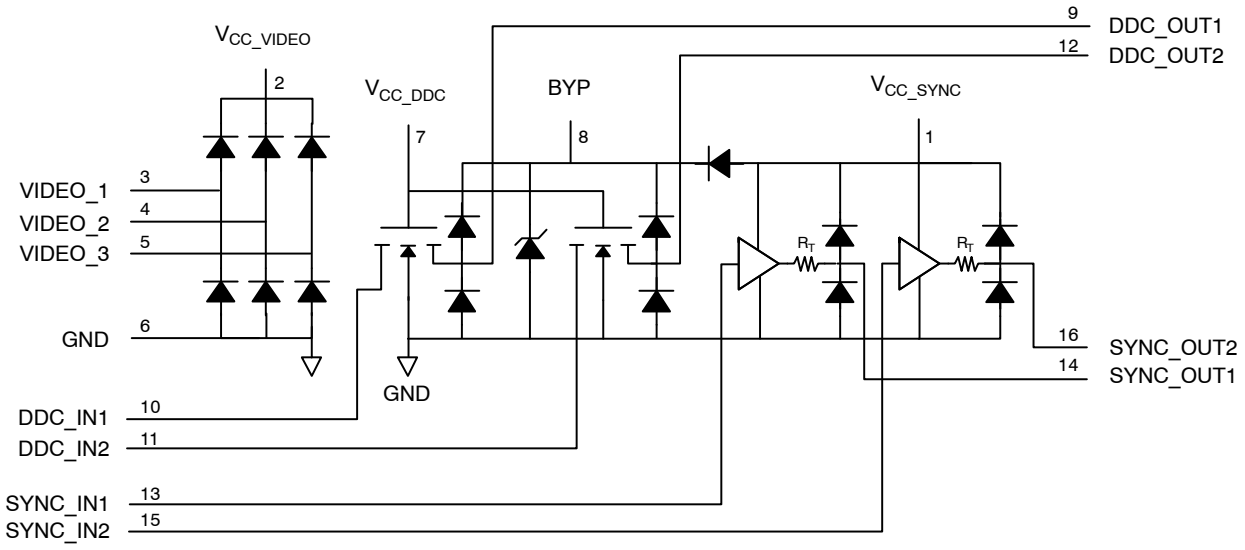
May, 2012 − Rev. 5

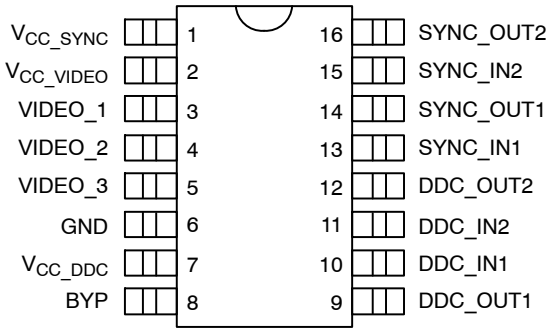
Publication Order Number:
CM2009/D

SIMPLIFIED ELECTRICAL SCHEMATIC



PACKAGE / PINOUT DIAGRAM

Top View



16 Pin QSOP

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	V_{CC_SYNC}	This is an isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits.
2	V_{CC_VIDEO}	This is a supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits.
3	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
4	VIDEO_2	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
5	VIDEO_3	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
6	GND	Ground reference supply pin.
7	V_{CC_DDC}	This is an isolated supply input for the DDC_1 and DDC_2 level−shifting N−FET gates.
8	BYP	This input is used to connect an external 0.2 μF bypass capacitor to the DDC circuits, resulting in an increased ESD withstand voltage rating for these circuits (±8 kV with vs. ±4 kV without).
9	DDC_OUT1	DDC signal output. Connects to the video connector side of one of the sync lines.
10	DDC_IN1	DDC signal input. Connects to the VGA controller side of one of the sync lines.

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
11	DDC_IN2	DDC signal input. Connects to the VGA controller side of one of the sync lines.
12	DDC_OUT2	DDC signal output. Connects to the video connector side of one of the sync lines.
13	SYNC_IN1	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
14	SYNC_OUT1	Sync signal buffer output. Connects to the video connector side of one of the sync lines.
15	SYNC_IN2	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
16	SYNC_OUT2	Sync signal buffer output. Connects to the video connector side of one of the sync lines.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
V_{CC_VIDEO}, V_{CC_DDC} and V_{CC_SYNC} Supply Voltage Inputs	[GND − 0.5] to +6.0	V
ESD Diode Forward Current (one diode conducting at a time)	10	mA
DC Voltage at Inputs VIDEO_1, VIDEO_2, VIDEO_3 DDC_IN1, DDC_IN2 DDC_OUT1, DDC_OUT2 SYNC_IN1, SYNC_IN2	 [GND − 0.5] to [V_{CC_VIDEO} + 0.5] [GND − 0.5] to 6.0 [GND − 0.5] to 6.0 [GND − 0.5] to [V_{CC_SYNC} + 0.5]	V
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−40 to +150	°C
Package Power Rating (T_A = 25°C)	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC_VIDEO}	V_{CC_VIDEO} Supply Current	V_{CC_VIDEO} = 5.0 V; VIDEO inputs at V_{CC_VIDEO} or GND			10	μA
I_{CC_DDC}	V_{CC_DDC} Supply Current	V_{CC_DDC} = 5.0 V			10	μA
I_{CC_SYNC}	V_{CC_SYNC} Supply Current	V_{CC_SYNC} = 5 V; SYNC inputs at GND or V_{CC_SYNC}; SYNC outputs unloaded			50	μA
		V_{CC_SYNC} = 5 V; SYNC inputs at 3.0 V; SYNC outputs unloaded			2.0	mA
V_F	ESD Diode Forward Voltage	I_F = 10 mA			1.0	V
V_{IH}	Logic High Input Voltage	V_{CC_SYNC} = 5.0 V; (Note 2)	2.0			V
V_{IL}	Logic Low Input Voltage	V_{CC_SYNC} = 5.0 V; (Note 2)			0.6	V
V_{OH}	Logic High Output Voltage	I_{OH} = 0 mA, V_{CC_SYNC} = 5.0 V; (Note 2)	4.85			V
V_{OL}	Logic Low Output Voltage	I_{OL} = 0 mA, V_{CC_SYNC} = 5.0 V; (Note 2)			0.15	V
R_{OUT}	SYNC Driver Output Resistance (CM2009−00 only)	V_{CC_SYNC} = 5.0 V; SYNC Inputs at GND or 3.0 V		65		Ω
R_{OUT}	SYNC Driver Output Resistance (CM2009−02 only)	V_{CC_SYNC} = 5.0 V; SYNC Inputs at GND or 3.0 V; (Note ?)		15		Ω
V_{OH-02}	Logic High Output Voltage (CM2009−02 only)	I_{OH} = 24 mA; V_{CC_SYNC} = 5.0 V; (Note 2)	2.0			V
V_{OL-02}	Logic Low Output Voltage (CM2009−02 only)	I_{OL} = 24 mA; V_{CC_SYNC} = 5.0 V; (Note 2)			0.8	V
I_{IN}	Input Current VIDEO Inputs	V_{CC_VIDEO} = 5.0 V; V_{IN} = V_{CC_VIDEO} or GND			±1	μA
	SYNC_IN1, SYNC_IN2 Inputs	V_{CC_SYNC} = 5.0 V; V_{IN} = V_{CC_SYNC} or GND			±1	μA
I_{OFF}	Level Shifting N−MOSFET "OFF" State Leakage Current	(V_{CC_DDC} − V_{DDC_IN}) ≤ 0.4 V; V_{DDC_OUT} = V_{CC_DDC}			10	μA
		(V_{CC_DDC} − V_{DDC_OUT}) ≤ 0.4 V; V_{DDC_IN} = V_{CC_DDC}			10	μA
V_{ON}	Voltage Drop Across Level−shifting N−MOSFET when "ON"	V_{CC_DDC} = 2.5 V; V_S = GND; I_{DS} = 3 mA;			0.18	V
C_{IN_VID}	VIDEO Input Capacitance	V_{CC_VIDEO} = 5.0 V; V_{IN} = 2.5 V; f = 1 MHz; (Note 4)			4	pF
		V_{CC_VIDEO} = 2.5 V; V_{IN} = 1.25 V; f = 1 MHz; (Note 4)			4.5	pF
t_{PLH}	SYNC Driver L => H Propagation Delay	C_L = 50 pF; V_{CC} = 5.0 V; Input t_R and t_F ≤ 5 ns			12	ns
t_{PHL}	SYNC Driver H => L Propagation Delay	C_L = 50 pF; V_{CC} = 5.0 V; Input t_R and t_F ≤ 5 ns			12	ns
t_R, t_F	SYNC Driver Output Rise & Fall Times	C_L = 50 pF; V_{CC} = 5.0 V; Input t_R and t_F ≤ 5 ns		4		ns
V_{ESD}	ESD Withstand Voltage	V_{CC_VIDEO} = V_{CC_SYNC} = 5 V; (Notes 3, 4 & ?)	±8			kV

1. All parameters specified over standard operating conditions unless otherwise noted.
2. These parameters apply only to the SYNC drivers. Note that R_{OUT} = R_T + R_{BUFFER}.
3. Per the IEC−61000−4−2 International ESD Standard, Level 4 contact discharge method. BYP, V_{CC_VIDEO} and V_{CC_SYNC} must be bypassed to GND via a low impedance ground plane with a 0.2 μF, low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulses can be positive or negative with respect to GND. Applicable pins are: VIDEO_1, VIDEO_2, VIDEO_3, SYNC_OUT1, SYNC_OUT2, DDC_OUT1 and DDC_OUT2. All other pins are ESD protected to the industry standard ±2 kV Human Body Model (MIL−STD−883, Method 3015). The bypass capacitor at the BYP pin may optionally be omitted, in which case the max. ESD withstand voltage for the DDC_OUT1 and DDC_OUT2 pins is reduced to ±4 kV.
4. The SYNC_OUT pins on the CM2009−02 are guaranteed for 2 kV HBM ESD protection.

APPLICATION INFORMATION

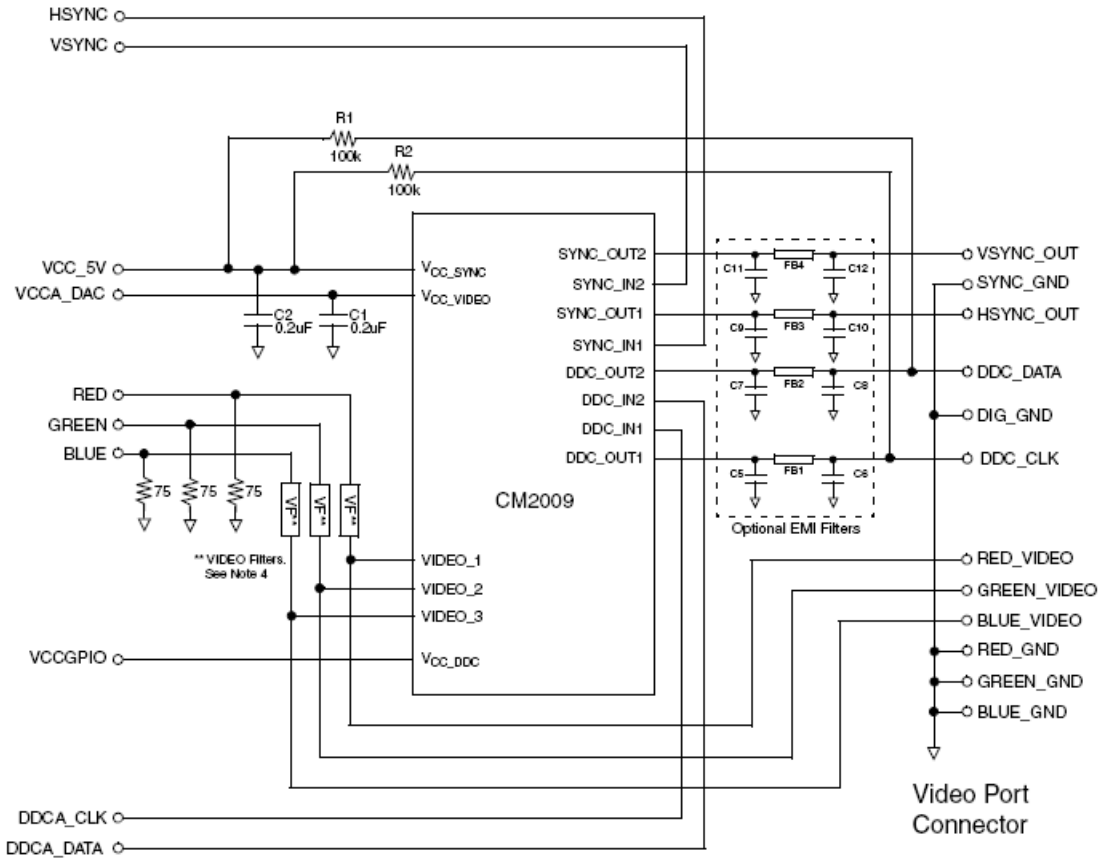
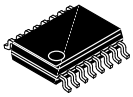


Figure 1. Typical Application Connection Diagram

NOTES:

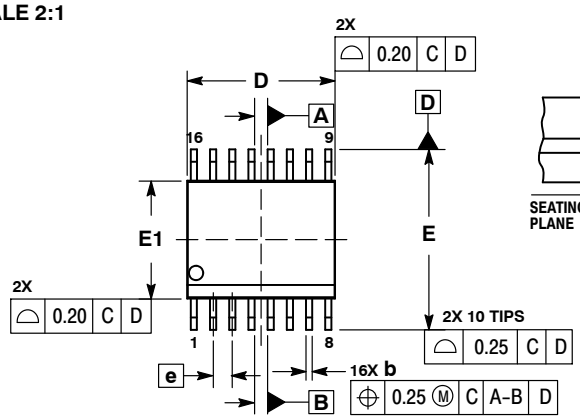
1. The CM2009 should be placed as close to the VGA or DVI−I connector as possible.
2. The ESD protection channels VIDEO_1, VIDEO_2, VIDEO_3 may be used interchangeably between the R, G, B signals.
3. If differential video signal routing is used, the RED, BLUE, and GREEN signal lines should be terminated with external 37.5 Ω resistors.
4. “VF” are external video filters for the RGB signals.
5. Supply bypass capacitors C1 and C2 must be placed immediately adjacent to the corresponding Vcc pins. Connections to the Vcc pins and ground plane must be made with minimal length copper traces (preferably less than 5 mm) for best ESD protection.
6. The bypass capacitor for the BYP pin has been omitted in this diagram. This results in a reduction in the maximum ESD withstand voltage at the DDC_OUT pins from ±8 kV to ±4 kV. If 8 kV ESD protection is required, a 0.2 μF ceramic bypass capacitor should be connected between BYP and ground.
7. The SYNC buffers may be used interchangeably between HSYNC and VSYNC.
8. The EMI filters at the SYNC_OUT and DDC_OUT pins (C5 to C12, and Ferrite Beads FB1 to FB4) are for reference only. The component values and filter configuration may be changed to suit the application.
9. The DDC level shifters DDC_IN, DDC_OUT, may be used interchangeably between DDCA_CLK and DDCA_DATA.
10. R1, R2 are optional. They may be used, if required, to pull the DDC_CLK and DDC_DATA lines to VCC_5V when no monitor is connected to the VGA connector. If used, it should be noted that “back current” may flow between the DDC pins and VCC_5V via these resistors when VCC_5V is powered down.
11. For optimal ESD performance with the CM2009−02, an additional clamp device (such as the CMD PACDN042) should be placed on HSYNC/VSYNC lines between the external matching resistor and the VGA connector.

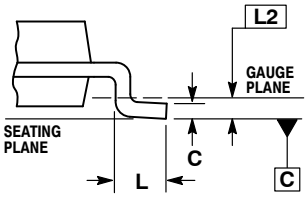


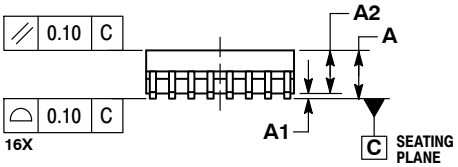
SCALE 2:1

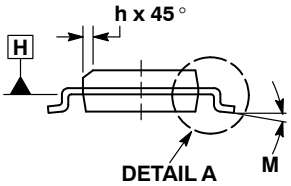
QSOP16
CASE 492−01
ISSUE A

DATE 23 MAR 2011





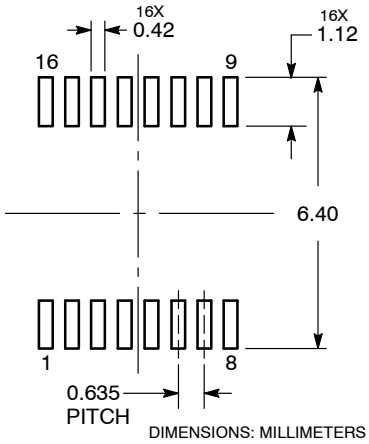




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	----	1.24	----
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.193 BSC		4.89 BSC	
E	0.237 BSC		6.00 BSC	
E1	0.154 BSC		3.90 BSC	
e	0.025 BSC		0.635 BSC	
h	0.009	0.020	0.22	0.50
L	0.016	0.050	0.40	1.27
L2	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

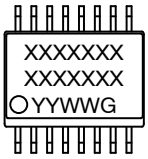
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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