Automotive Current Mode PWM Control Circuit

The CS2841B provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS2841B (a variation of the CS2843A) is designed specifically for use in automotive operation. The low start threshold voltage of 8.0 V (typ), and the ability to survive 40 V automotive load dump transients are important for automotive subsystem designs. The CS2841 series has a history of quality and reliability in automotive applications.

The CS2841B incorporates a precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. Duty-cycles greater than 50% are also possible. On board logic ensures that V_{REF} is stabilized before the output stage is enabled. Ion implant resistors provide tighter control of undervoltage lockout.

Features

- Optimized for Off-Line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty-Cycle Clamp
- V_{REF} Stabilized Before Output Stage Enabled
- Low Start-Up Current
- Pulse-By-Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1.0 % Trimmed Bandgap Reference
- High Current Totem Pole Output
- Pb-Free Packages are Available*



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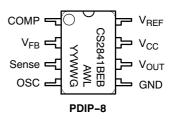


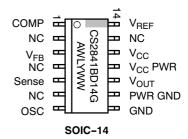
PDIP-8 N SUFFIX CASE 626



SOIC-14 D SUFFIX CASE 751A

PIN CONNECTIONS AND MARKING DIAGRAM





CS2841B = Device Code A = Assembly Location

WL = Wafer Lot
 YY, Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

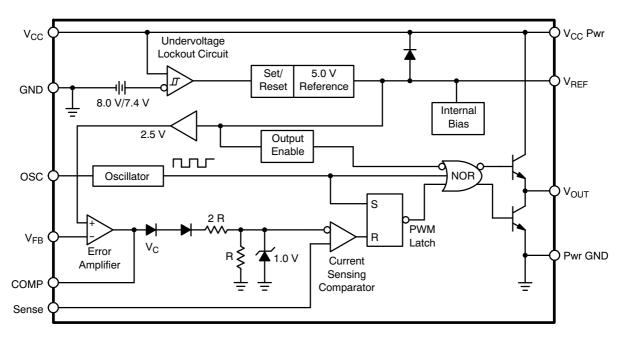


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit	
Supply Voltage (Low Impedance Source)		40	V
Output Current		±1.0	Α
Output Energy (Capacitive Load)		5.0	μЈ
Analog Inputs (V _{FB} , Sense)		-0.3 to 5.5	٧
Error Amp Output Sink Current		10	mA
·	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	ο̈́ο

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. 10 seconds max
- 2. 60 seconds max above 183°C

ORDERING INFORMATION

Device	Package	Shipping [†]
CS2841BEBN8	PDIP-8	50 Units / Rail
CS2841BEBN8G	PDIP-8 (Pb-Free)	50 Units / Rail
CS2841BED14	SOIC-14	55 Units / Rail
CS2841BED14G	SOIC-14 (Pb-Free)	55 Units / Rail
CS2841BEDR14	SOIC-14	2500 / Tape & Reel
CS2841BEDR14G	SOIC-14 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

 $\textbf{ELECTRICAL CHARACTERISTICS} \ (-40^{\circ}C \leq T_{A} \leq 85^{\circ}C, \ R_{T} = 680 \ k\Omega, \ C_{T} = 0.022 \ \mu\text{F for Triangular Mode, V}_{CC} = 15 \ V \ (\text{Note 3}), \ R_{T} = 680 \ k\Omega, \ R_{T}$ R_T = 10 k Ω , C_T = 3.3 nF for Sawtooth Mode (see Figure 7); unless otherwise specified.)

Characteristic	Test Conditions	Min	Тур	Max	Unit
Reference Section					
Output Voltage	T _J = 25°C, I _{OUT} = 1.0 mA	4.9	5.0	5.1	V
Line Regulation	8.4 ≤ V _{CC} ≤ 16 V	-	6.0	20	mV
Load Regulation	1.0 ≤ I _{OUT} ≤ 20 mA	-	6.0	25	mV
Temperature Stability	Note 4	-	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. Note 4	4.82	-	5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T _J = 25°C. Note 4	-	50	-	μV
Long Term Stability	T _A = 125°C, 1000 Hrs. Note 4	-	5.0	25	mV
Output Short Circuit	T _A = 25°C	-30	-100	-180	mA
Oscillator Section				-1	•
Initial Accuracy	Sawtooth Mode: $T_J = 25^{\circ}C$. See Figure 7. Sawtooth Mode: $-40^{\circ}C \le T_A \le +85^{\circ}C$ Triangular Mode: $T_J = 25^{\circ}C$. See Figure 7.	47 44 44	52 52 52	57 60 60	kHz kHz kHz
Voltage Stability	8.4 ≤ V _{CC} ≤ 16 V	-	0.2	1.0	%
Temperature Stability	Sawtooth Mode: $T_{MIN} \le T_A \le T_{MAX}$. Note 4 Triangular Mode: $T_{MIN} \le T_A \le T_{MAX}$. Note 4	-	5.0 8.0		% %
Amplitude	V _{OSC} (Peak to Peak)	-	1.7	-	V
Discharge Current	$T_{J} = 25^{\circ}C$ $T_{MIN} \le T_{A} \le T_{MAX}$	7.4 7.2	8.3	9.2 9.4	mA mA
Error Amp Section					
Input Voltage	V _{COMP} = 2.5 V	2.42	2.5	2.58	V
Input Bias Current	V _{FB} = 0 V	-	-0.3	-2.0	μΑ
A _{VOL}	2.0 ≤ V _{OUT} ≤ 4.0 V	65	90	-	dB
Unity Gain Bandwidth	Note 4	0.7	1.0	-	MHz
PSRR	8.4 V ≤ V _{CC} ≤ 16 V	60	70	-	dB
Output Sink Current	V _{FB} = 2.7 V, V _{COMP} = 1.1 V	2.0	6.0	-	mA
Output Source Current	V _{FB} = 2.3 V, V _{COMP} = 5.0 V	-0.5	-0.8	-	mA
V _{OUT} High	V_{FB} = 2.3 V, R_L = 15 k Ω to Ground	5.0	6.0	-	V
V _{OUT} Low	V_{FB} = 2.7 V, R_L = 15 k Ω to V_{REF}	-	0.7	1.1	V
Current Sense Section					
Gain	Notes 5 and 6	2.85	3.0	3.15	V/V
Maximum Input Signal	V _{COMP} = 5.0 V. Note 5	0.9	1.0	1.1	V
PSRR	12 V ≤ V _{CC} ≤ 25 V. Note 5	-	70	-	dB
Input Bias Current	V _{Sense} = 0 V	-	-2.0	-10	μΑ
Delay to Output	T _J = 25°C. Note 4	_	150	300	ns

$$A = \frac{\Delta V_{\mbox{COMP}}}{\Delta V_{\mbox{Sense}}}; \ 0 \le V_{\mbox{Sense}} \le 0.8 \ V.$$

Adjust V_{CC} above the start threshold before setting at 15 V
 These parameters, although guaranteed, are not 100% tested in production
 Parameter measured at trip point of latch with V_{FB} = 0
 Gain defined as:

ELECTRICAL CHARACTERISTICS ($-40^{\circ}C \le T_A \le 85^{\circ}C$, $R_T = 680 \text{ k}\Omega$, $C_T = 0.022 \text{ }\mu\text{F}$ for Triangular Mode, $V_{CC} = 15 \text{ V}$ (Note 3), $R_T = 10 \text{ k}\Omega$, $C_T = 3.3 \text{ nF}$ for Sawtooth Mode (see Figure 7); unless otherwise specified.)

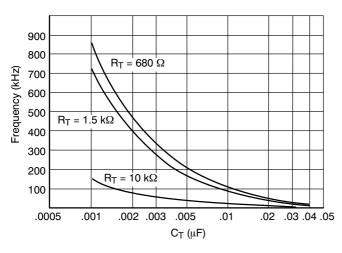
Characteristic	istic Test Conditions		Тур	Max	Unit
Output Section		•	•	•	•
Output Low Level I _{SINK} = 20 mA I _{SINK} = 200 mA		-	0.1 1.5	0.4 2.2	V V
Output High Level	I _{SOURCE} = 20 mA I _{SOURCE} = 200 mA	13 12	13.5 13.5		V V
Rise Time	T _J = 25°C, C _L = 1.0 nF. Note 7		50	150	ns
Fall Time	T _J = 25°C, C _L = 1.0 nF. Note 7	-	50	150	ns
Output Leakage	Undervoltage Active, V _{OUT} = 0	-	-0.01	-10	μΑ
Total Standby Current					
Startup Current	-	-	0.5	1.0	mA
Operating Supply Current I _{CC}	$V_{FB} = V_{Sense} = 0 \text{ V}, R_T = 10 \text{ k}\Omega, C_T = 3.3 \text{ nF}$	-	11	17	mA
Undervoltage Lockout Section			•	•	•
Start Threshold	-	7.6	8.0	8.4	V
Min. Operating Voltage	After Turn On	7.0	7.4	7.8	V
	U			1	

^{7.} These parameters, although guaranteed, are not 100% tested in production.

PACKAGE PIN DESCRIPTION

PACKA	PACKAGE PIN # PDIP-8 SOIC-14 PIN SYMBOL		
PDIP-8			FUNCTION
1	1	COMP	Error Amp Output, Used to Compensate Error Amplifier
2	3	V _{FB}	Error Amp Inverting Input
3	5	Sense	Noninverting Input to Current Sense Comparator
4	7	osc	Oscillator Timing Network with Capacitor to Ground, Resistor to V _{REF}
5	8	GND	Ground
	9	Pwr GND	Output Driver Ground
6	10	V _{OUT}	Output Drive Pin
	11	V _{CC} Pwr	Output Driver Positive Supply
7	12	V _{CC}	Positive Power Supply
8	14	V _{REF}	Output of 5.0 V Internal Reference
	2, 4, 6, 13	NC	No Connection

TYPICAL PERFORMANCE CHARACTERISTICS



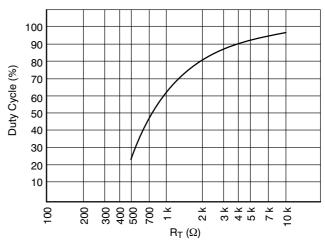


Figure 2. Oscillator Frequency vs. C_T

Figure 3. Oscillator Duty Cycle vs. R_T

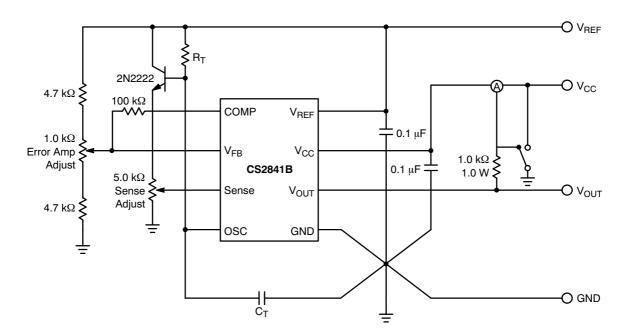


Figure 4. Test Circuit

CIRCUIT DESCRIPTION

Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.

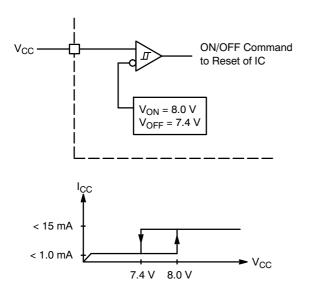


Figure 5. Typical Undervoltage Characteristics

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal representing the peak output inductor current (Figure 6). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

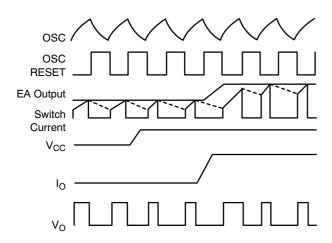
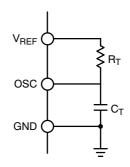
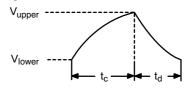


Figure 6. Timing Diagram for Key CS2841B Parameters

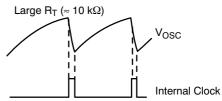
When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of OSC components.



Timing Parameters



Sawtooth Mode



Triangular Mode

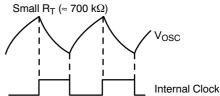


Figure 7. Oscillator Timing Network and Parameters

Setting the Oscillator

Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:

$$t_{C} = R_{T}C_{T} ln \left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}} \right)$$

$$t_{d} = R_{T}C_{T}In \left(\frac{V_{REF} - I_{d}R_{T} - V_{upper}}{V_{REF} - I_{d}R_{T} - V_{lower}} \right)$$

Substituting in typical values for the parameters in the above formulas:

$$\begin{array}{l} \text{VREF} = 5.0 \text{ V} \\ \text{Vupper} = 2.7 \text{ V} \\ \text{Vlower} = 1.0 \text{ V} \\ \text{I}_{d} = 8.3 \text{ mA} \\ \text{t}_{C} \approx 0.5534 \text{RTCT} \end{array}$$

$$t_d = R_T C_T \ln \left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

The frequency and maximum duty cycle can be determined from the Typical Performance Characteristic graphs.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND pin in a single point ground.

The transistor and 5.0 k Ω potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

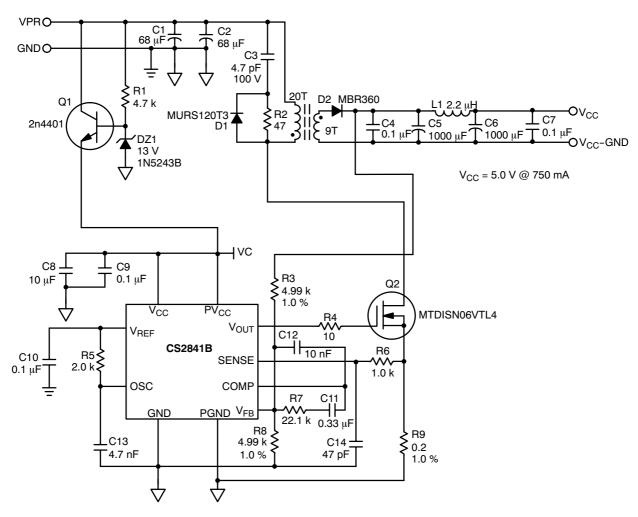


Figure 8. Flyback Application

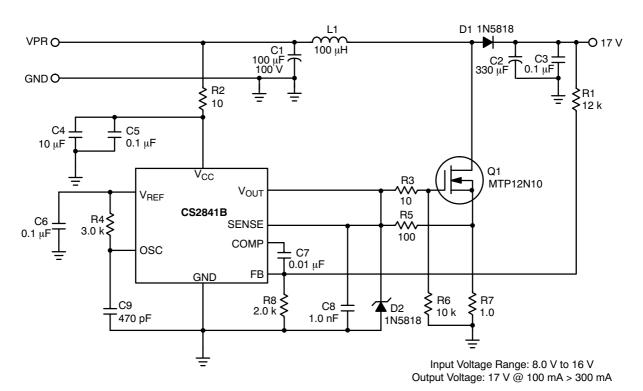


Figure 9. Boost Application

PACKAGE THERMAL DATA

Paramo	eter	PDIP-8	SOIC-14	Unit
$R_{\theta JC}$	Typical	52	30	°C/W
$R_{\theta JA}$	Typical	100	125	°C/W



PDIP-8 CASE 626-05 ISSUE P

DATE 22 APR 2015



TOP VIEW

b2

В



NOTE 5

e/2 NOTE 3 SEATING PLANE C D1 eВ 8X b **END VIEW** |⊕|0.010 M| C| A M| B M NOTE 6 SIDE VIEW

STYLE 1: PIN 1. AC IN 2. DC + IN 3. DC - IN 4. AC IN 5. GROUND 6. OUTPUT 7. AUXILIARY 8. V_{CC}

NOTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
 DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACK-
- AGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
 DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
- DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR
- 6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE
- LEADS UNCONSTRAINED.

 DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
- PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α		0.210		5.33
A1	0.015		0.38	
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060	TYP	1.52	TYP
С	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005		0.13	
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
е	0.100 BSC		2.54	BSC
eВ		0.430		10.92
L	0.115	0.150	2.92	3.81
М		10°		10°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

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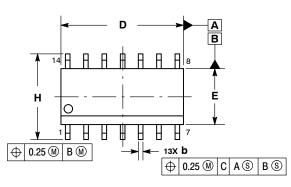




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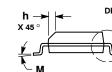
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016





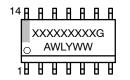




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
- MAXIMUM MATERIAL CONDITION.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
АЗ	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
e	1.27	BSC	0.050	BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
М	0 °	7°	0 °	7 °

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*

C SEATING PLANE



DIMENSIONS: MILLIMETERS

STYLES ON PAGE 2

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$

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