

MOSFET – Power, Dual, N-Channel, for 1-2 Cells Lithium-ion Battery Protection

20 V, 30 mΩ, 6 A

EFC3C001NUZ

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1–2 cells lithium–ion battery applications.

Features

- 2.5 V Drive
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb–Free, Halide Free and RoHS Compliant

Applications

- 1-2 Cells Lithium-ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

| Parameter | Symbol | Value | Unit |
|--|------------------|-------------|------|
| Source to Source Voltage | V _{SSS} | 20 | V |
| Gate to Source Voltage | V _{GSS} | ±10 | V |
| Source Current (DC) | I _S | 6 | A |
| Source Current (Pulse) PW ≤ 100 μs, duty cycle ≤ 1% | I _{SP} | 60 | A |
| Total Dissipation (Note 1) | P _T | 1.6 | W |
| Junction Temperature | T _j | 150 | °C |
| Storage Temperature | T _{stg} | –55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

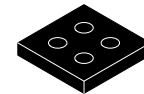
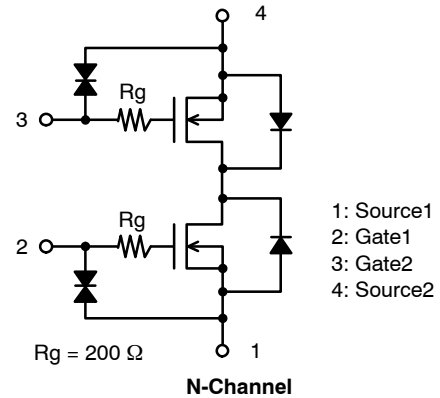
THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Value | Unit |
|------------------------------|------------------|-------|------|
| Junction to Ambient (Note 1) | R _{θJA} | 78.1 | °C/W |

1. Surface mounted on ceramic substrate (5000 mm² × 0.8 mm).

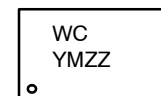
| V _{SSS} | R _{SS(on)} Max | I _S Max |
|------------------|-------------------------|--------------------|
| 20 V | 30 mΩ @ 4.5 V | 6 A |
| | 34 mΩ @ 3.8 V | |
| | 39 mΩ @ 3.1 V | |
| | 56 mΩ @ 2.5 V | |

ELECTRICAL CONNECTION



WLCSP4 1.26x1.26 /
EFCP1313–4DG–020
CASE 567LM

MARKING DIAGRAM



WC = Specific Device Code
Y = Year
M = Month
ZZ = Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|----------------------|--|------|-------|-----|------|
| Source to Source Breakdown Voltage | V _{(BR)SSS} | I _S = 1 mA, V _{GS} = 0 V (Figure 1) | 20 | – | – | V |
| Zero-Gate Voltage Source Current | I _{SSS} | V _{SS} = 20 V, V _{GS} = 0 V (Figure 1) | – | – | 1 | μA |
| Gate to Source Leakage Current | I _{GSS} | V _{GS} = ±8 V, V _{SS} = 0 V (Figure 2) | – | – | ±1 | μA |
| Gate Threshold Voltage | V _{GS(th)} | V _{SS} = 10 V, I _S = 1 mA (Figure 3) | 0.5 | – | 1.3 | V |
| Static Source to Source On-State Resistance | R _{SS(on)1} | I _S = 2 A, V _{GS} = 4.5 V (Figure 4) | 17 | 23 | 30 | mΩ |
| | R _{SS(on)2} | I _S = 2 A, V _{GS} = 3.8 V (Figure 4) | 19.5 | 26 | 34 | mΩ |
| | R _{SS(on)3} | I _S = 2 A, V _{GS} = 3.1 V (Figure 4) | 21 | 28 | 39 | mΩ |
| | R _{SS(on)4} | I _S = 2 A, V _{GS} = 2.5 V (Figure 4) | 24.5 | 35 | 56 | mΩ |
| Turn-ON Delay Time | t _{d(on)} | V _{SS} = 10 V, V _{GS} = 4.5 V, I _S = 2 A (Figure 5) | – | 50 | – | ns |
| Rise Time | t _r | | – | 350 | – | ns |
| Turn-OFF Delay Time | t _{d(off)} | | – | 42000 | – | ns |
| Fall Time | t _f | | – | 47000 | – | ns |
| Total Gate Charge | Q _g | V _{SS} = 10 V, V _{GS} = 4.5 V, I _S = 6 A (Figure 6) | – | 15 | – | nC |
| Forward Source to Source Voltage | V _{F(S-S)} | I _S = 2 A, V _{GS} = 0 V (Figure 7) | – | 0.81 | 1.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test Circuits are Example of Measuring FET1 Side

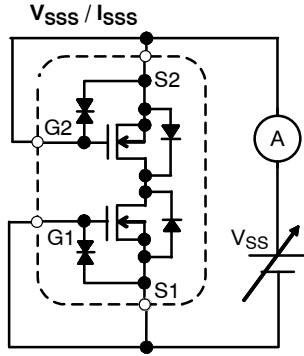


Figure 1. Test Circuit 1

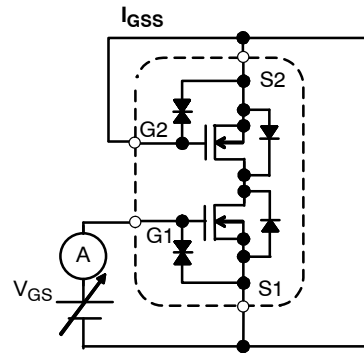
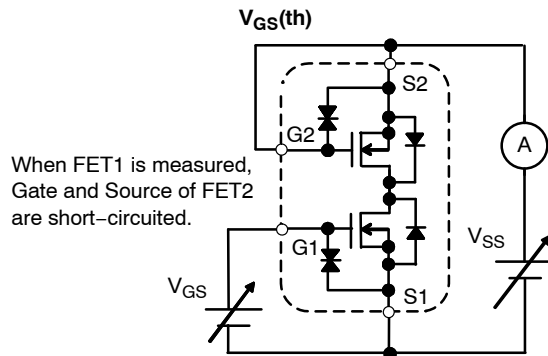


Figure 2. Test Circuit 2

When FET1 is measured, Gate and Source of FET2 are short-circuited.



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 3. Test Circuit 3

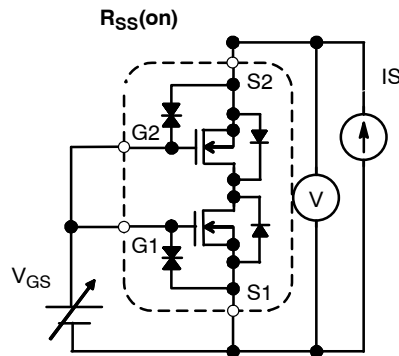
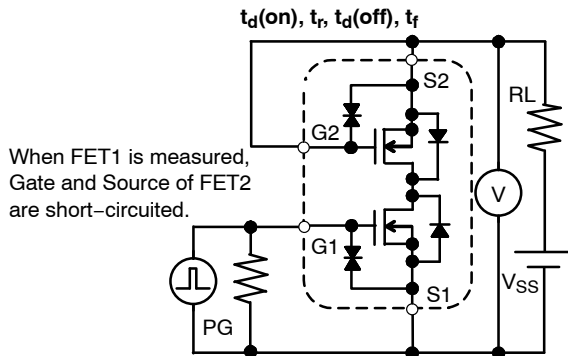
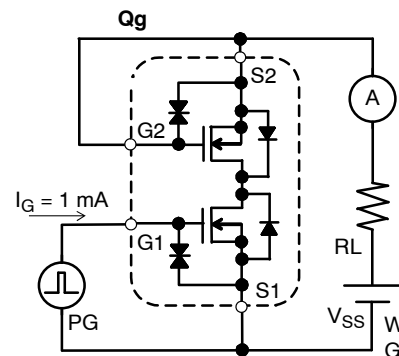


Figure 4. Test Circuit 4



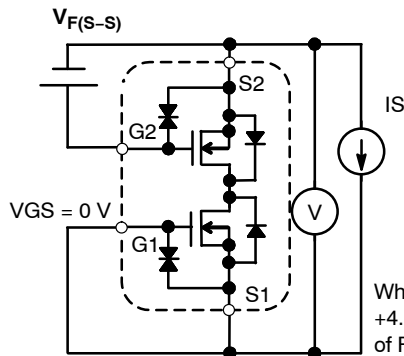
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 5. Test Circuit 5



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 6. Test Circuit 6



When FET1 is measured, +4.5 V is added to VGS of FET2.

Figure 7. Test Circuit 7

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

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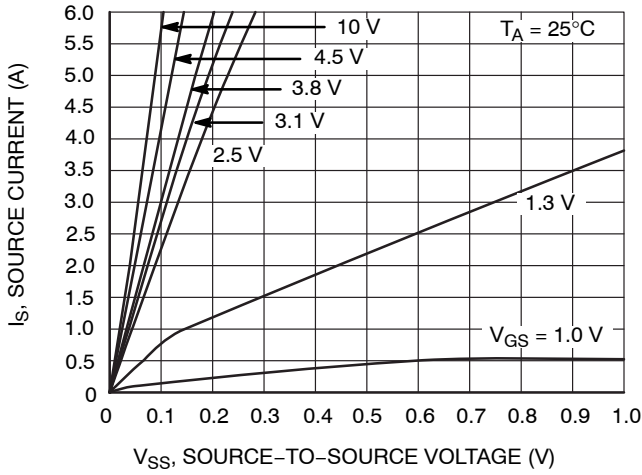


Figure 8. $I_S - V_{SS}$

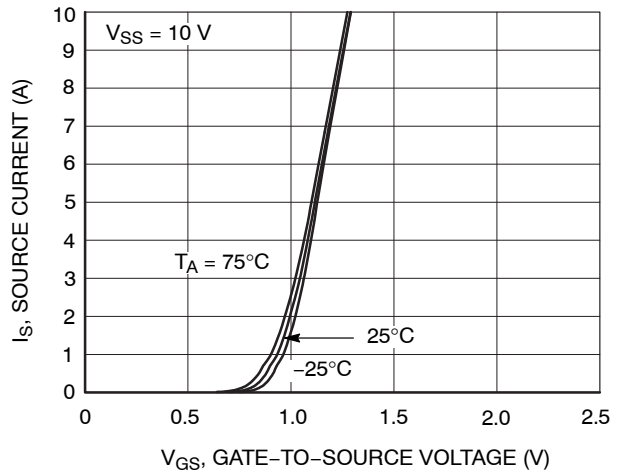


Figure 9. $I_S - V_{GS}$

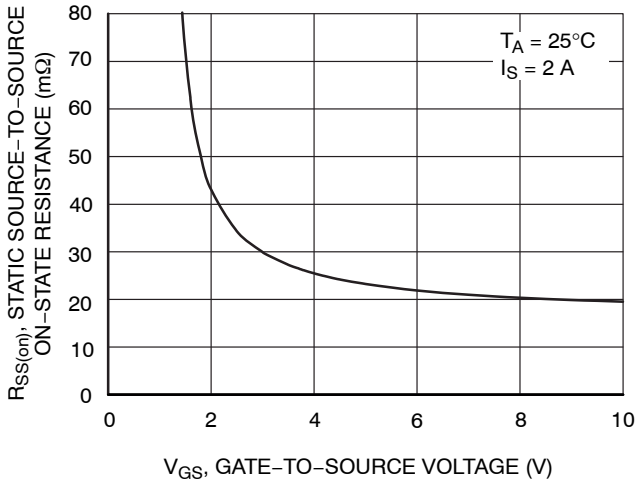


Figure 10. $R_{SS(on)} - V_{GS}$

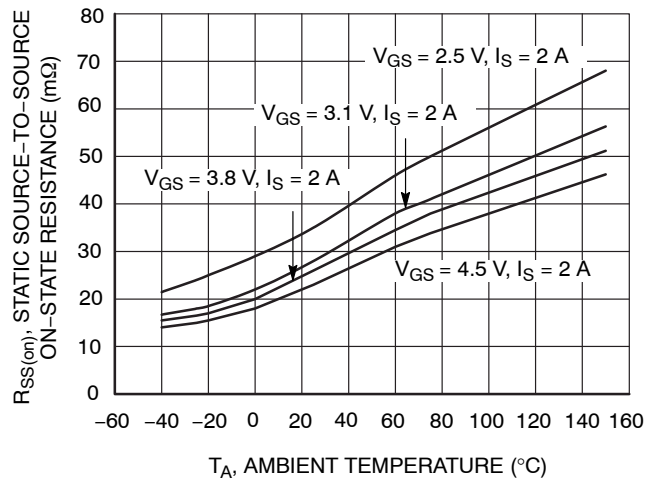


Figure 11. $R_{SS(on)} - T_a$

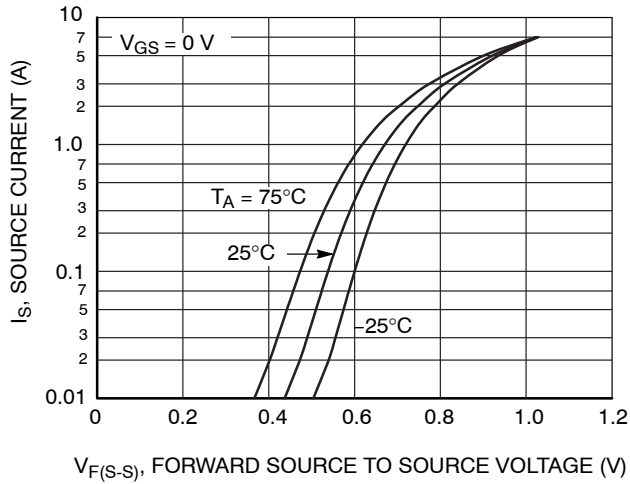


Figure 12. $I_S - V_{F(S-S)}$

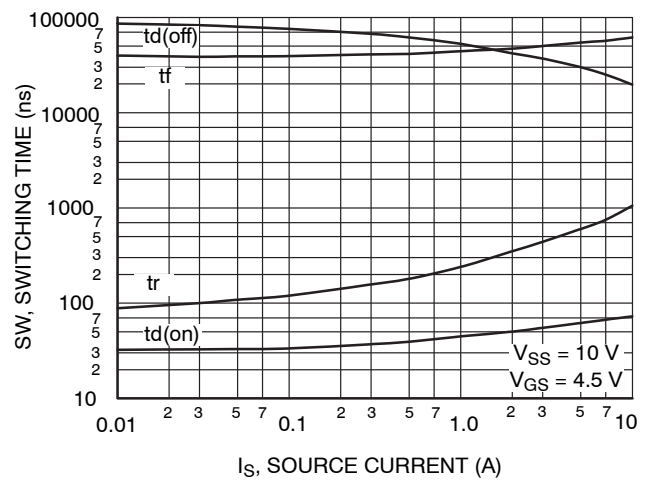


Figure 13. SW Time - I_S

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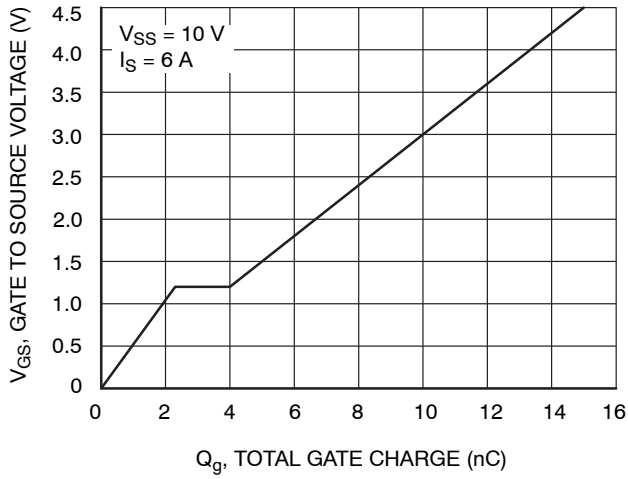


Figure 14. $V_{GS} - Q_g$

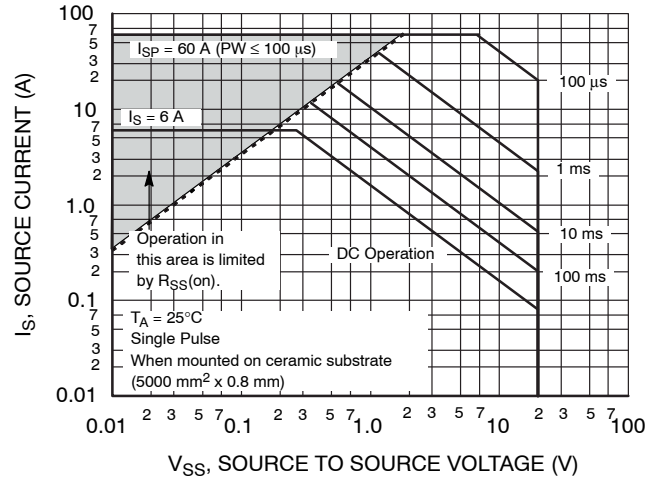


Figure 15. SOA

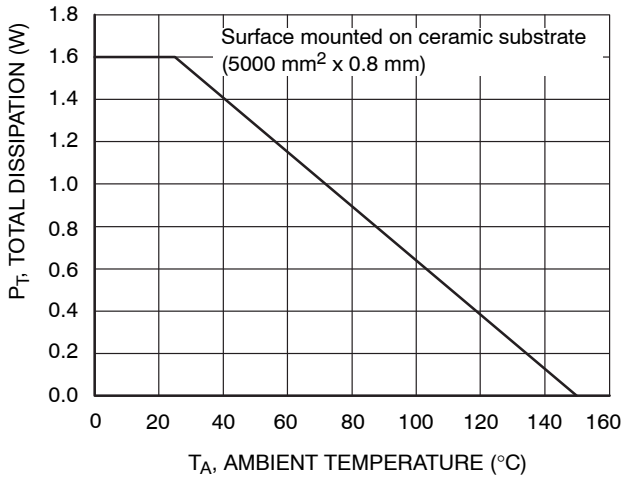


Figure 16. $P_T - T_a$

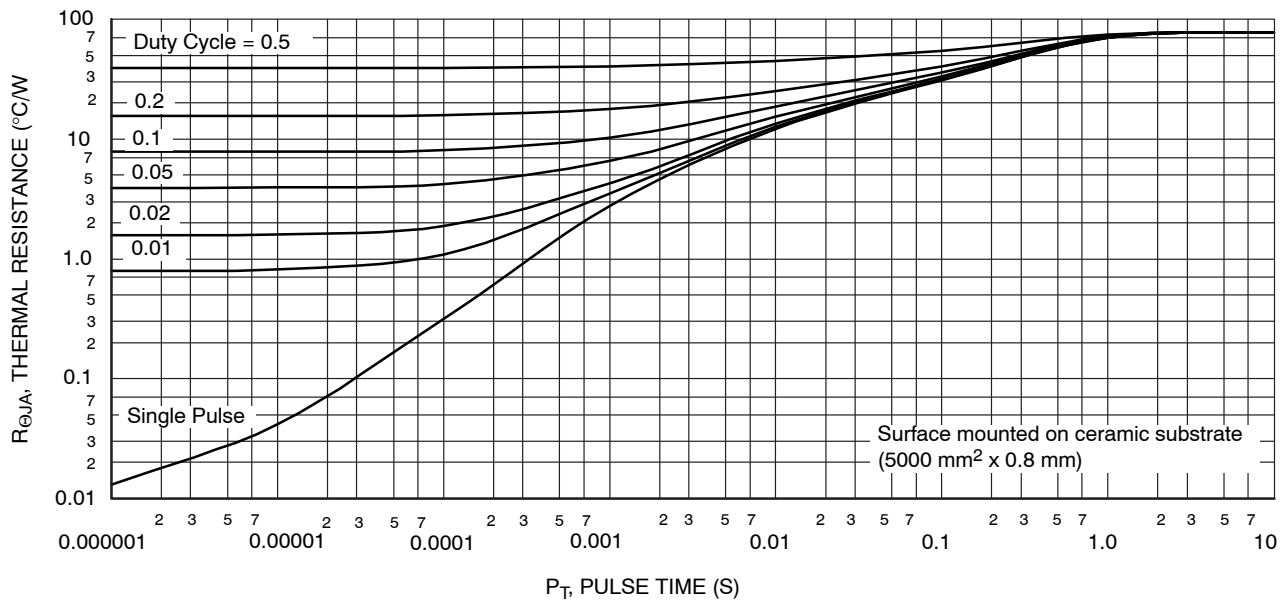


Figure 17. $R_{\theta JA} - \text{Pulse Time}$

EFC3C001NUZ

ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] (Qty / Packing) |
|----------------|---------|---|---------------------------------------|
| EFC3C001NUZTCG | WC | WLCSP4, 1.26 x 1.26 / EFCP1313-4DG-020 (Pb-Free / Halogen Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

Note on usage: Since the EFC3C001NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

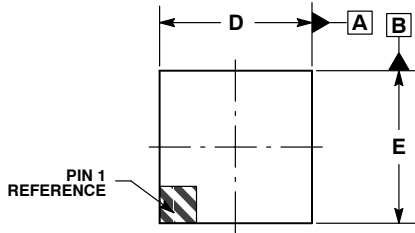
ON Semiconductor®



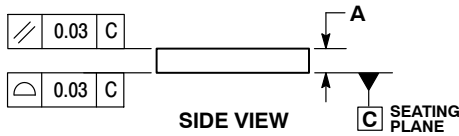
SCALE 4:1

WLCSP4 1.26x1.26 / EFCP1313-4DG-020
CASE 567LM
ISSUE O

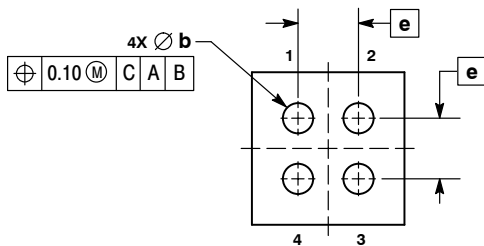
DATE 10 APR 2015



TOP VIEW



SIDE VIEW



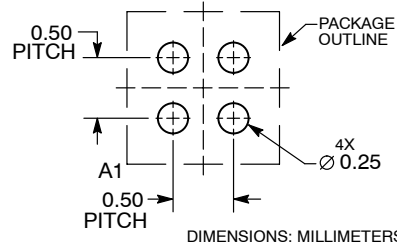
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.18 | 0.22 |
| b | 0.22 | 0.28 |
| D | 1.21 | 1.31 |
| E | 1.21 | 1.31 |
| e | 0.50 BSC | |

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|-------------------------|--|--|
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