ESD8024

ESD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD8024 surge protection is designed specifically to protect Low Voltage Differential Signals (LVDS) for LCD panels. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive data lines. The integrated 24 lines of protection offers a simplified solution with premier performance for LVDS applications.

Features

- Full Function LVDS Solution
- 4 pF Max, I/O to GND
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (ESD) ±8 kV (Contact)
  IEC61000−4−5 (Lightning) 20 A (8/20 μs)
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- LVDS
- LCD Panel TCON

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±30 ±30	kV kV
Maximum Peak Pulse Current 8/20 μs @ T_A = 25°C	I_{pp}	20	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

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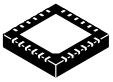


QFN24
CASE 485L

MARKING DIAGRAM

8024 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
ESD8024MNTAG	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

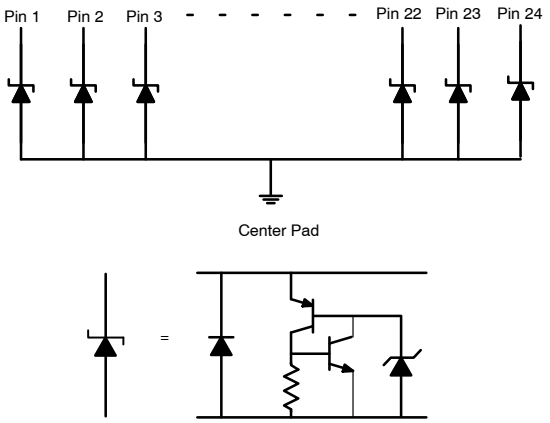
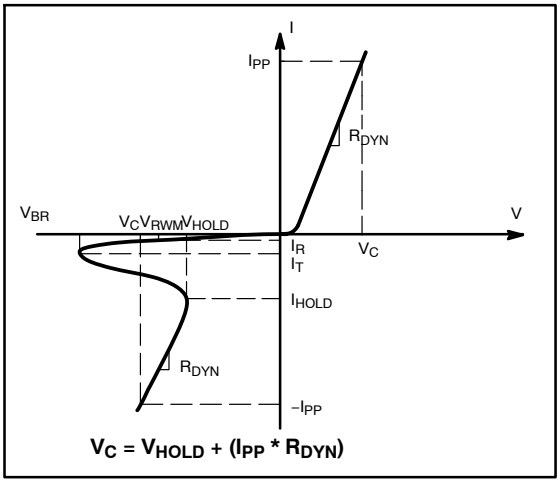


Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	All Pins (1−24) to GND (Note 1)			2.5	V
Forward Voltage	V_F	I_F = 10 mA, GND to All Pins (1−24)	0.5	0.85	1.1	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, All Pins (1−24) to GND	5.5	7.0	9.0	V
Reverse Leakage Current	I_R	V_{RWM} = 2.5 V, All Pins (1−24) to GND			0.5	μA
Holding Reverse Voltage	V_{HOLD}	I/O Pin to GND	1	1.5		V
Holding Reverse Current	I_{HOLD}	I/O Pin to GND		50		mA
Clamping Voltage	V_C	I_{PP} = 1 A, All Pins (1−24) to GND (8/20 μs pulse)			4.0	V
Clamping Voltage	V_C	I_{PP} = 10 A, All Pins (1−24) to GND (8/20 μs pulse)			7.0	V
Clamping Voltage	V_C	I_{PP} = 15 A, All Pins (1−24) to GND (8/20 μs pulse)			8.0	V
Clamping Voltage	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 2 and 3			V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins			2.0	pF
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND			4.0	pF

1. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.

TYPICAL CHARACTERISTICS

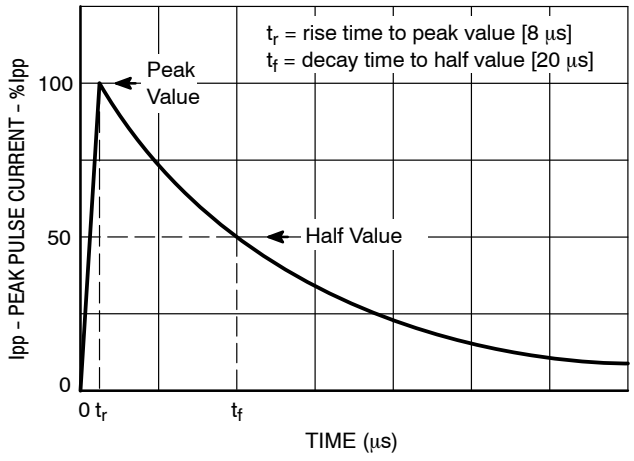


Figure 2. IEC61000−4−5 8/20 μs Pulse Waveform

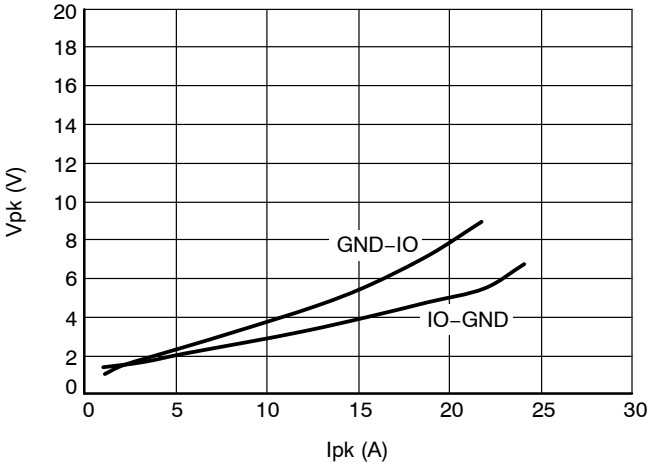


Figure 3. Clamping Voltage vs. Peak Pulse Current (tp = 8/20 μs per Figure 2)

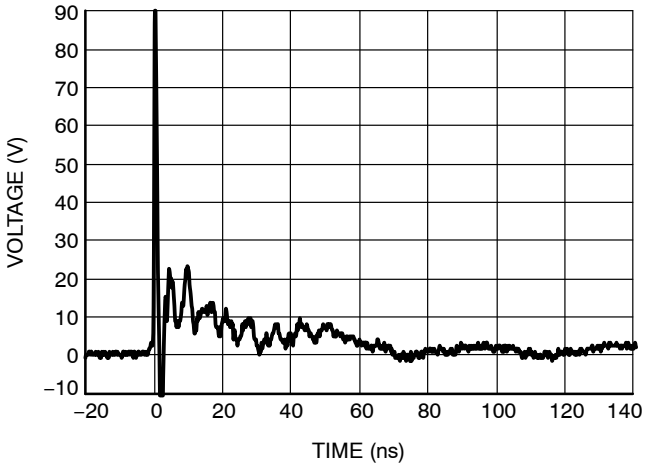


Figure 4. IEC61000−4−2 + 8 kV Contact Clamping Voltage

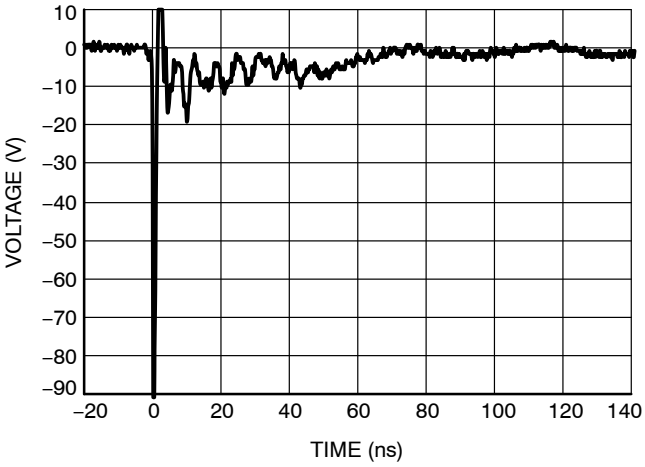


Figure 5. IEC61000−4−2 − 8 kV Contact Clamping Voltage

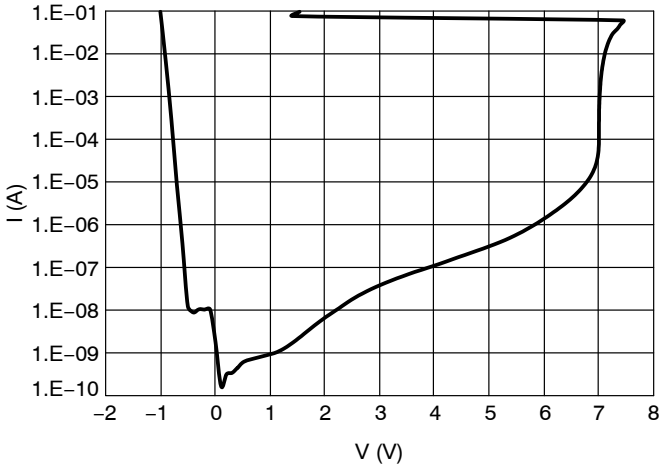


Figure 6. IV Characteristics

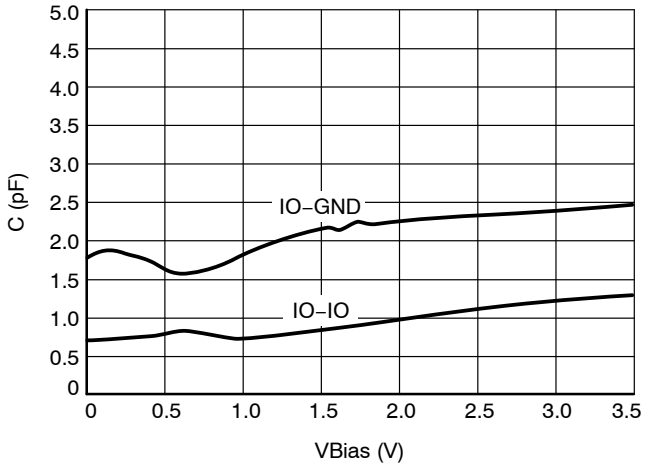


Figure 7. CV Characteristics

TYPICAL CHARACTERISTICS

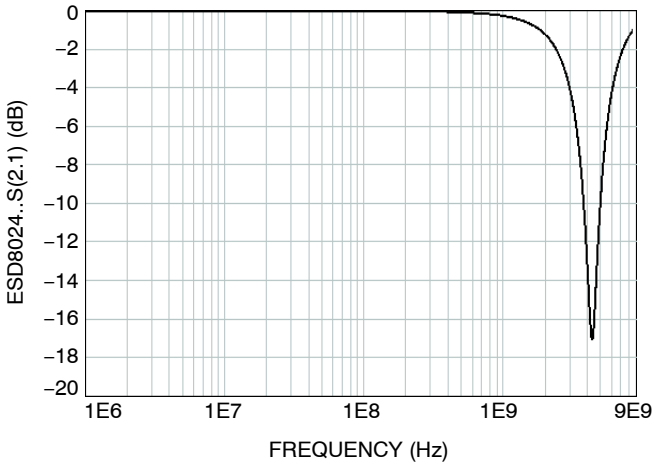


Figure 8. RF Insertion Loss

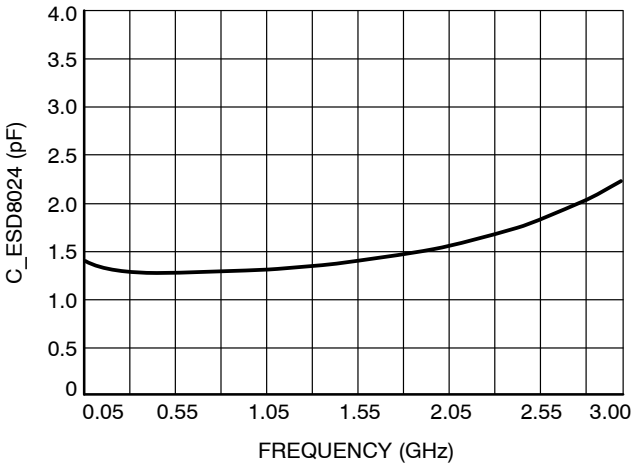


Figure 9. Capacitance over Frequency

PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the protection device in order to ensure the maximum survivability and signal integrity for the application. Such steps are listed below.

- Place the protection device as close as possible to the I/O connector to reduce the transient path to ground and improve the protection performance.
  - Consequently, place the device under protection as far as possible from the protection device to help further improve protection performance.
- Keep trace lengths connecting protection device pins to data lines as short as possible. These “stub” traces, if long enough, can create voltage drops that impede the turn-on of the protection device.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - Use curved traces when possible to avoid unwanted reflections.
  - Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

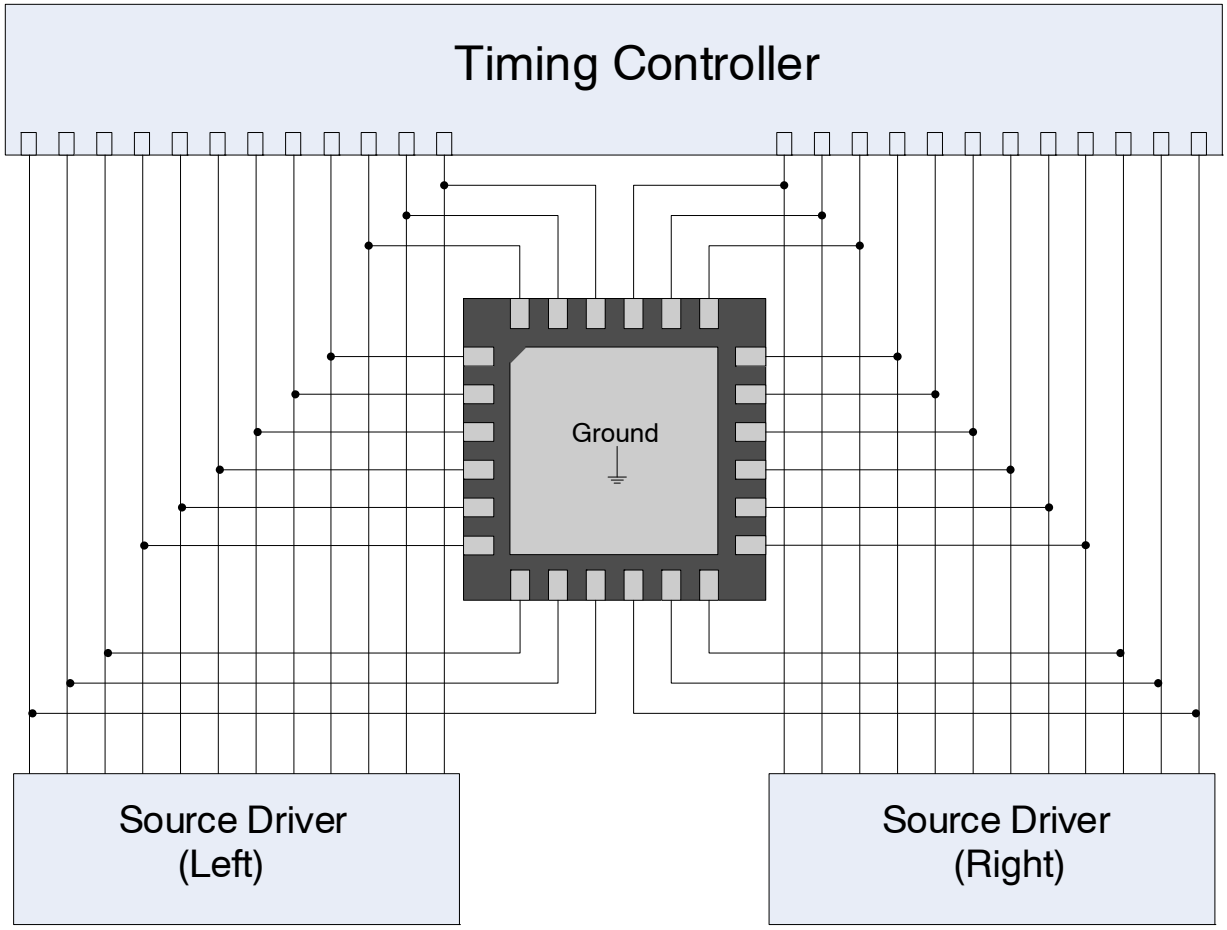
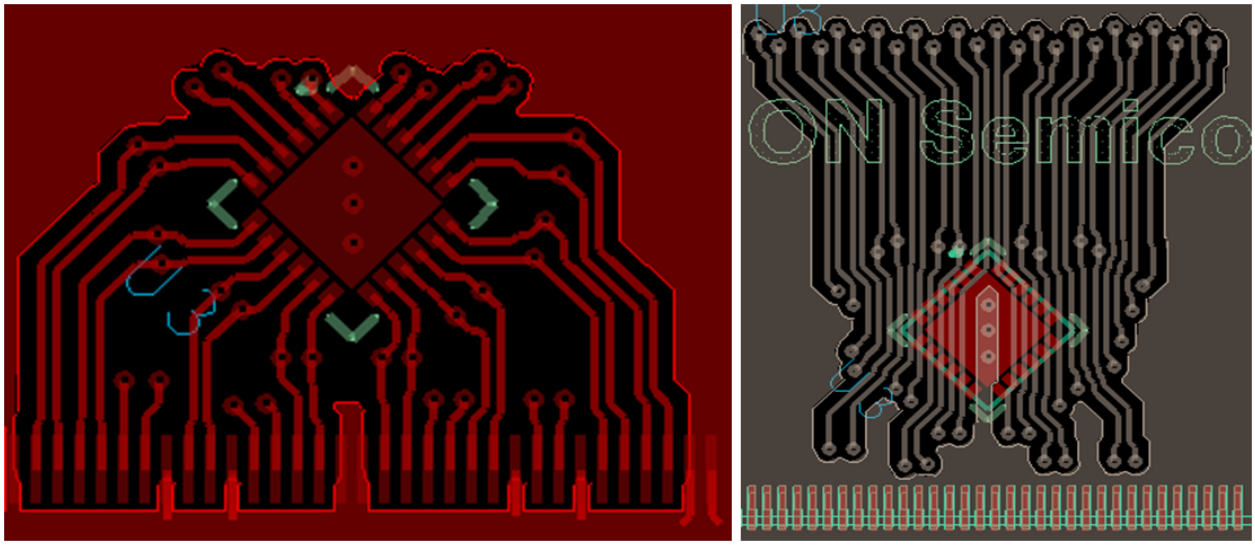


Figure 10. Board Routing Diagram – TCON LVDS Interface

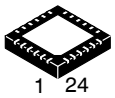


Top Layer Routing **Bottom Layer Routing**

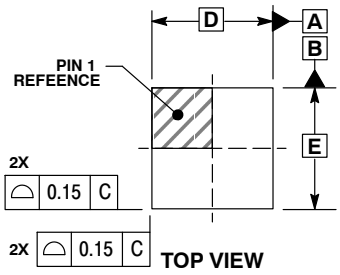
Figure 11. ESD8024 Recommended PCB Layout

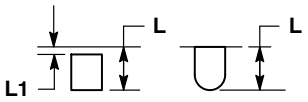
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

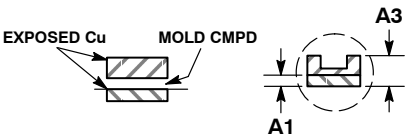


SCALE 2:1

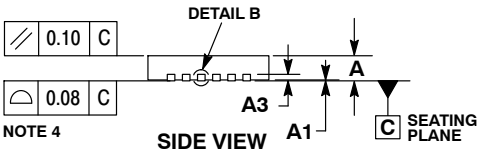


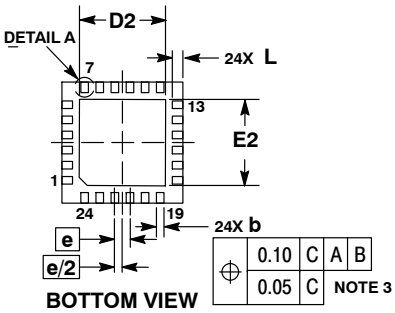


DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE TERMINAL CONSTRUCTIONS

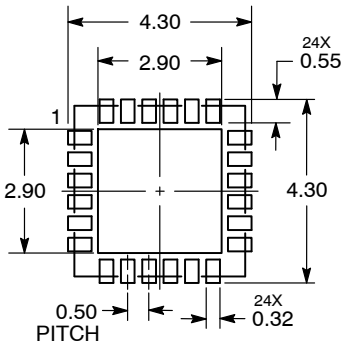




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN24, 4X4, 0.5P**		**PAGE 1 OF 1**

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