

# ESD Protection Diode

## Low Capacitance Array for High Speed Data Lines

### ESD8104

The ESD8104 is designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0/3.1 and HDMI 2.0.

#### Features

- Low Capacitance (0.37 pF Max, I/O to GND)
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- USB 3.0/3.1
- eSATA
- HDMI 1.3/1.4/2.0
- DisplayPort

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

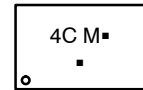
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

#### MARKING DIAGRAM



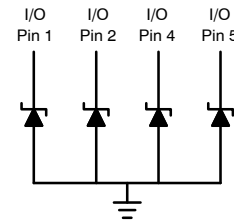
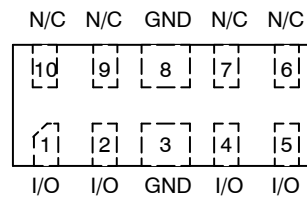
UDFN10  
CASE 517BB



- 4C = Specific Device Code (tbd)
- M = Date Code
- = Pb-Free Package

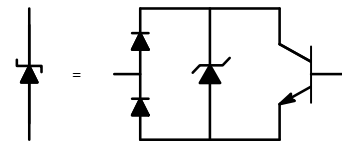
(Note: Microdot may be in either location)

#### PIN CONFIGURATION AND SCHEMATIC



Pins 3, 8

Note: Common GND - Only Minimum of 1 GND connection required



#### ORDERING INFORMATION

Device	Package	Shipping
ESD8104MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel
SZESD8104MUTAG	UDFN10 (Pb-Free)	3000 / Tape & Reel

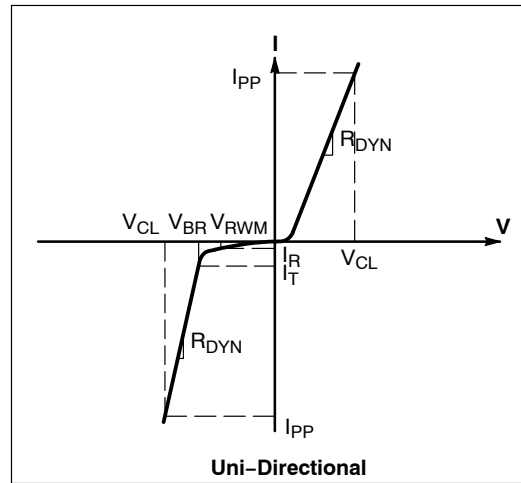
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$R_{DYN}$	Dynamic Resistance

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	I/O Pin to GND			3.3	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ , I/O Pin to GND	4.0	5.0		V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3\text{ V}$ , I/O Pin to GND			1.0	$\mu\text{A}$
Clamping Voltage (Note 1)	$V_C$	IEC61000-4-2, $\pm 8\text{ kV}$ Contact	See Figures 1 and 2			V
Clamping Voltage TLP (Note 2) See Figures 5 through 8	$V_C$	$I_{PP} = 8\text{ A}$ $I_{PP} = -8\text{ A}$	IEC 61000-4-2 Level 2 equivalent ( $\pm 4\text{ kV}$ Contact, $\pm 4\text{ kV}$ Air)		8.5 -4.5	V
		$I_{PP} = 16\text{ A}$ $I_{PP} = -16\text{ A}$	IEC 61000-4-2 Level 4 equivalent ( $\pm 8\text{ kV}$ Contact, $\pm 15\text{ kV}$ Air)		11.4 -8.0	
Dynamic Resistance	$R_{DYN}$	I/O Pin to GND GND to I/O Pin		0.36 0.44		$\Omega$
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins and GND $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins $V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = 65^\circ\text{C}$ between I/O Pins and GND		0.30 0.15 0.37	0.37 0.20 0.47	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see Figures 3 and 4 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions:  $Z_0 = 50\ \Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 4\text{ ns}$ , averaging window;  $t_1 = 30\text{ ns}$  to  $t_2 = 60\text{ ns}$ .

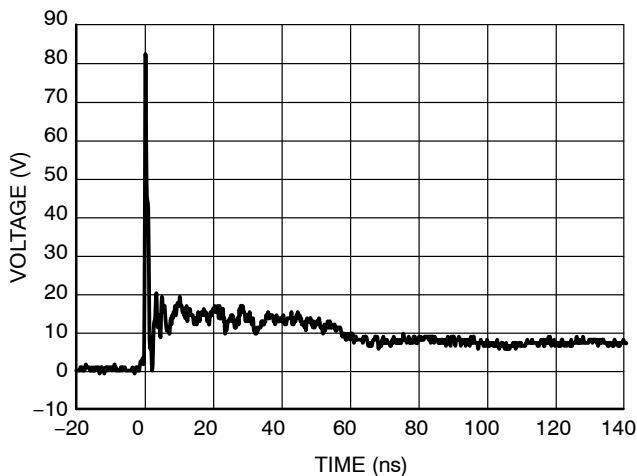


Figure 1. IEC61000-4-2 +8 kV Contact Clamping Voltage

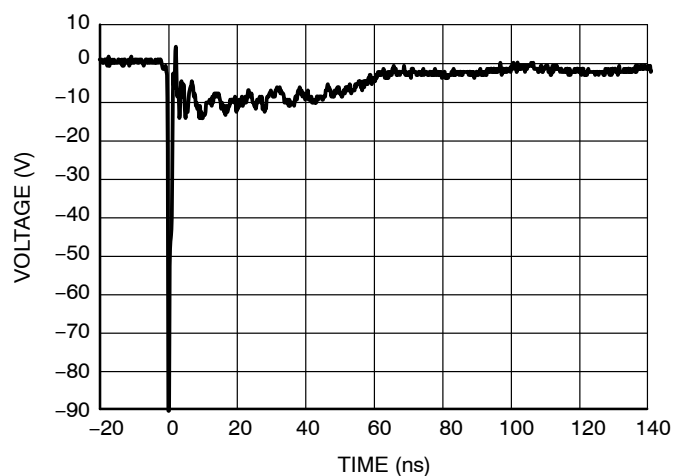


Figure 2. IEC61000-4-2 -8 kV Contact Clamping Voltage

# ESD8104

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 3. IEC61000-4-2 Spec

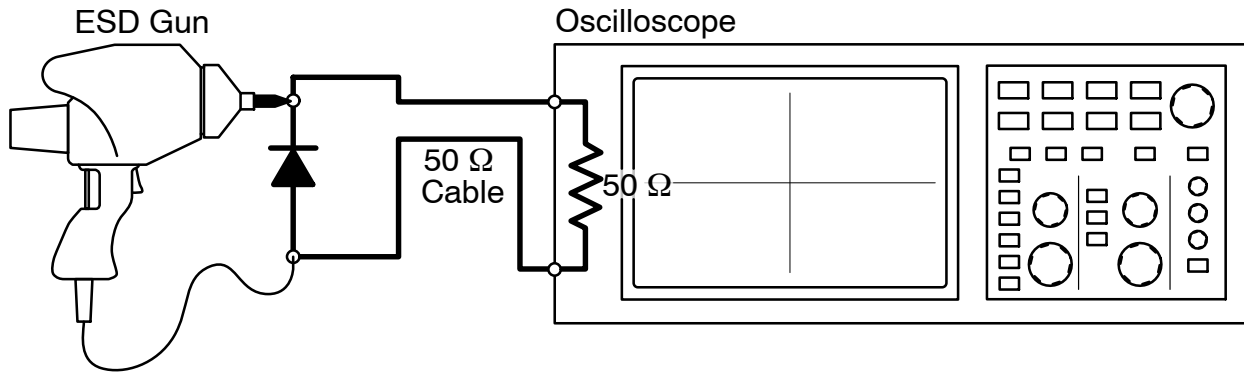


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D – Characterization of ESD Clamping Performance.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

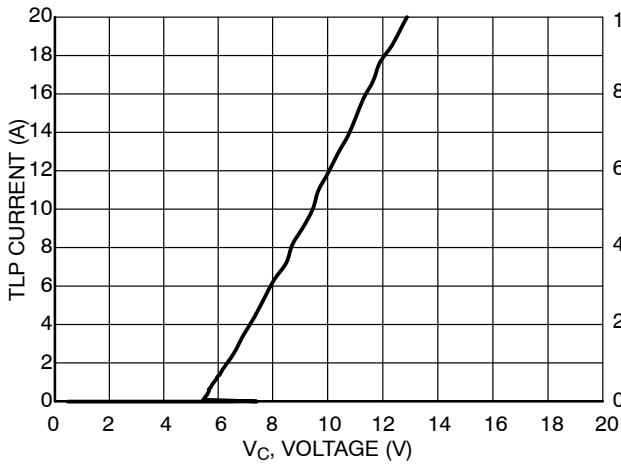


Figure 5. Positive TLP I-V Curve

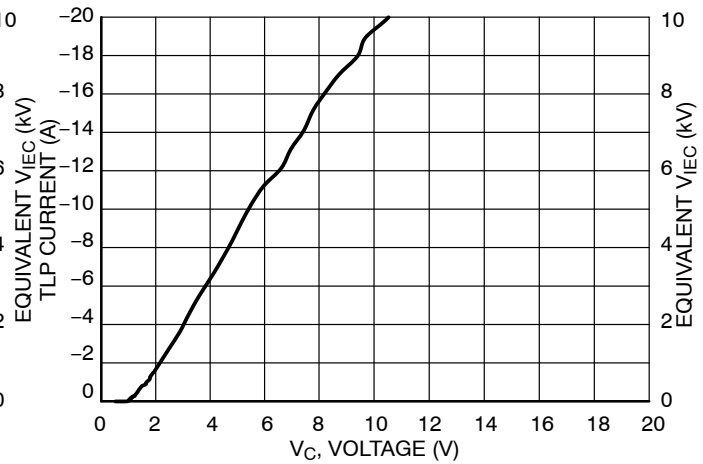


Figure 6. Negative TLP I-V Curve

NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .  $V_{IEC}$  is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at  $t = 30 \text{ ns}$  with  $2 \text{ A/kV}$ . See TLP description below for more information.

**Transmission Line Pulse (TLP) Measurement**

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

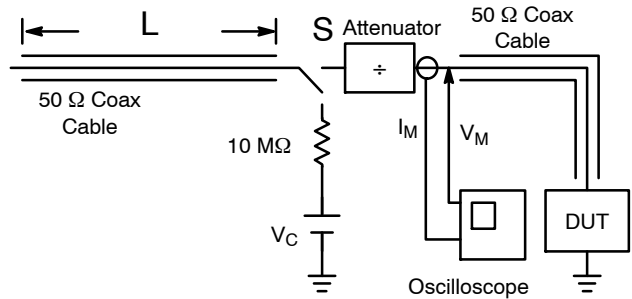


Figure 7. Simplified Schematic of a Typical TLP System

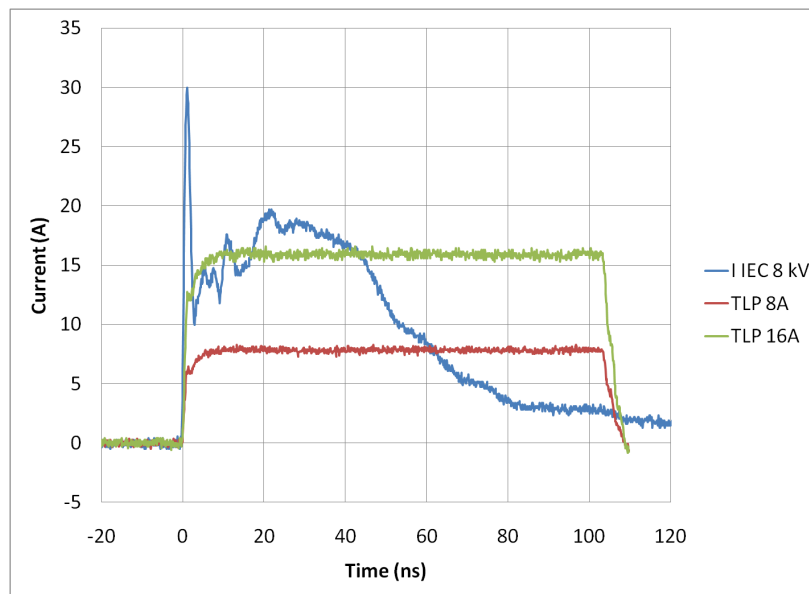
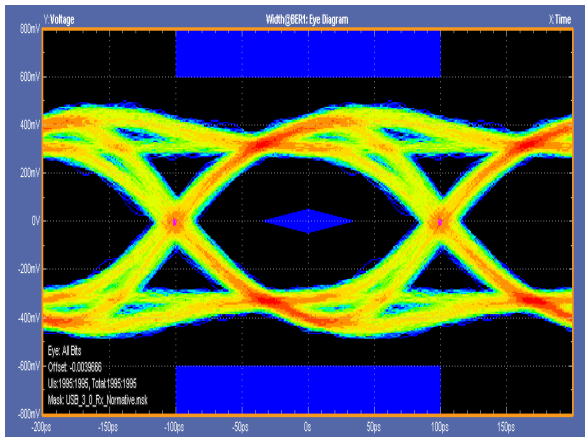
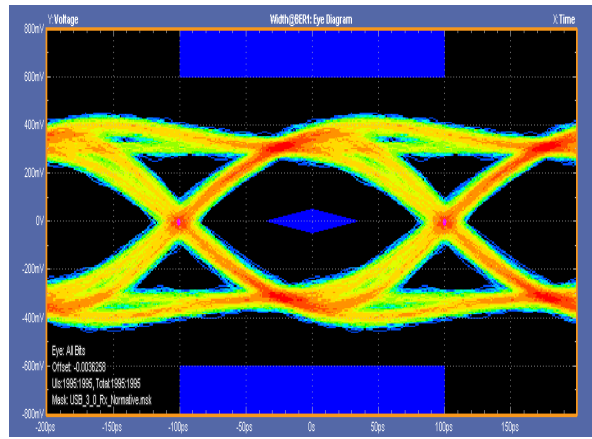


Figure 8. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# ESD8104

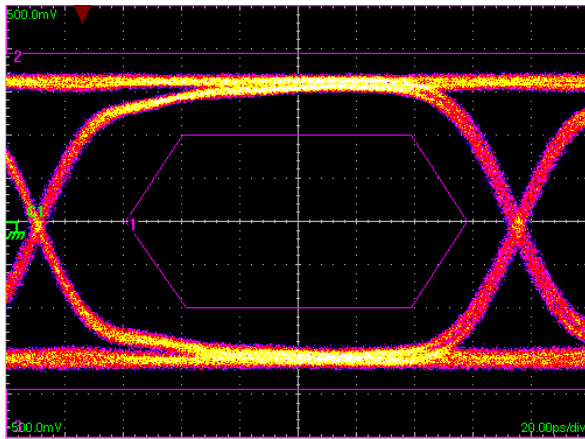


Without ESD8104

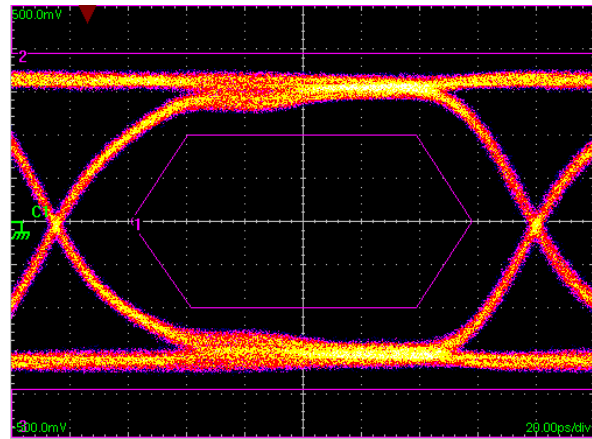


With ESD8104

Figure 9. USB 3.0 Eye Diagram with and without ESD8104. 5 Gb/s

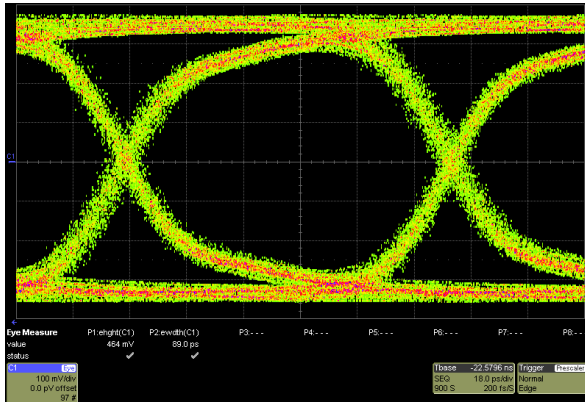


Without ESD8104

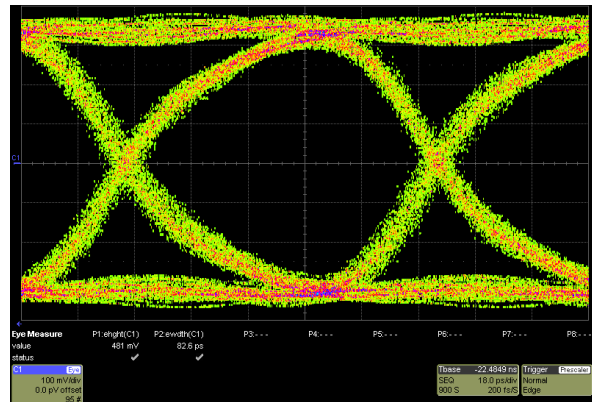


With ESD8104

Figure 10. HDMI 2.0 Eye Diagram with and without ESD8104. 6 Gb/s



Without ESD8104



With ESD8104

Figure 11. USB 3.1 Eye Diagram with and without ESD8104. 10 Gb/s

See application note AND9075/D for further description of eye diagram testing methodology.

# ESD8104

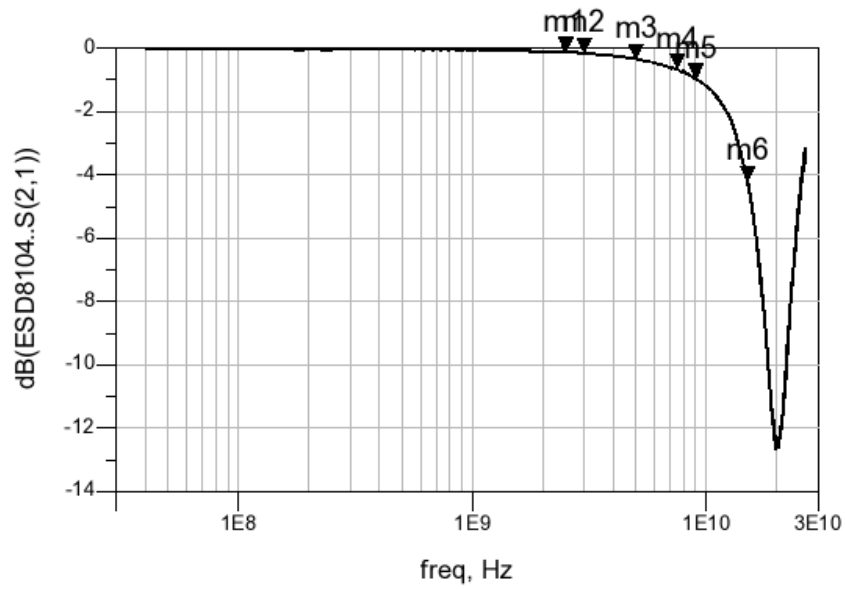


Figure 12. RF Insertion Loss

Table 1. RF INSERTION LOSS: APPLICATION DESCRIPTION

Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3 <sup>rd</sup> Harmonic Frequency (GHz)	ESD8104 Insertion Loss (dB)
USB 3.0	5.0	2.5 (m1)	7.5 (m4)	m1 = 0.128 m2 = 0.155 m3 = 0.352 m4 = 0.659 m5 = 0.958 m6 = 4.194
HDMI 2.0	6.0	3.0 (m2)	9.0 (m5)	
USB 3.1	10	5.0 (m3)	15 (m6)	

# ESD8104

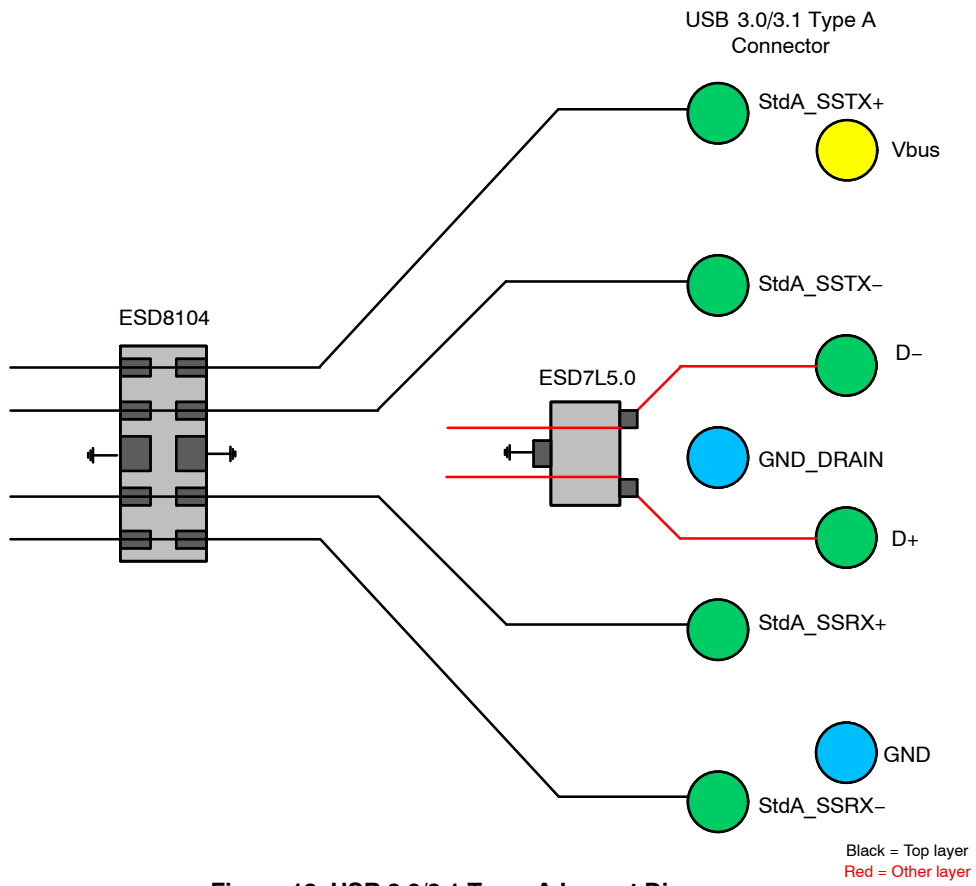


Figure 13. USB 3.0/3.1 Type-A Layout Diagram

# ESD8104

## Type-C Hybrid Top Mount Connector Top Layer



## Type-C Hybrid Top Mount Connector Bottom Layer

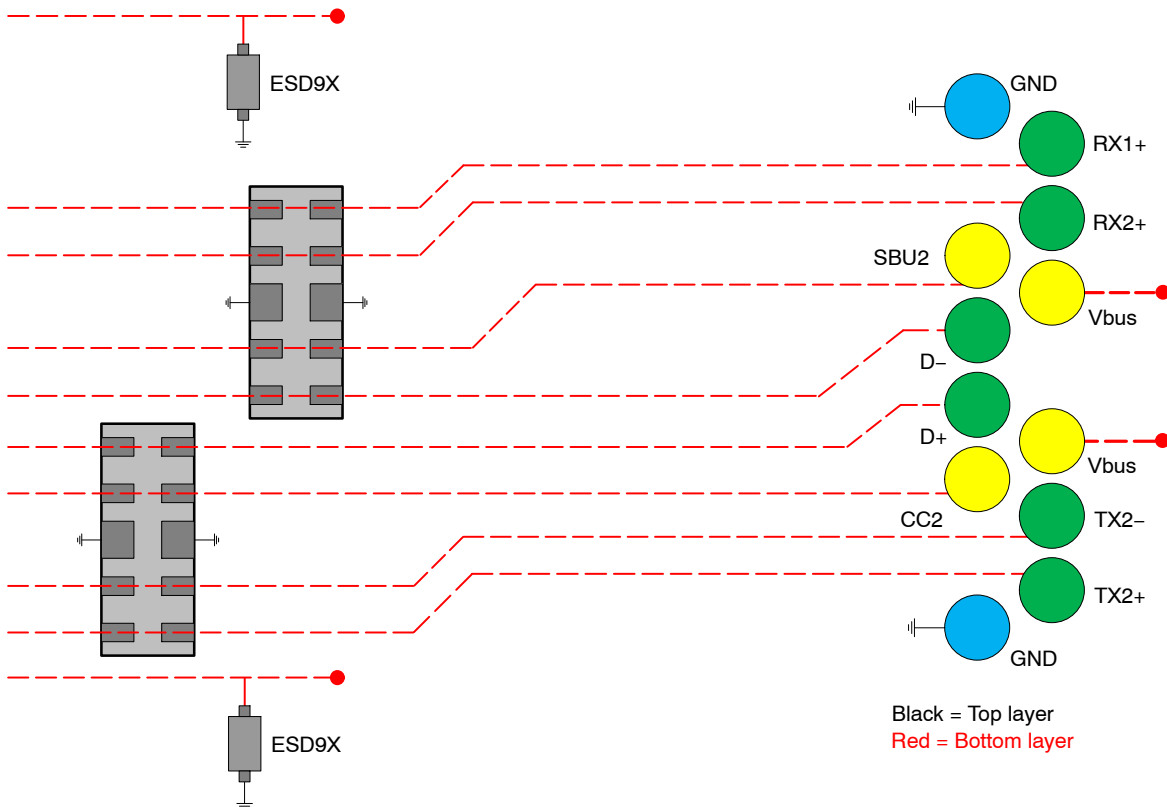
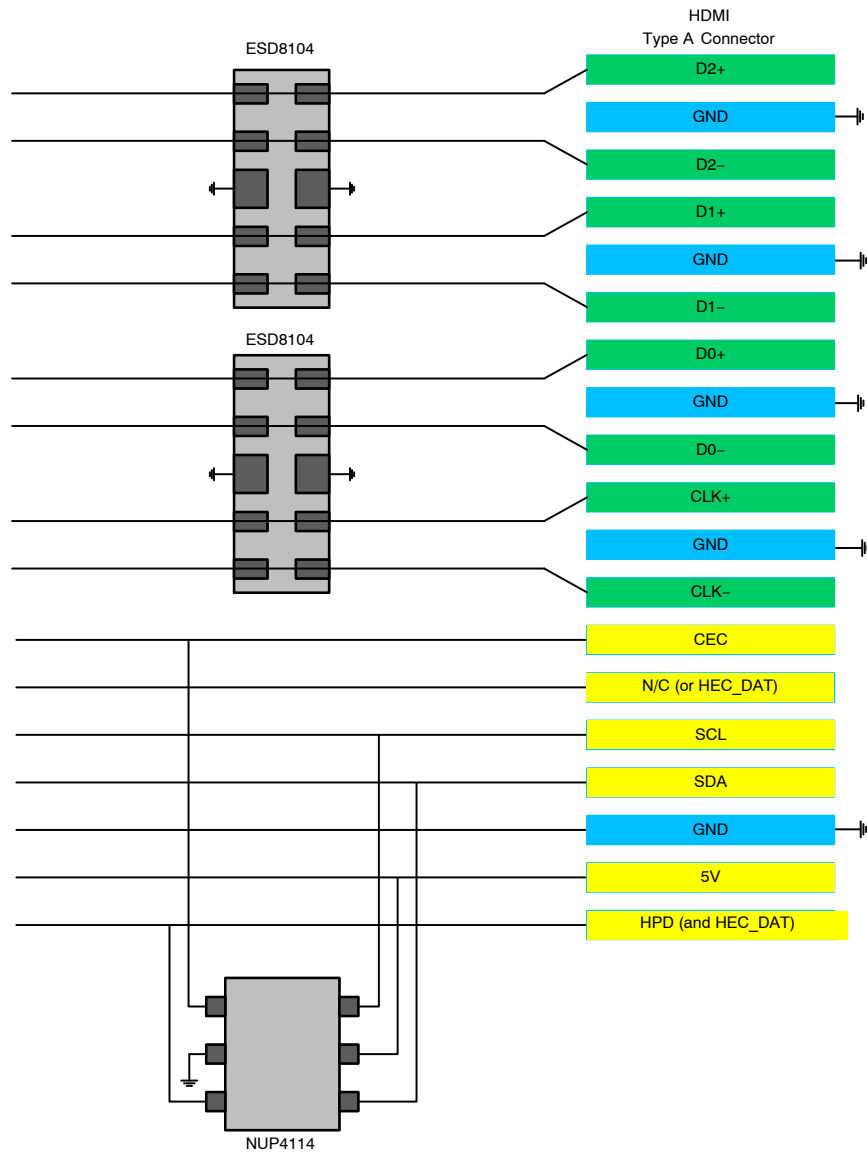


Figure 14. USB 3.1 Type-C Layout Diagram



# ESD8104



**Figure 15. HDMI Layout Diagram**

## ESD8104

### PCB Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
  - ◆ In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in Figure 16.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
  - ◆ Use curved traces when possible to avoid unwanted reflections.
  - ◆ Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
  - ◆ Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

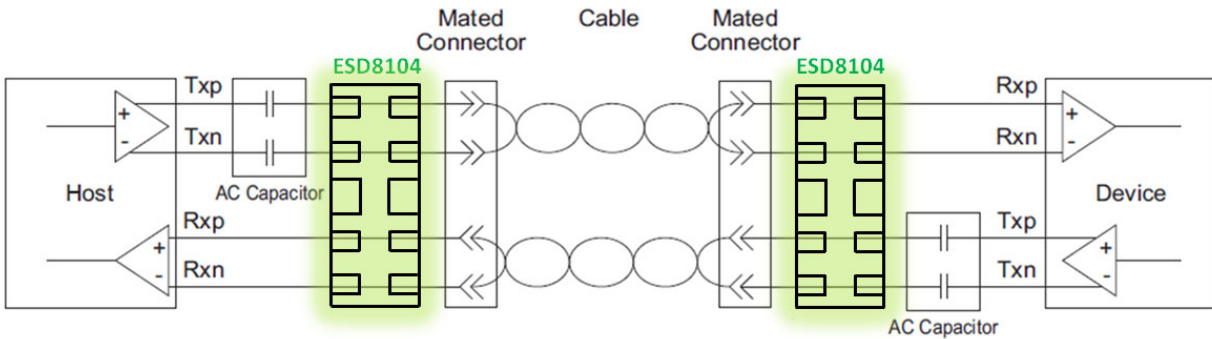


Figure 16. USB 3.0/3.1 Connection Diagram

# ESD8104

## ESD Protection Device Technology

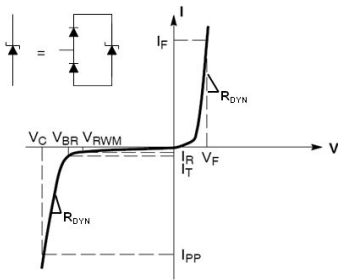
onsemi's portfolio contains three main technologies for low capacitance ESD protection device which are highlighted below and in Figure 17.

- ESD7000 series: Zener diode based technology. This technology has a higher breakdown voltage (VBR) limiting it to protecting chipsets with larger geometries.
- ESD8000 series: Silicon controlled rectifier (SCR) type technology. The key advantage for this technology is a low holding voltage (VH) which produces a deeper snapback that results in lower voltage over high

currents as shown in the TLP results in Figure 18. This technology provides optimized protection for chipsets with small geometries against thermal failures resulting in chipset damage (also known as "hard failures").

- ESD8100 series: Low voltage punch through (LVPT) type technology. The key advantage for this technology is a very low turn-on voltage as shown in Figure 19. This technology provides optimized protection for chipsets with small geometries against recoverable failures due to voltage peaks (also known as "soft failures").

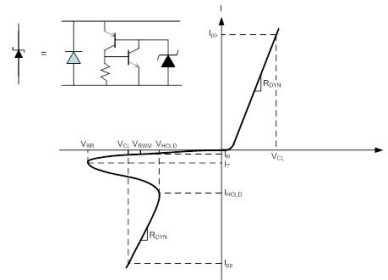
ON Semi ESD7000 series  
(Zener based ESD protection)



$$V_c = V_{BR} + I_{pp} \times R_{DYN}$$

Zener based technology has higher Vbr limiting it to chipsets greater than 45nm

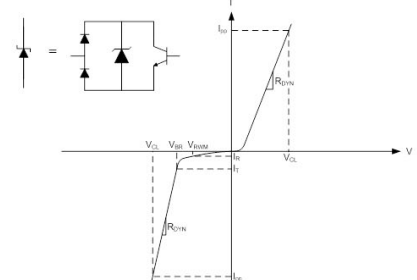
ON Semi ESD8000 series  
(SCR based ESD protection)  
Protects chipsets < 45nm



$$V_c = V_{HOLD} + I_{pp} \times R_{DYN}$$

SCR technology's key advantage is low Vhold. Deeper snapback results in lower voltage over high currents.

ON Semi ESD8100 series  
(LVPT based ESD protection)  
Protects chipsets < 45nm



$$V_c = V_{BR} + I_{pp} \times R_{DYN}$$

LVPT technology's key advantage is very low turn on voltage

Figure 17. onsemi's Low-cap ESD Technology Portfolio

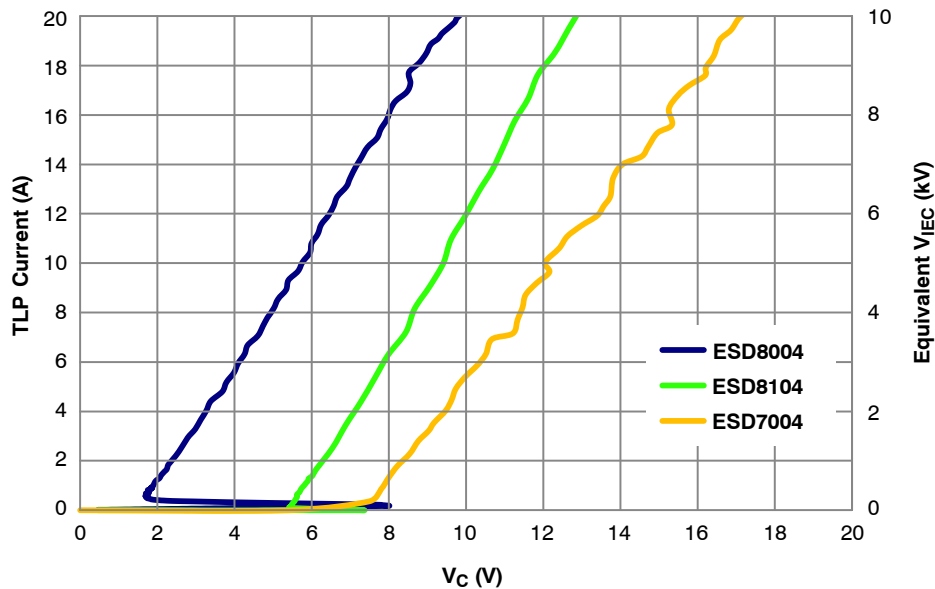


Figure 18. High Current, TLP, IV Characteristic of Each Technology

# ESD8104

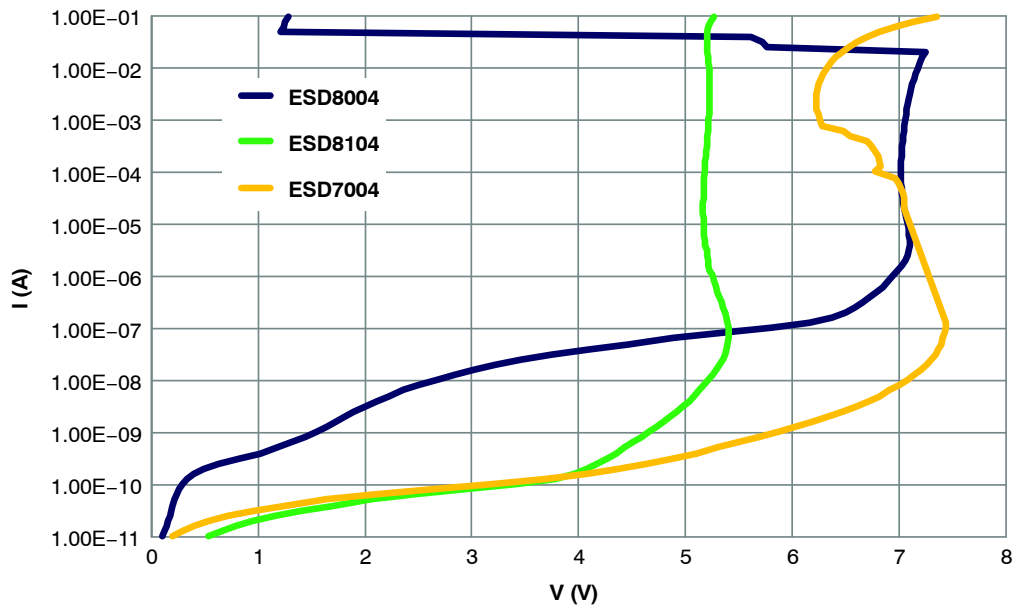


Figure 19. Low Current, DC, IV Characteristic of Each Technology

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

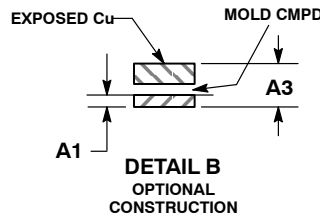
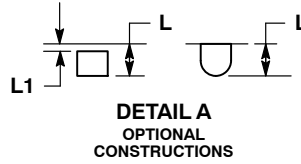
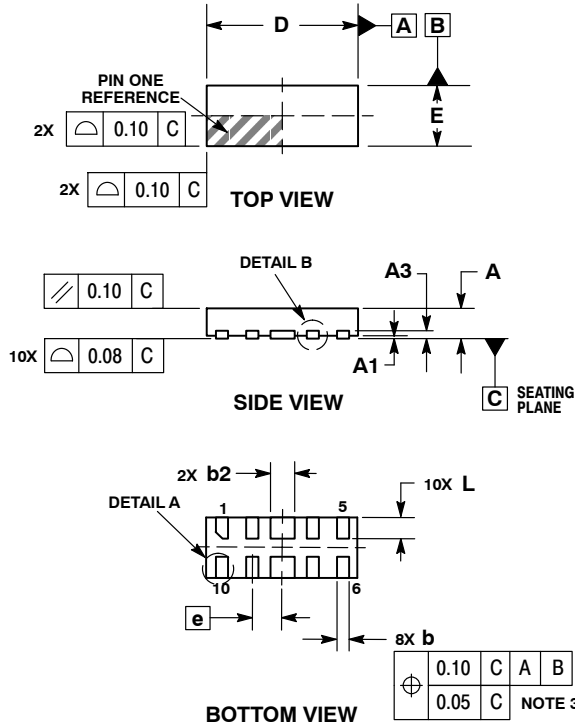
ON Semiconductor®



**UDFN10 2.5x1, 0.5P**  
CASE 517BB-01  
ISSUE O

DATE 17 NOV 2009

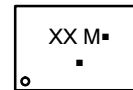
SCALE 4:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
b2	0.35	0.45
D	2.50 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.05

### GENERIC MARKING DIAGRAM\*

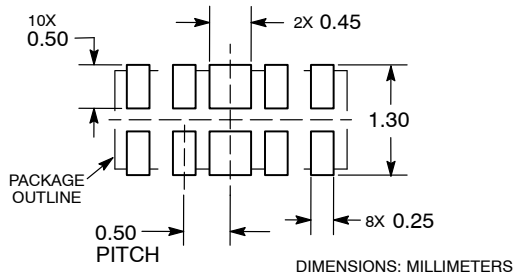


- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON47059E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>UDFN10 2.5X1, 0.5P</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)