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May 2024

FAN73611_OP Single-Channel High-Side Gate Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- 250 mA/500 mA Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise-Canceling Circuit
- 3.3 V and 5 V Input Logic Compatible
- Output In Phase with Input Signal
- Under-Voltage Lockout for V_{DD} and V_{BS}
- 8-Lead Small Outline Package (SOP)

The FAN73611_OP is a monolithic bigh-side gate drive IC that can drive MOSFETs and serating up to +600 V. Fairchild's high-voltage rocess and common mode noise canceling to iniques rovid stable operation of the high-side driver in high additional recurrent stances. An advantable in-shift incuit offers high-side gate driver peraticular $V_S=-9.2$ (typical) for $V_{BS}=15$. The VLO coults prevents malfunction when V_{DC} or $V_{BS}=10$. The the specified threshold voltage. The rest typically source/sink 250 mA/500 mA; the vely, such is suitable for Plasma Display Panel (Fig. 2) a plication, motor drive invertex, and switching mode power supply applications.

Applications

- PDP Scan Driver
- Motor Driver
- Switching-Mode Power July (MPS)

Related A plic ton Jtes

- AN 6076 Design .d Application Guide of Boostrar,
 _ircu. `or i oh-voitage Cate Drive IC
- N-905 Design Guide for Selection of Bootstrap
- AN 3102 Recommendations to Avoid Snort Pulse Width Issues in HVIC Cate Driver Applications

Description

Ordering Information

Part Number	Package	Operating Temperature	Packing Method	Description
FAN73611MX_OP ⁽¹⁾	8 SOP	-40°C ~ 125°C	Tape & Reel	General Application

Note:

1. This device passed wave soldering test by JESD22A-111.





Typical Application Diagrams

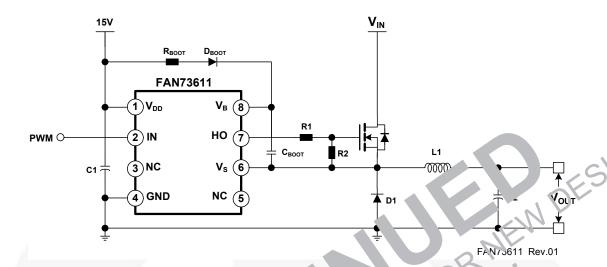


Figure 1. Step-Down (Buc) Control Verter Application

Internal Block Diagn

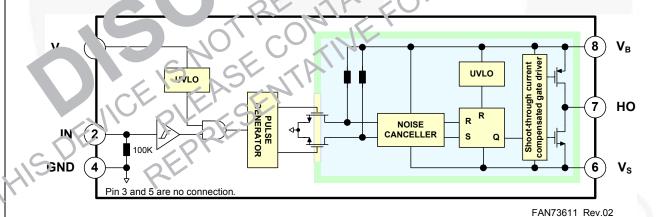


Figure 2. Functional Block Diagram

Pin Configuration

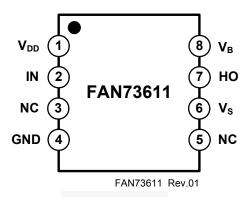


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	V _{DD}	Supply Vulage
2	IN	Log mut i High-to Je Gate Driver Output
3	NC	Co 'ecuc
4	GND	Grc d
5		No unnection
6	V _S	піgh-Voltage Floatir g Supply Retu 1
7		High-Side Driver Cutput
8	V _B	Fligh-Side Fluating Supriy

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}C$ unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V _S	High-Side Floating Offset Voltage	V _B -25	V _B +0.3	V
V _B	High-Side Floating Supply Voltage	-0.3	625.0	V
V _{HO}	High-Side Floating Output Voltage	V _S -0.3	V _B +0.3	V
V _{DD}	Low-Side and Logic Supply Voltage	-0.3	25.0	V
V _{IN}	Logic Input Voltage	-0.3	V _D	V
dV _S /dt	Allowable Offset Voltage Slew Rate		50	V/ns
P _D	Power Dissipation ^(2, 3, 4)		J.0.	W
θ_{JA}	Thermal Resistance		200	°C /\V
T _J	Junction Temperature	-5	+150	, ℃
T _{STG}	Storage Temperature	-55	-150	°C

Notes:

- 2. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass 30. ma rial).
- 3. Refer to the following standards:

 JESD51-2: Integrated circuits thermal test mathod expressions and conditions, natural convection, and JESD51-3: Low effective thermal conductivity and standards surface mount package.
- 4. Do not exceed power dissipation (PD) to include irreduces

Recommended Or Julian Cor litions

The Recommended Or rating Conditions table defines the conditions for actual device operation. Recommended operating condition, are recific to ensure optimal performance to the datasheet specifications. Fairchild does not recommend e. eed them... designing to absolute maximum ratings.

emb.	Parameter	Min.	Max.	Unit
V _L	High-Side Floating Supply Voltage	V _S +10	V _S +20	V
Vc	Figh-Side Floating Supply Officet Voltage	6-V _{DD}	600	V
НО	Ligh-Side Output Voltage	V _S	V_{B}	V
Vini	Logic เลput Vokage	GND	V_{DD}	V
V _{DD}	Supply Votage	10	20	V
T _A	Operating Ambient Temperature	-40	+125	°C

Electrical Characteristics

 $V_{BIAS}(V_{DD},\,V_{BS})$ = 15.0 V and T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are relative to V_S and are applicable to the respective output HO.

Symbol	Characteristics	Test Condition	Min.	Тур.	Max.	Unit
Power Su	pply Section				1	
I_{QDD}	Quiescent V _{DD} Supply Current	V _{IN} =0 V or 5 V, C _{LOAD} =1000 pF		80	140	μА
I _{PDD}	Operating V _{DD} Supply Current	C _{LOAD} =1000 pF, f _{IN} =20 KHz, RMS value		80	160	μА
$V_{DDUV+} \ V_{BSUV+}$	V_{DD} and V_{BS} Supply Under-Voltage Positive Going Threshold Voltage	V _{DD} =Sweep, V _{BS} =Sweep	7.8	8.8	9.8	٧
V _{DDUV-} V _{BSUV-}	V _{DD} and V _{BS} Supply Under-Voltage Negative Going Threshold Voltage	V _{DD} =Sweep, V _{BS} =Sweep	7.	8.3	9.3	8
V _{DDHYS} V _{BSHYS}	V_{DD} and V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage	V _{DD} =Sweep, V _{BS} =Swε τ		0.5	(O)	٧
I _{LK}	Offset Supply Leakage Current	V _B =V _S =600 V		6	10	μА
I _{QBS}	Quiescent V _{BS} Supply Current	V _{IN} =0 ' 5 V, OAL JU pF	2	60	100	μА
I _{PBS}	Operating V _{BS} Supply Current	C _O , =1c 7 pr, :20 KHz RMS 'ue	-ex	420	600	μΑ
Input Log	ic Section	OED OF	3	7		
V_{IH}	Logic "1" Input Voltage	ND R	2.5			V
V_{IL}	Logic "0" Input Voltage	WE, Op, O			0.8	V
I _{IN+}	Logic Input High Bias rrrent	V _N =5 V		50	75	μА
I _{IN-}	Logic Input L w Bias Cu.	V _{IN} =0 V			2	μА
R_{IN}	Input Do Resi ance	(K-CO)	60	100		ΚΩ
Gate Driv	r C tion					
V	in the Liver utput Voltage (V _{BIAS} · V _D)	I 'o Load			0.1	V
V _{OL}	Lov. evel Octput Voltage	No Load			0.1	V
	Output High, Short Circuit Pulsed Current	V _{HO} =0 V, V _{IN} =5 V, PW ≤10 μs	200	250	7	mA
I _{O-}	Output Low, Short Circuit Puisea Current	V_{HO} =15 V, V_{IN} =0 V, PW \leq 10 μ s	400	500		mA
C VS	Allowable Negative V., Pin Voltage for IN Signal Propagation to HO	V _{BS} =15 V		-9.8	-7.0	V

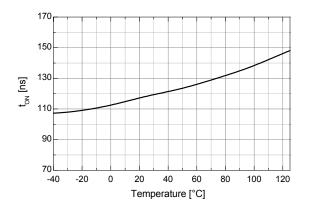
Dynamic Electrical Characteristics

 $\rm V_{DD}\text{=}V_{BS}\text{=}15$ V, $\rm C_{LOAD}\text{=}1000$ pF, and $\rm T_{A}\text{=}25^{\circ}C,$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
t _{on}	Turn-On Propagation Delay Time	V _S =0 V	70	120	170	ns
t _{off}	Turn-Off Propagation Delay Time	V _S =0 V	70	120	170	ns
t _r	Turn-On Rise Time			70	140	ns
t _f	Turn-Off Fall Time			30	60	ns

.

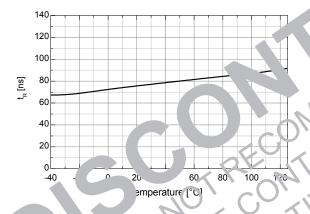
Typical Characteristics

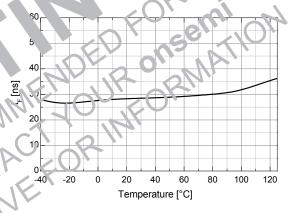


170 150 130 110 90 -40 -20 0 20 60 80 0 120 Ten ratur C]

Figure 5. Turn-On Propagation Delay vs. Temperature

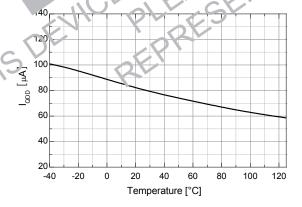
Figu. 6. Tu. -On pagation Delay vs. emperature





Figu. 7. rn-On Ries Time vs. Temperature

Figure 8. Turn-Off Fall Time vs. Temperature



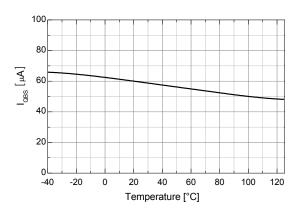
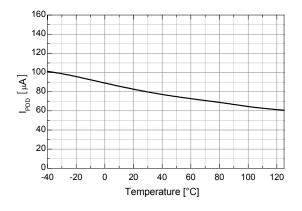


Figure 9. Quiescent V_{DD} Supply Current vs. Temperature

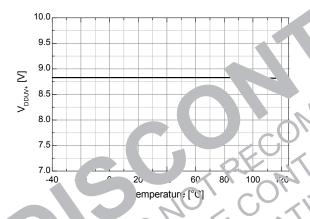
Figure 10. Quiescent V_{BS} Supply Current vs. Temperature



600 550 500 500 440 350 300 250 -40 -20 0 20 60 80 0 120 Ten__ratur C]

Figure 11. Operating V_{DD} Supply Current vs. Temperature

Figure 2. Op htm Supply Current vs. amperature



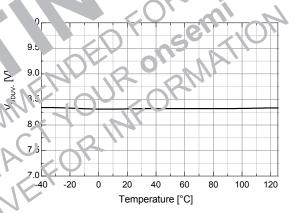
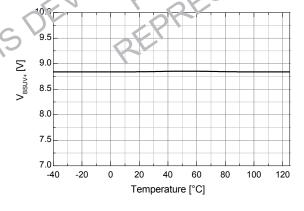


Figure 3. V_{DD} U /LQ+ vs. Temperature

Figure 14. V_{DD} UVLO- vs. Temperature



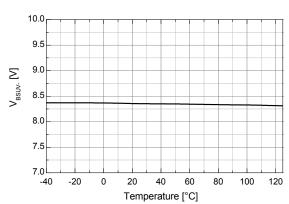
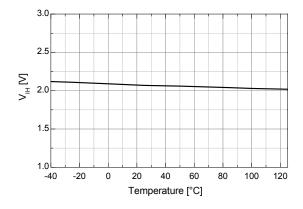


Figure 15. V_{BS} UVLO+ vs. Temperature

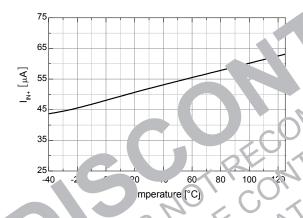
Figure 16. V_{BS} UVLO- vs. Temperature



3.0 2.5 2.0 1.5 1.0 0.5 -40 -20 0 20 5 60 '0 0 120 Tem, 'att', C]

Figure 17. Logic HIGH Input Voltage vs. Temperature

Fig. > 18. L. nic Input Voltage vs. emperature



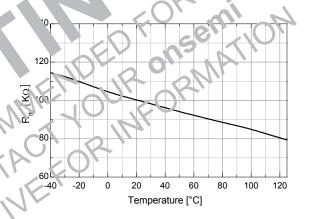
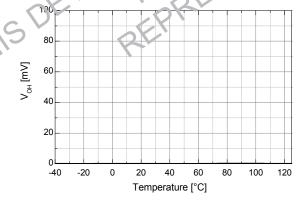


Fig e 1 Logic High Input Stas Current
vs. Temperature

Figure 20. Input Pull-Down Resistance vs. Temperature



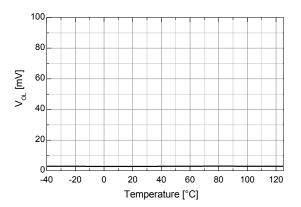
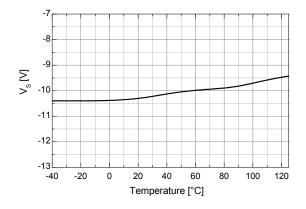


Figure 21. High-Level Output Voltage vs. Temperature

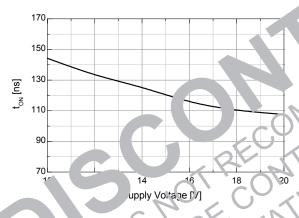
Figure 22. Low-Level Output Voltage vs. Temperature

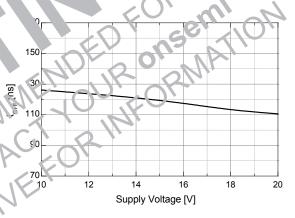


-4
-6
-8
-8
-7
-10
-12
-14
-16
10
12
14
16
18
20
Supi Volta [V]

Figure 23. Allowable Negative V_S Voltage vs. Temperature

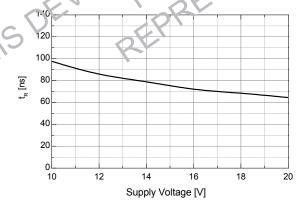
Figure 4. Allc able gative V₃ Voltage vs. 5 pply Voltage





Filine 5. Turn On Propagation Delay vs. Supply Voltage

Figure 26. Turn-Off Propagation Delay vs. Supply Voltage



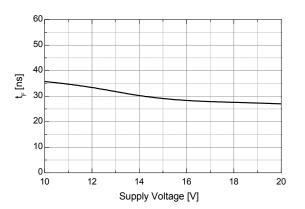


Figure 27. Turn-On Rise Time vs. Supply Voltage

Figure 28. Turn-Off Fall Time vs. Supply Voltage

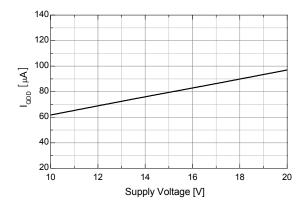
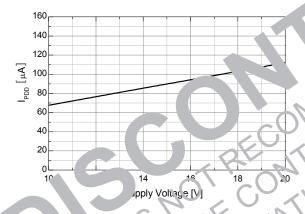


Figure 29. Quiescent V_{DD} Supply Current vs. Supply Voltage

Figure 1. Qu. cei as Supply Current vs. 5 pply Voltage



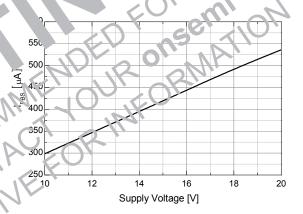


Fig. 'e 5. Operating V_{DD} Supply Current vs. Supply Yoltage

Figure 32. Operating V_{BS} Supply Current vs. Supply Voltage

Switching Time Definitions

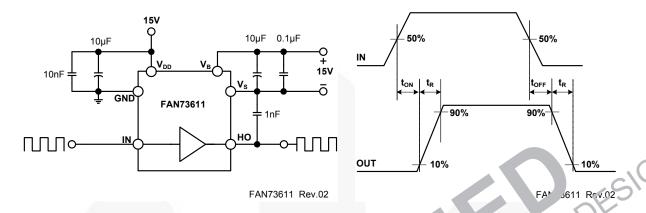


Figure 33. Switching Time Test Circuit and Way form of fin or

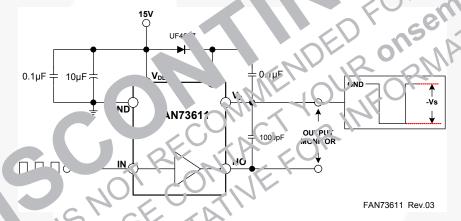
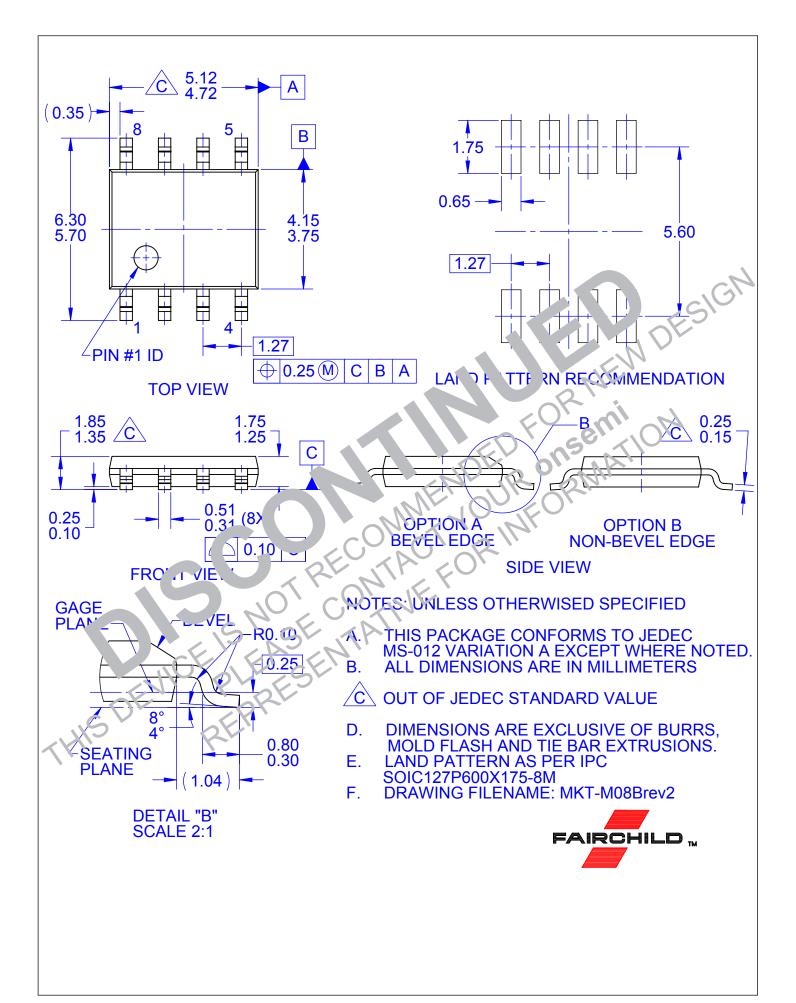


Figure 34. Floating Supply Voltage Transient Test





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