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July 2012

# FAN7393A
# Half-Bridge Gate Drive IC

## Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 2.5A/2.5A Sourcing/Sinking Current Driving Capability
- Extended Allowable Negative $V_S$ Swing to -9.8V for Signal Propagation at $V_{BS}$=15V
- High-Side Output in Phase of IN Input Signal
- 3.3V and 5V Input Logic Compatible
- Matched Propagation Delay for Both Channels
- Built-in Shutdown Function
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Cancelling Circuit
- Internal 400ns Minimum Dead Time at $R_{DT}$=0Ω
- Programmable Turn-On Delay Control (Dead-Time)

## Applications

- High-Speed Power MOSFET and IGBT Gate Driver
- Induction Heating
- High-Power DC-DC Converter
- Synchronous Step-Down Converter
- Motor Drive Inverter

## Description

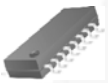
The FAN7393A is a half-bridge gate-drive IC with shut-down and programmable dead-time control functions that can drive high-speed MOSFETs and Isolated Gate Bridge Transistors (IGBTs) operating up to +600V. It has a buffered output stage with all NMOS transistors designed for high-pulse-current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circum-stances. An advanced level-shift circuit offers high-side gate driver operation up to $V_S$=-9.8V (typical) for $V_{BS}$=15V.

The UVLO circuit prevents malfunction when $V_{DD}$ and $V_{BS}$ are lower than the specified threshold voltage.

The high-current and low-output voltage drop feature makes this device suitable for diverse half- and full-bridge inverters; motor drive inverters, switching mode power supplies, induction heating, and high-power DC-DC converter applications.

**14-SOP**



## Ordering Information

| Part Number | Package | Operating Temperature | Packing Method |
|---|---|---|---|
| FAN7393AMX | 14-SOIC | -40°C to +125°C | Tape & Reel |

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## Typical Application Diagrams

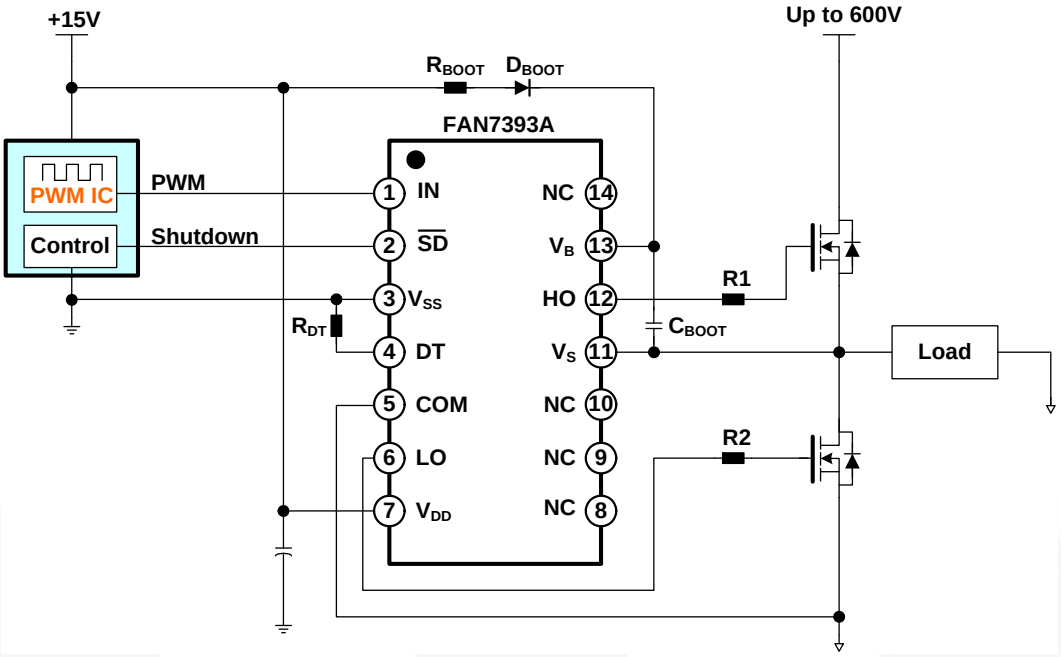


**Figure 1. Typical Application Circuit**

## Internal Block Diagram

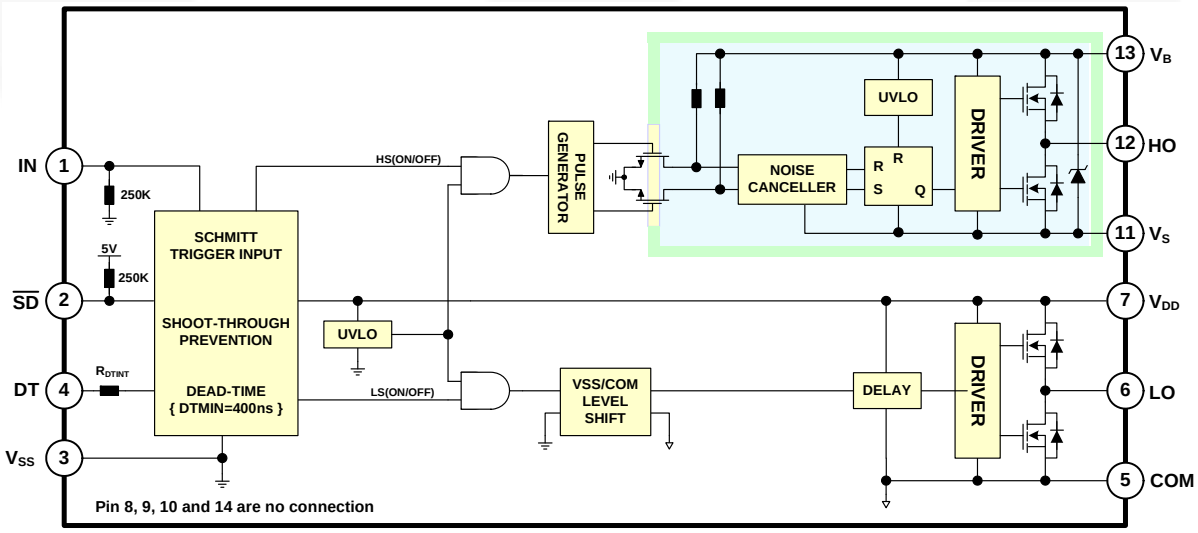


**Figure 2. Functional Block Diagram**

## Pin Configuration

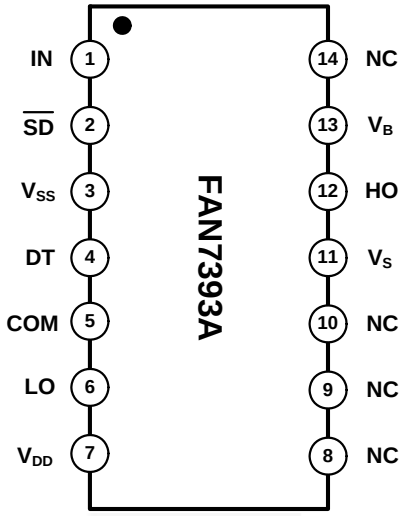


**Figure 3. Pin Configurations (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | IN | Logic Input for High-Side and Low-Side Gate Driver Output, In-Phase with HO |
| 2 | $\overline{SD}$ | Logic Input for Shutdown |
| 3 | $V_{SS}$ | Logic Ground |
| 4 | DT | Dead-Time Control with External Resistor (Referenced to $V_{SS}$) |
| 5 | COM | Ground |
| 6 | LO | Low-Side Driver Return |
| 7 | $V_{DD}$ | Supply Voltage |
| 8 | NC | No Connection |
| 9 | NC | No Connection |
| 10 | NC | No Connection |
| 11 | $V_S$ | High-Voltage Floating Supply Return |
| 12 | HO | High-Side Driver Output |
| 13 | $V_B$ | High-Side Floating Supply |
| 14 | NC | No Connection |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C unless otherwise specified.

| Symbol | Characteristics | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_B$ | High-Side Floating Supply Voltage | -0.3 | 625.0 | V |
| $V_S$ | High-Side Floating Offset Voltage(1) | $V_B$-$V_{SHUNT}$ | $V_B$+0.3 | V |
| $V_{HO}$ | High-Side Floating Output Voltage | $V_S$-0.3 | $V_B$+0.3 | V |
| $V_{LO}$ | Low-Side Output Voltage | -0.3 | $V_{DD}$+0.3 | V |
| $V_{DD}$ | Low-Side and Logic Fixed Supply Voltage | -0.3 | 25.0 | V |
| $V_{IN}$ | Logic Input Voltage (IN) | -0.3 | $V_{DD}$+0.3 | V |
| $V_{SD}$ | Logic Input Voltage ($\overline{SD}$) | $V_{SS}$ | 5.5 | V |
| DT | Programmable Dead-Time Pin Voltage | -0.3 | $V_{DD}$+0.3 | V |
| $V_{SS}$ | Logic Ground | $V_{DD}$-25 | $V_{DD}$+0.3 | V |
| $dV_S/dt$ | Allowable Offset Voltage Slew Rate | | ± 50 | V/ns |
| $P_D$ | Power Dissipation(2, 3, 4) | | 1 | W |
| $\theta_{JA}$ | Thermal Resistance | | 110 | °C/W |
| $T_J$ | Junction Temperature | | +150 | °C |
| $T_{STG}$ | Storage Temperature | -55 | +150 | °C |

**Notes:**

1. This IC contains a shunt regulator on $V_{BS}$. This supply pin should not be driven by a low-impedance voltage source greater than $V_{SHUNT}$ specified in the Electrical Characteristics section.
2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
3. Refer to the following standards:
   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection, and
   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
4. Do not exceed maximum $P_D$ under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_B$ | High-Side Floating Supply Voltage | $V_S$+10 | $V_S$+20 | V |
| $V_S$ | High-Side Floating Supply Offset Voltage | 6-$V_{DD}$ | 600 | V |
| $V_{HO}$ | High-Side Output Voltage | $V_S$ | $V_B$ | V |
| $V_{DD}$ | Low-Side and Logic Fixed Supply Voltage | 10 | 20 | V |
| $V_{LO}$ | Low-Side Output Voltage | COM | $V_{DD}$ | V |
| $V_{IN}$ | Logic Input Voltage (IN) | $V_{SS}$ | $V_{DD}$ | V |
| $V_{SD}$ | Logic Input Voltage ($\overline{SD}$) | $V_{SS}$ | 5 | V |
| DT | Programmable Dead-Time Pin Voltage | $V_{SS}$ | $V_{DD}$ | V |
| $V_{SS}$ | Logic Ground | -5 | +5 | V |
| $T_A$ | Operating Ambient Temperature | -40 | +125 | °C |

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## Electrical Characteristics

$V_{BIAS}(V_{DD}, V_{BS})$=15.0V, $V_{SS}$=COM=0V, DT=$V_{SS}$, and $T_A$=25°C unless otherwise specified. The $V_{IN}$ and $I_{IN}$ parameters are referenced to $V_{SS}$/COM and are applicable to the respective input leads: IN and $\overline{SD}$. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY SECTION** | | | | | | |
| $I_{QDD}$ | Quiescent $V_{DD}$ Supply Current | $V_{IN}$=0V or 5V | | 600 | 1000 | μA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{IN}$=0V or 5V | | 55 | 100 | μA |
| $I_{PDD}$ | Operating $V_{DD}$ Supply Current | $f_{IN}$=20KHz, No Load | | 1.0 | 1.6 | mA |
| $I_{PBS}$ | Operating $V_{BS}$ Supply Current | $C_L$=1nF, $f_{IN}$=20KHz, RMS | | 450 | 800 | μA |
| $I_{SD}$ | Shutdown Mode Supply Current | $\overline{SD}$=$V_{SS}$ | | 650 | 1000 | μA |
| $I_{LK}$ | Offset Supply Leakage Current | $V_B$=$V_S$=600V | | | 10 | μA |
| **BOOTSTRAPPED SUPPLY SECTION** | | | | | | |
| $V_{DDUV+}$ $V_{BSUV+}$ | $V_{DD}$ and $V_{BS}$ Supply Under-Voltage Positive-Going Threshold Voltage | $V_{IN}$=0V, $V_{DD}$=$V_{BS}$=Sweep | 7.8 | 8.8 | 9.8 | V |
| $V_{DDUV-}$ $V_{BSUV-}$ | $V_{DD}$ and $V_{BS}$ Supply Under-Voltage Negative-Going Threshold Voltage | $V_{IN}$=0V, $V_{DD}$=$V_{BS}$=Sweep | 7.3 | 8.3 | 9.3 | V |
| $V_{DDUVH-}$ $V_{BSUVH}$ | $V_{DD}$ and $V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage | $V_{IN}$=0V, $V_{DD}$=$V_{BS}$=Sweep | | 0.5 | | V |
| **SHUNT REGULATOR SECTION** | | | | | | |
| $V_{SHUNT}$ | Shunt Regulator Clamping Voltage for $V_{BS}$ | $V_{BS}$=Sweep, $I_{SHUNT}$=5mA | 21 | 23 | 25 | V |
| **INPUT LOGIC SECTION** | | | | | | |
| $V_{IH}$ | Logic “1” Input Voltage for HO & Logic “0” for LO | | 2.5 | | | V |
| $V_{IL}$ | Logic “0” Input Voltage for HO & Logic “1” for LO | | | | 0.8 | V |
| $I_{IN+}$ | Logic Input High Bias Current | $V_{IN}$=5V, $\overline{SD}$=0V | | 20 | 50 | μA |
| $I_{IN-}$ | Logic Input Low Bias Current | $V_{IN}$=0V, $\overline{SD}$=5V | | | 3 | μA |
| $R_{IN}$ | Logic Input Pull-Down Resistance | | 100 | 250 | | KΩ |
| $V_{SDCLAMP}$ | Shutdown ($\overline{SD}$) Input Clamping Voltage(5) | | | 5.0 | 5.5 | V |
| $\overline{SD}$+ | Shutdown ($\overline{SD}$) Input Positive-Going Threshold | | 2.5 | | | V |
| $\overline{SD}$- | Shutdown ($\overline{SD}$) Input Negative-Going Threshold | | | | 0.8 | V |
| $R_{PSD}$ | Shutdown ($\overline{SD}$) Input Pull-Up Resistance | | 100 | 250 | | KΩ |
| **GATE DRIVER OUTPUT SECTION** | | | | | | |
| $V_{OH}$ | High-Level Output Voltage ($V_{BIAS}$ - $V_O$) | No Load ($I_O$=0A) | | | 1.5 | V |
| $V_{OL}$ | Low-Level Output Voltage | No Load ($I_O$=0A) | | | 100 | mV |
| $I_{O+}$ | Output High, Short-Circuit Pulsed Current(5) | $V_{HO}$=0V, $V_{IN}$=5V, PW ≤10μs | 2.0 | 2.5 | | A |
| $I_{O-}$ | Output Low, Short-Circuit Pulsed Current(5) | $V_{HO}$=15V, $V_{IN}$=0V, PW ≤10μs | 2.0 | 2.5 | | A |
| $V_{SS}$/COM | $V_{SS}$-COM/COM-$V_{SS}$ Voltage Endurability(5) | | -5.0 | | 5.0 | V |
| $V_S$ | Allowable Negative $V_S$ Pin Voltage for IN Signal Propagation to HO | | | -9.8 | -7.0 | V |

**Note:**

5 These parameters are guaranteed by design.

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## Dynamic Electrical Characteristics

$V_{BIAS}$($V_{DD}$, $V_{BS}$)=15.0V, $V_{SS}$=COM=0V, $C_L$=1000pF, DT=$V_{SS}$, and $T_A$=25°C, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ON}$ | Turn-On Propagation Delay(6) | $V_S$=0V, $R_{DT}$=0Ω | | 530 | 730 | ns |
| $t_{OFF}$ | Turn-Off Propagation Delay | $V_S$=0V | | 130 | 250 | ns |
| $t_{SD}$ | Shutdown Propagation Delay | | | 140 | 210 | ns |
| $Mt_{ON}$ | Delay Matching, HO and LO Turn-On | | | 0 | 90 | ns |
| $Mt_{OFF}$ | Delay Matching, HO and LO Turn-Off | | | 0 | 40 | ns |
| $t_R$ | Turn-On Rise Time | $V_S$=0V | | 25 | 50 | ns |
| $t_F$ | Turn-Off Fall Time | $V_S$=0V | | 15 | 35 | ns |
| DT | Dead Time: LO Turn-Off to HO Turn-On, HO Turn-Off to LO Turn-On | $R_{DT}$=0Ω | 300 | 400 | 500 | ns |
| | | $R_{DT}$=200KΩ | 4 | 5 | 6 | µs |
| MDT | Dead-Time Matching=\|$DT_{LO-HO}$ - $DT_{HO-LO}$\| | $R_{DT}$=0Ω | | 0 | 40 | ns |
| | | $R_{DT}$=200KΩ | | 0 | 500 | ns |

**Note:**

6 The turn-on propagation delay includes dead time.

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## Typical Characteristics

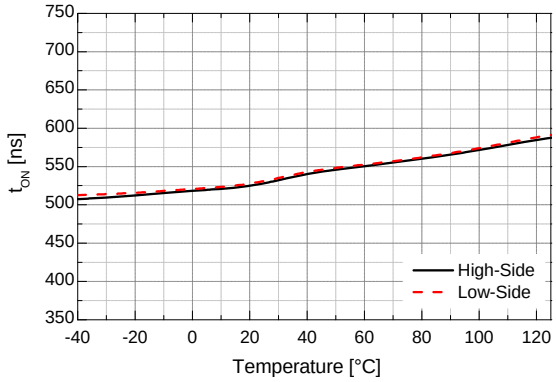


**Figure 4. Turn-On Propagation Delay vs. Temperature**

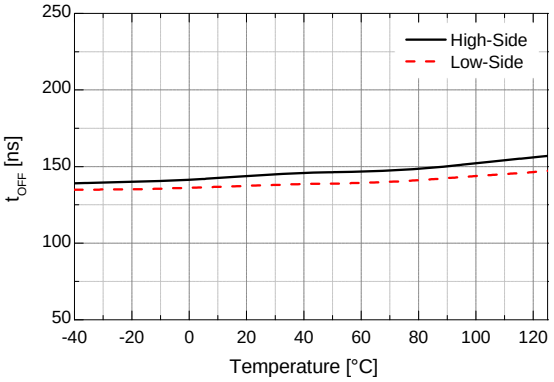


**Figure 5. Turn-Off Propagation Delay vs. Temperature**

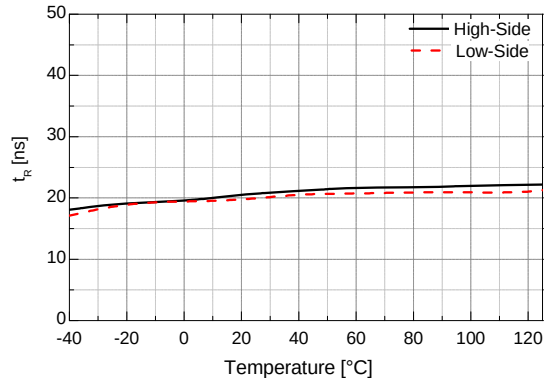


**Figure 6. Turn-On Rise Time vs. Temperature**

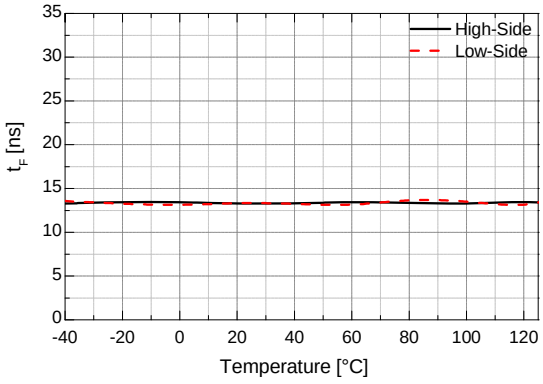


**Figure 7. Turn-Off Fall Time vs. Temperature**

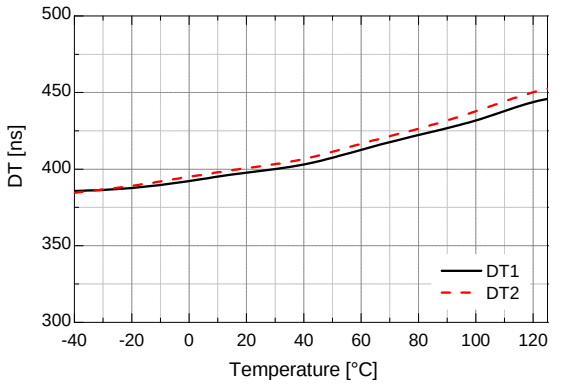


**Figure 8. Dead Time ($R_{DT}$=0Ω) vs. Temperature**

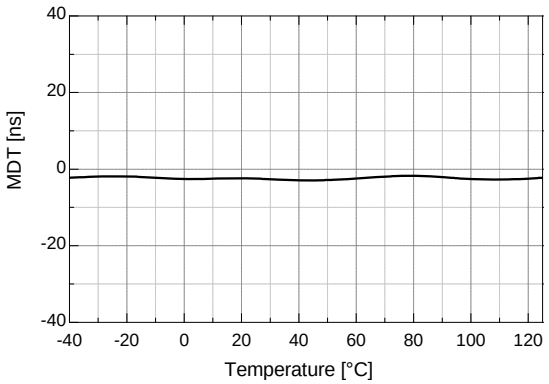


**Figure 9. Dead Time Matching ($R_{DT}$=0Ω) vs. Temperature**

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## Typical Characteristics (Continued)

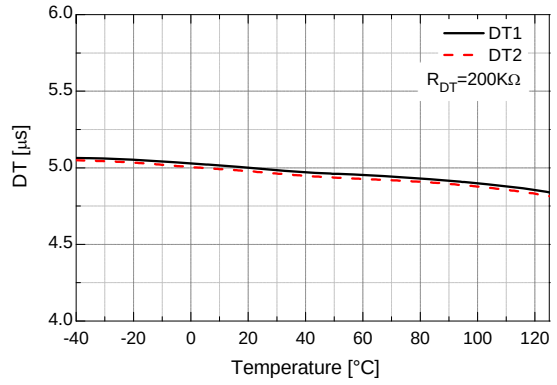


**Figure 10. Dead Time ($R_{DT}$=200KΩ) vs. Temperature**

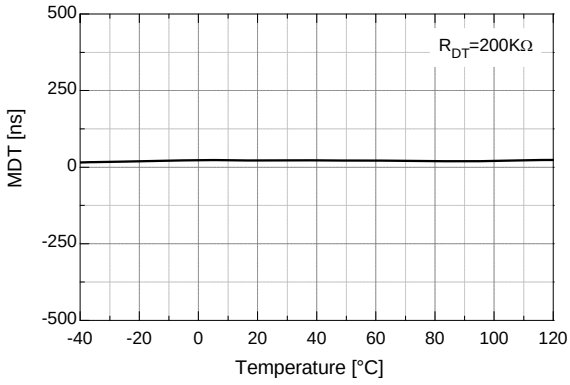


**Figure 11. Dead-Time Matching ($R_{DT}$=200KΩ) vs. Temperature**

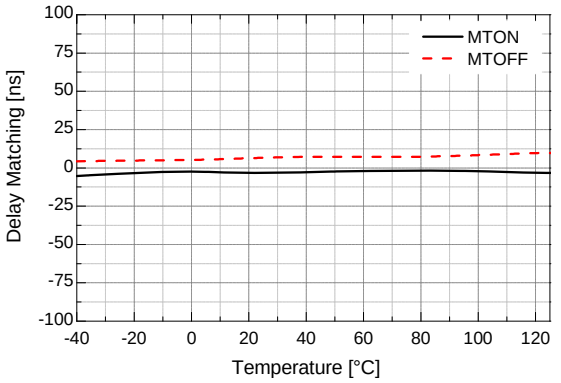


**Figure 12. Delay Matching vs. Temperature**

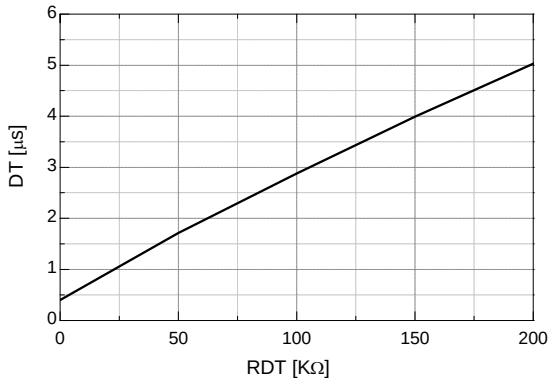


**Figure 13. Dead Time vs. $R_{DT}$**

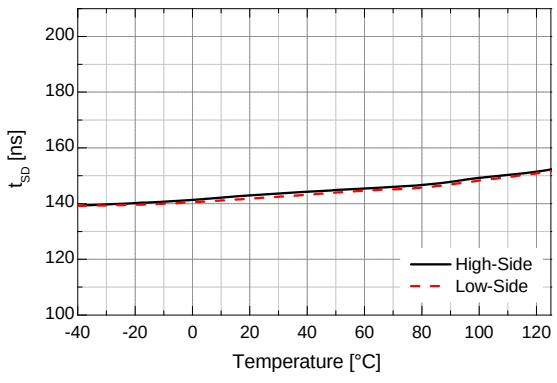


**Figure 14. Shutdown Propagation Delay vs. Temperature**

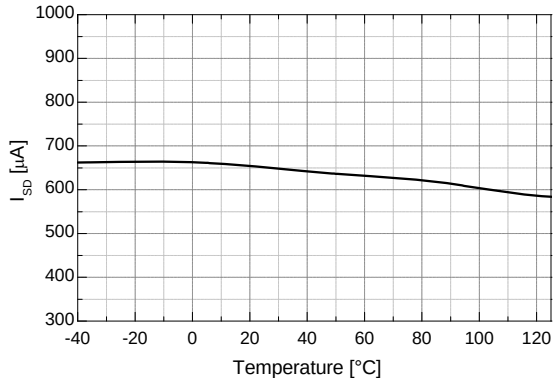


**Figure 15. Shutdown Mode Supply Current vs. Temperature**

## Typical Characteristics (Continued)

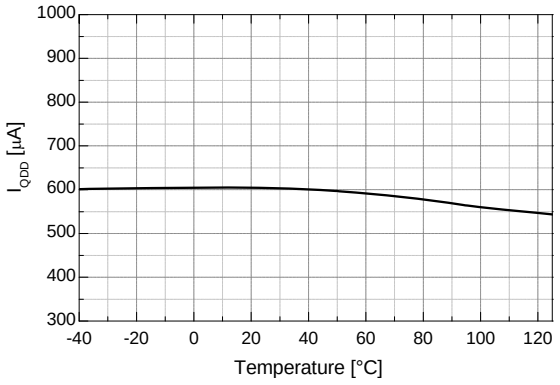


**Figure 16. Quiescent $V_{DD}$ Supply Current vs. Temperature**

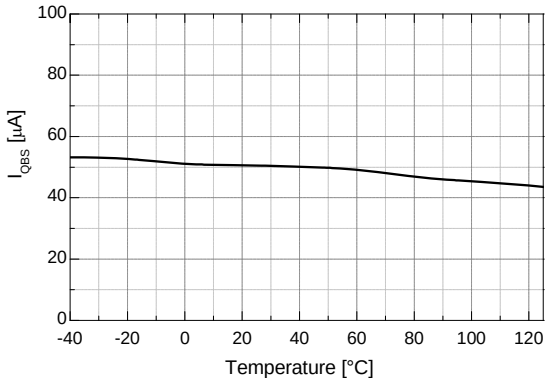


**Figure 17. Quiescent $V_{BS}$ Supply Current vs. Temperature**

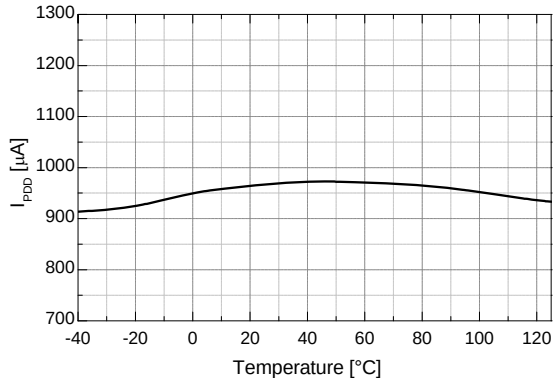


**Figure 18. Operating $V_{DD}$ Supply Current vs. Temperature**

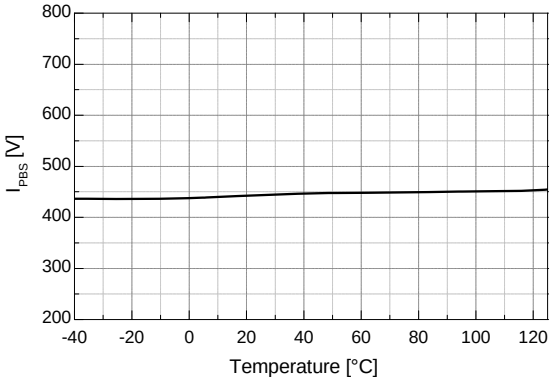


**Figure 19. Operating $V_{BS}$ Supply Current vs. Temperature**

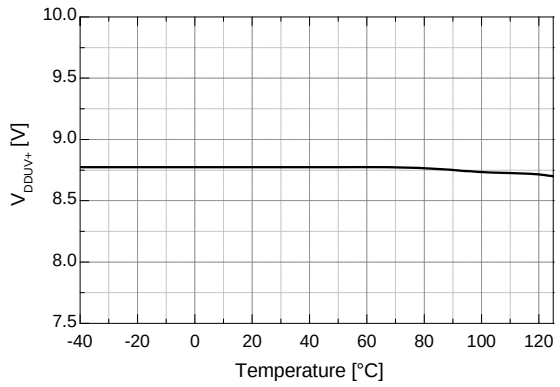


**Figure 20. $V_{DD}$ UVLO+ vs. Temperature**

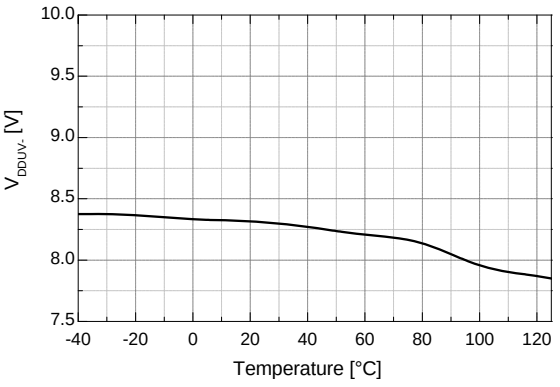


**Figure 21. $V_{DD}$ UVLO- vs. Temperature**

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## Typical Characteristics (Continued)

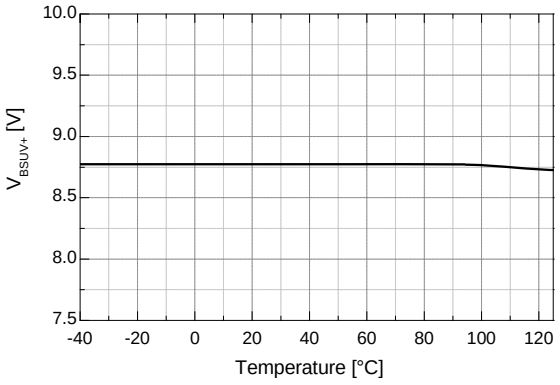


**Figure 22. $V_{BS}$ UVLO+ vs. Temperature**

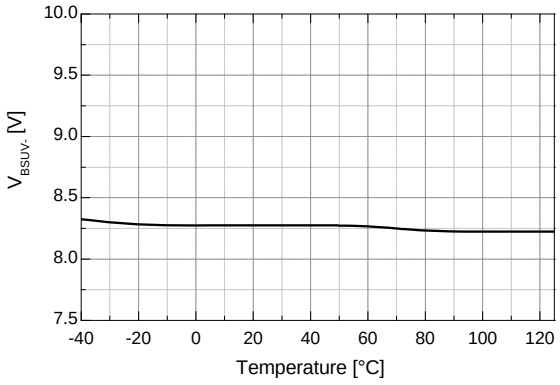


**Figure 23. $V_{BS}$ UVLO- vs. Temperature**

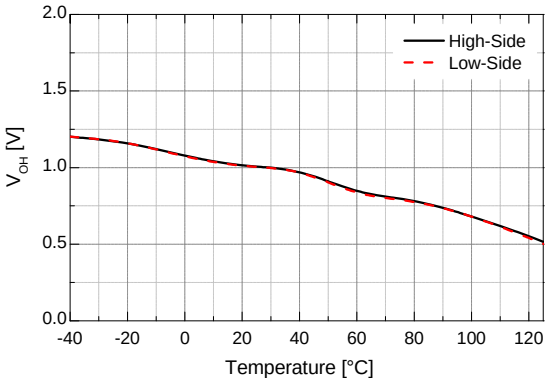


**Figure 24. High-Level Output Voltage vs. Temperature**

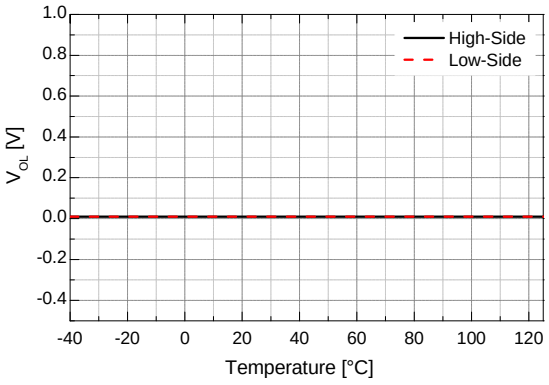


**Figure 25. Low-Level Output Voltage vs. Temperature**

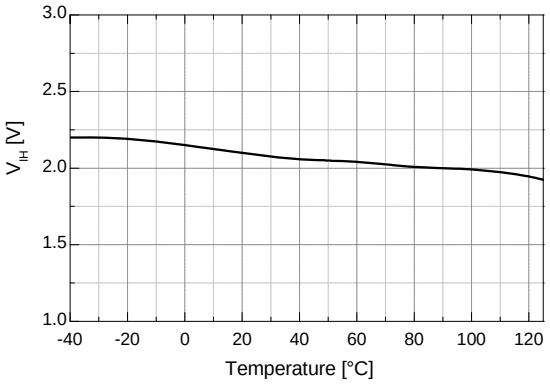


**Figure 26. Logic HIGH Input Voltage vs. Temperature**

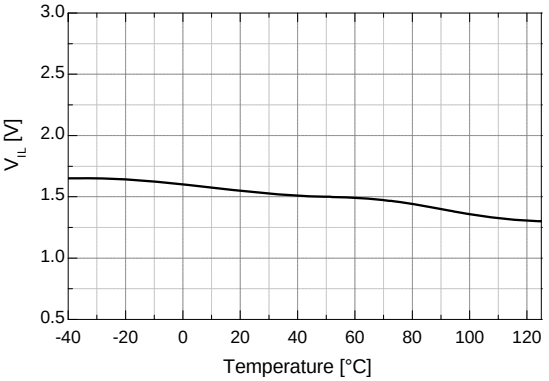


**Figure 27. Logic LOW Input Voltage vs. Temperature**

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## Typical Characteristics (Continued)

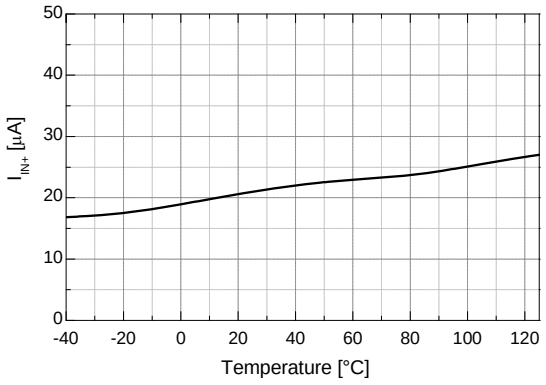



**Figure 28. Logic Input High Bias Current vs. Temperature**

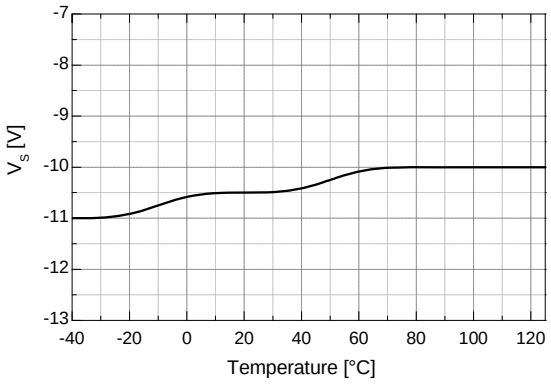



**Figure 29. Allowable Negative $V_S$ Voltage vs. Temperature**

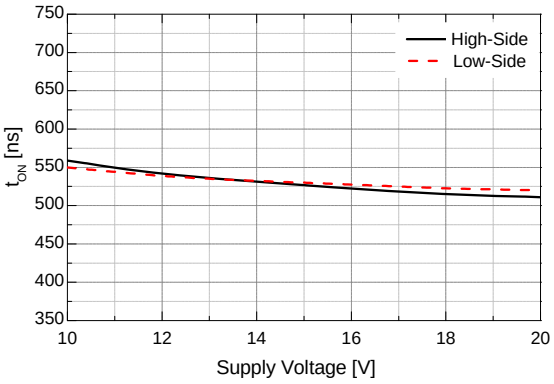



**Figure 30. Turn-On Propagation Delay vs. Supply Voltage**

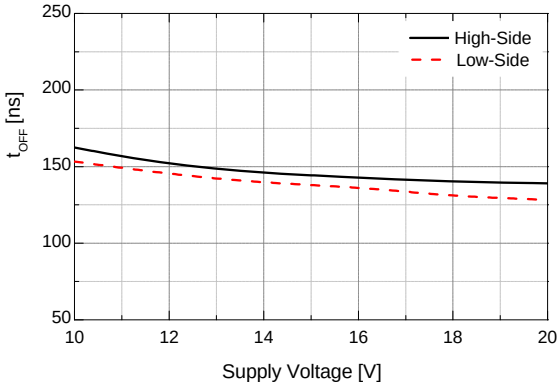



**Figure 31. Turn-Off Propagation Delay vs. Supply Voltage**

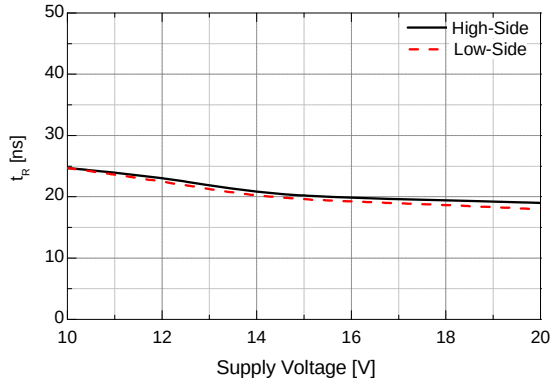



**Figure 32. Turn-On Rise Time vs. Supply Voltage**

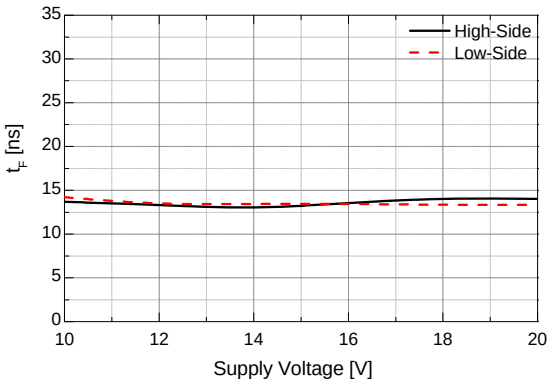



**Figure 33. Turn-Off Fall Time vs. Supply Voltage**

## Typical Characteristics (Continued)

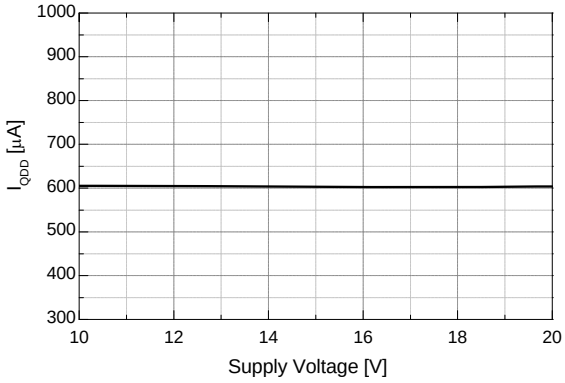



**Figure 34. Quiescent $V_{DD}$ Supply Current vs. Supply Voltage**

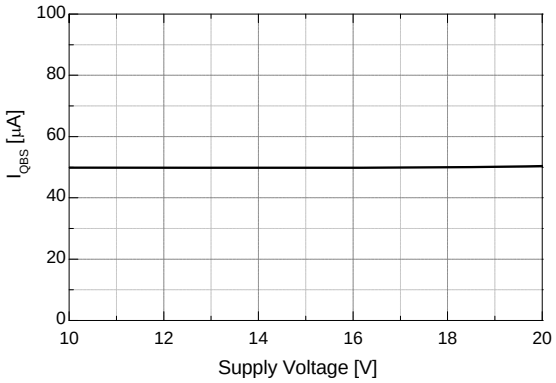



**Figure 35. Quiescent $V_{BS}$ Supply Current vs. Supply Voltage**

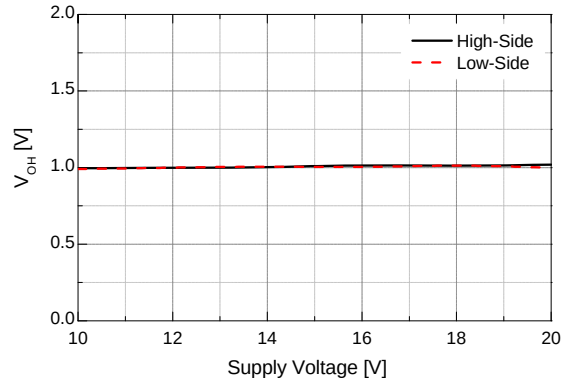



**Figure 36. High-Level Output Voltage vs. Supply Voltage**

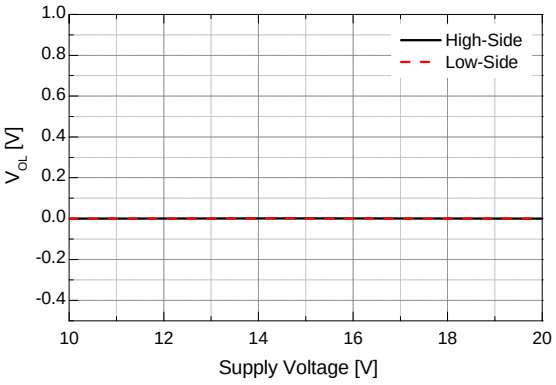



**Figure 37. Low-Level Output Voltage vs. Supply Voltage**

## Switching Time Definitions

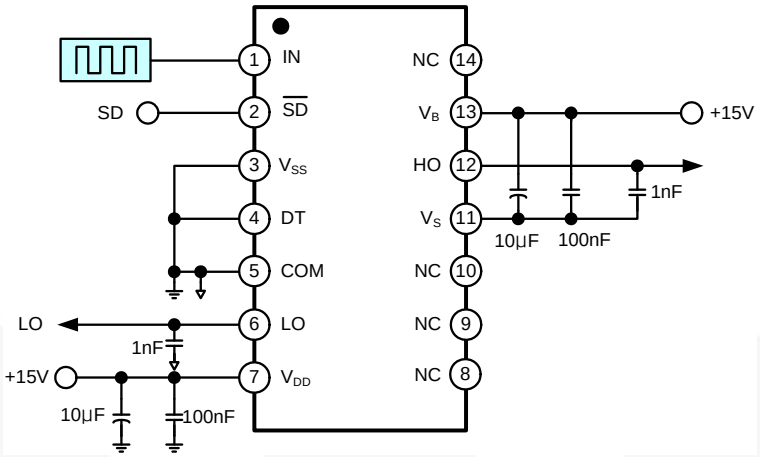



**Figure 38. Switching Time Test Circuit**

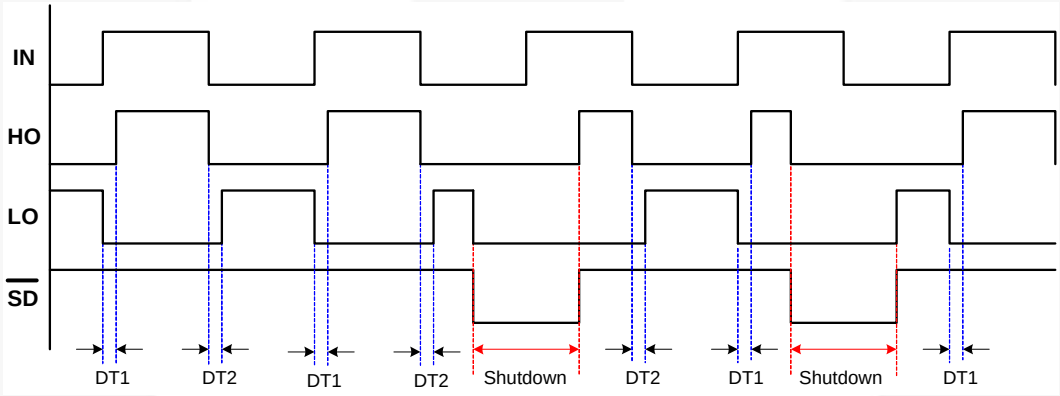



**Figure 39. Input / Output Timing Diagram**

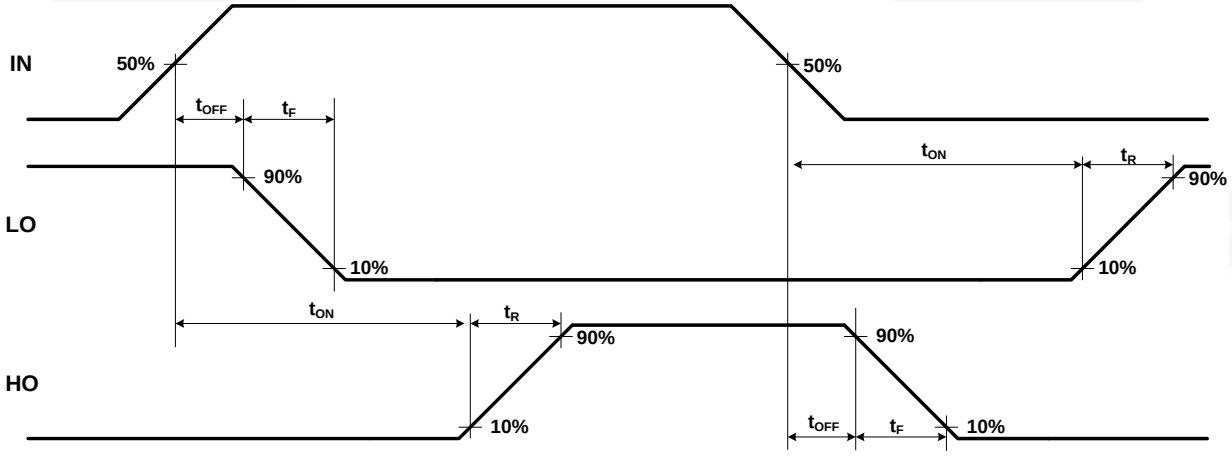



**Figure 40. Switching Time Waveform Definition**

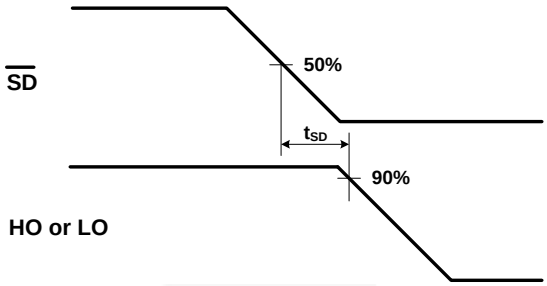
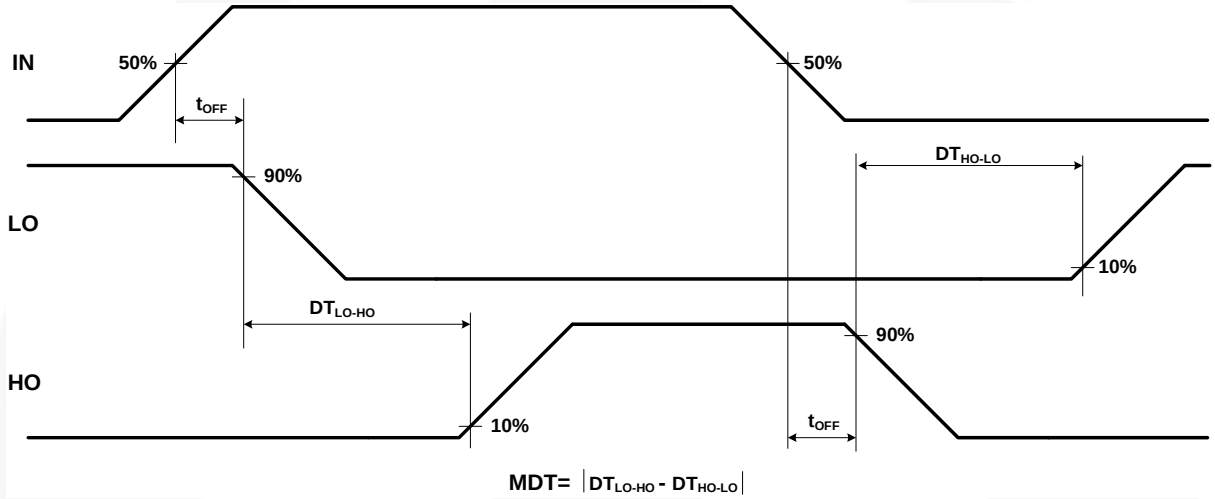



**Figure 41. Shutdown Waveform Definition**




$$MDT = |DT_{LO-HO} - DT_{HO-LO}|$$

**Figure 42. Dead-Time Waveform Definition**

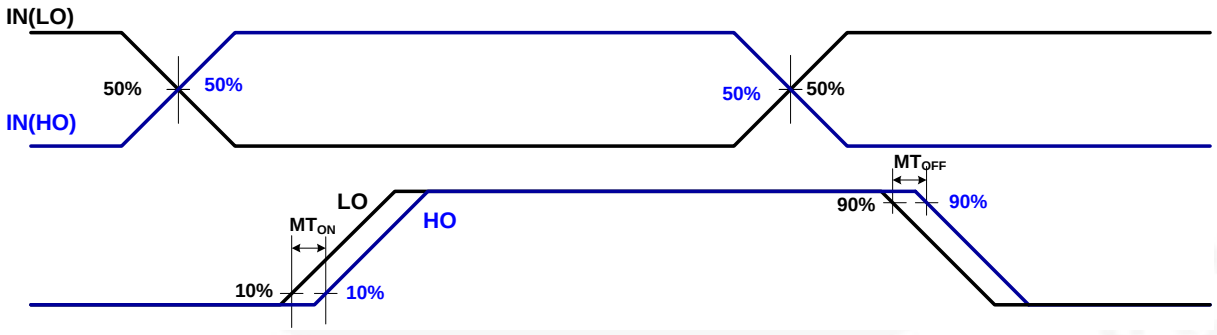
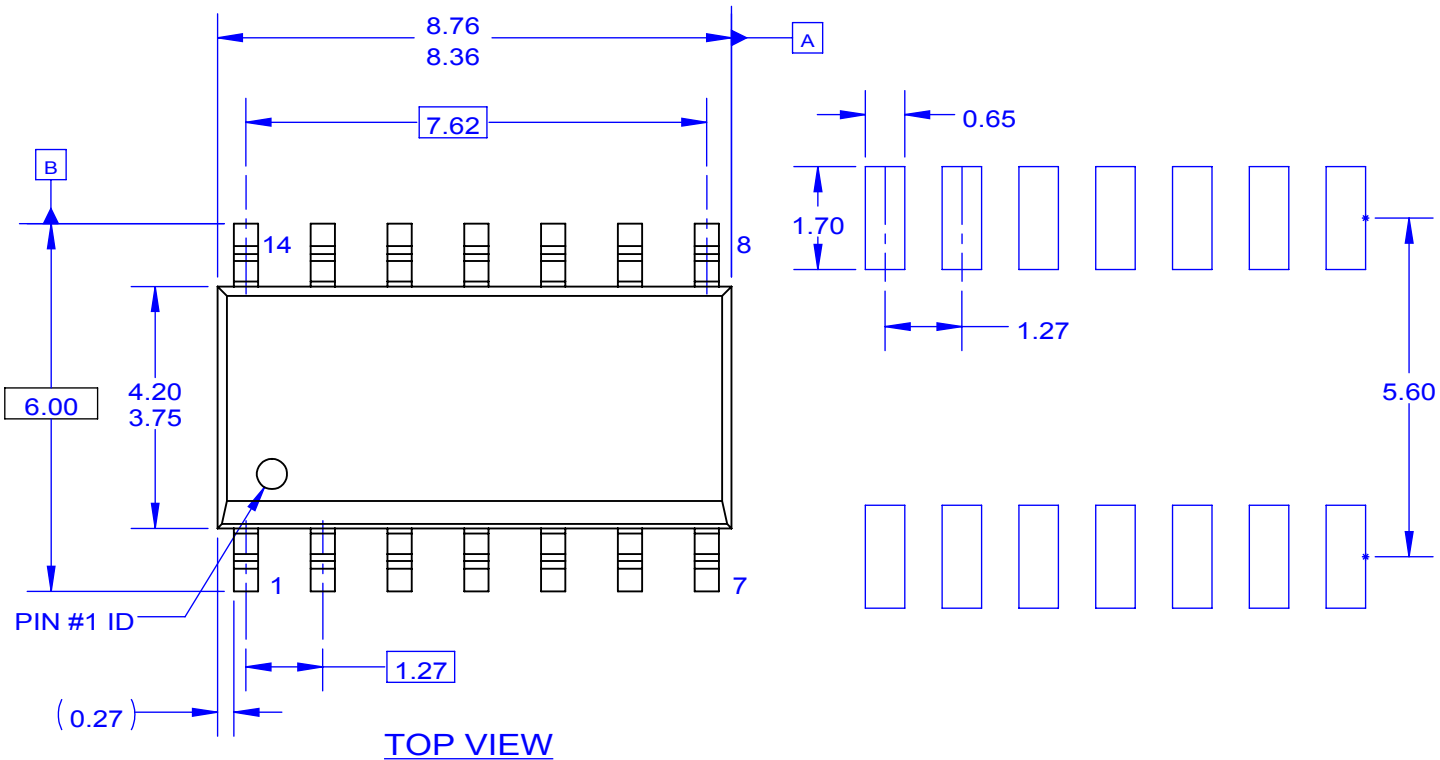
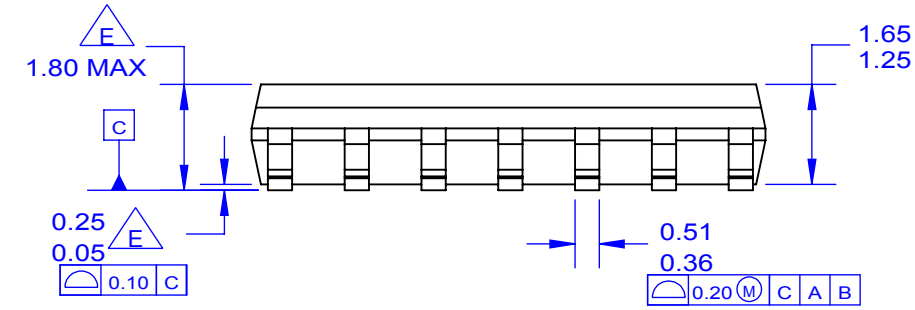



**Figure 43. Delay Matching Waveform Definition**

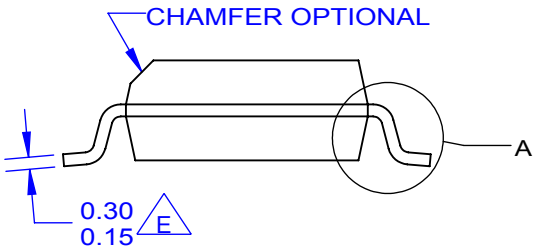



TOP VIEW




ALL LEAD TIPS

SIDE VIEW




END VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

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C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
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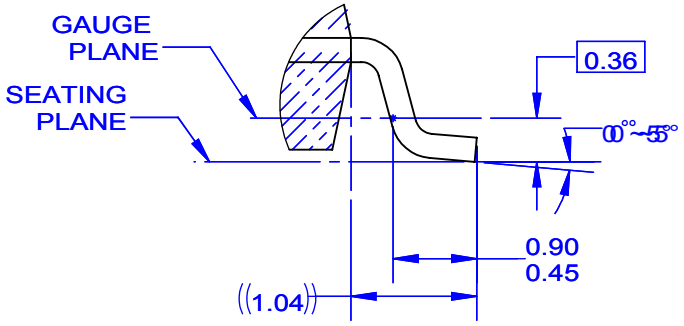
E OUT OF JEDEC STANDARD VALUE.
F. LAND PATTERN STANDARD: SOIC127P600X145-14M.
G. FILE NAME: MKT-M14C REV2

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