MOSFET – Dual, N & P-Channel, POWERTRENCH®

2.5 V Specified

FDC6327C

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
20 V	0.08 Ω @ 4.5 V	2.7 A
	0.12 Ω @ 2.5 V	

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−20 V	0.17 Ω @ −4.5 V	−1.6 A
	0.25 Ω @ −2.5 V	

General Description

These N & P−Channel 2.5 V specified MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize on−state resistance and yet maintain low gate charge for superior switching performance.

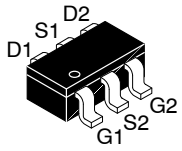
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO−8 and TSSOP−8 packages are impractical.

Features

- N−Channel 2.7 A, 20 V
  $R_{DS(ON)}$ = 0.08 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.12 Ω @ V_{GS} = 2.5 V
- P−Channel −1.6 A, −20 V
  $R_{DS(ON)}$ = 0.17 Ω @ V_{GS} = −4.5 V
  $R_{DS(ON)}$ = 0.25 Ω @ V_{GS} = −2.5 V
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOT™ −6 Package: Small Footprint (72% Smaller than SO−8); Low Profile (1 mm Thick)
- This is a Pb−Free Device

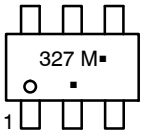
Applications

- DC/DC Converter
- Load Switch
- Motor Driving



TSOT23 6−Lead SUPERSOT™ −6 CASE 419BL

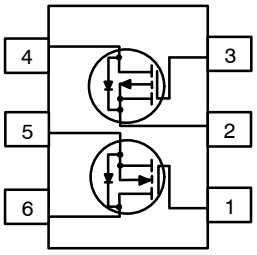
MARKING DIAGRAM



327 = Specific Device Code
M = Assembly Operation Month
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
FDC6327C	TSOT−23−6 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		N−Channel	P−Channel	Unit
V_{DSS}	Drain−Source Voltage		20	−20	V
V_{GSS}	Gate−Source Voltage		±8	±8	V
I_D	Drain Current	− Continuous (Note 1a)	2.7	−1.9	A
		− Pulsed	8	−8	A
P_D	Power Dissipation	(Note 1a)	0.96		W
		(Note 1b)	0.9		W
		(Note 1c)	0.7		W
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	60	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

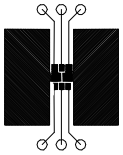
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = −250 μA	N−Ch P−CH	20 −20	− −	− −	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C I_D = −250 μA,Referenced to 25°C	N−Ch P−CH	− −	12 −19	− −	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = −16 V, V_{GS} = 0 V	N−Ch P−CH	− −	− −	1 −1	μA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V	All	−	−	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −8 V, V_{DS} = 0 V	All	−	−	−100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = −250 μA	N−Ch P−CH	0.4 −0.4	0.9 −0.9	1.5 −1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = −250 μA, Referenced to 25°C	N−Ch P−CH	− −	−2.1 2.3	− −	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 4.5 V, I_D = 2.7 A V_{GS} = 4.5 V, I_D = 2.7 A, T_J = 125°C V_{GS} = 2.5 V, I_D = 2.2 A V_{GS} = −4.5 V, I_D = −1.6 A V_{GS} = −4.5 V, I_D = −1.6 A, T_J = 125°C V_{GS} = −2.5 V, I_D = −1.3 A	N−Ch N−Ch N−Ch P−CH P−CH P−CH	− − − − − −	0.069 0.094 0.093 0.141 0.203 0.205	0.08 0.13 0.12 0.17 0.27 0.25	Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V V_{GS} = −4.5 V, V_{DS} = −5 V	N−Ch P−CH	8 −8	− −	− −	A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 2.7 A V_{DS} = −5 V, I_D = −1.9 A	N−Ch P−CH	− −	7.7 4.5	− −	S

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (continued)

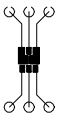
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N–Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N–Ch P–CH	– –	325 315	– –	pF
C_{oss}	Output Capacitance	P–Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N–Ch P–CH	– –	75 65	– –	pF
C_{rss}	Reverse Transfer Capacitance		N–Ch P–CH	– –	35 24	– –	pF
SWITCHING CHARACTERISTICS (Note 2)							
$t_{d(on)}$	Turn–On Delay Time	N–Channel V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω	N–Ch P–CH	– –	5 7	15 14	ns
t_r	Turn–On Rise Time		N–Ch P–CH	– –	9 14	18 25	ns
$t_{d(off)}$	Turn–Off Delay Time	P–Channel V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6 Ω	N–Ch P–CH	– –	12 14	22 25	ns
t_f	Turn–Off Fall Time		N–Ch P–CH	– –	3 3	9 9	ns
Q_g	Total Gate Charge	N–Channel V_{DS} = 10 V, I_D = 2.7 A, V_{GS} = 4.5 V	N–Ch P–CH	– –	3.25 2.85	4.5 4.0	nC
Q_{gs}	Gate–Source Charge	P–Channel V_{DS} = –10 V, I_D = –1.9 A, V_{GS} = –4.5 V	N–Ch P–CH	– –	0.65 0.68	– –	nC
Q_{gd}	Gate–Drain Charge		N–Ch P–CH	– –	0.90 0.65	– –	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain–Source Diode Forward Current		N–Ch P–CH	– –	– –	0.8 –0.8	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.8 A (Note 2) V_{GS} = 0 V, I_S = –0.8 A (Note 2)	N–Ch P–CH	– –	0.76 –0.79	1.2 –1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

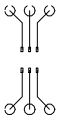
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a. 130°C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b. 140°C/W when mounted on a 0.005 in^2 pad of 2 oz. copper.



c. 180°C/W when mounted on a 0.0015 in2 pad of 2 oz. copper.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS: N−CHANNEL

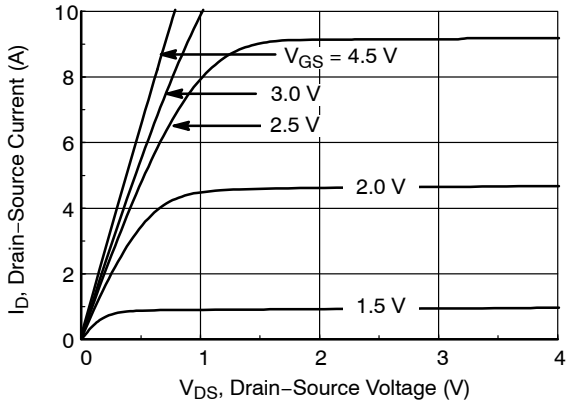


Figure 1. On−Region Characteristics

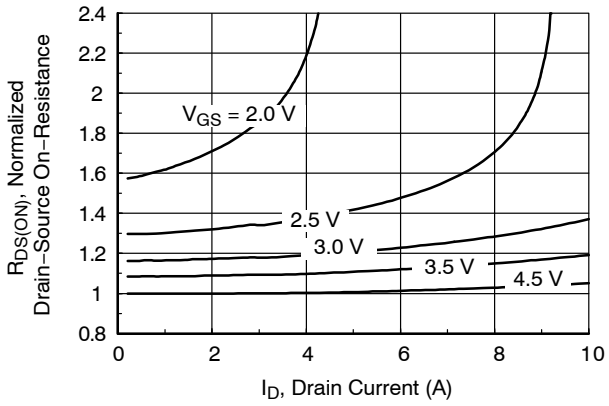


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

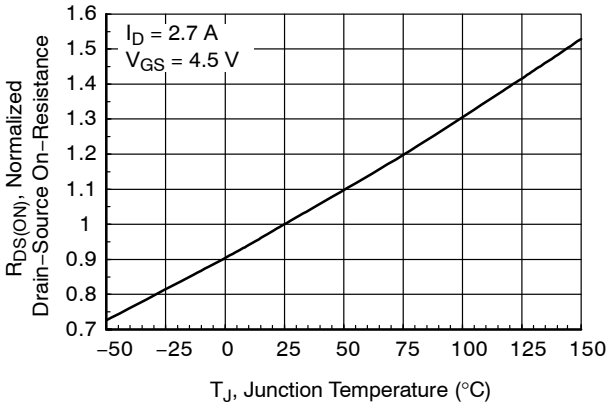


Figure 3. On−Resistance Variation with Temperature

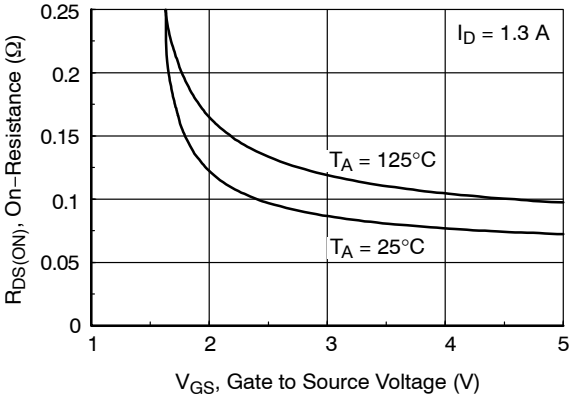


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

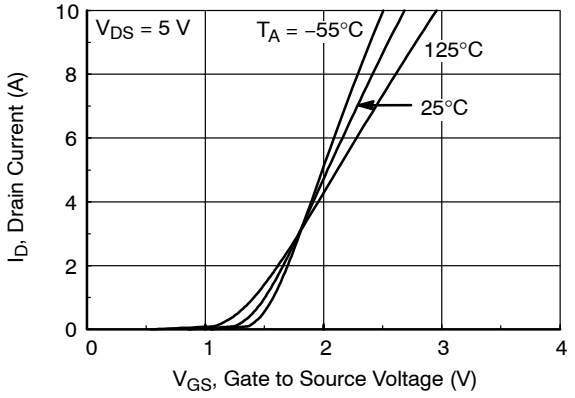


Figure 5. Transfer Characteristics

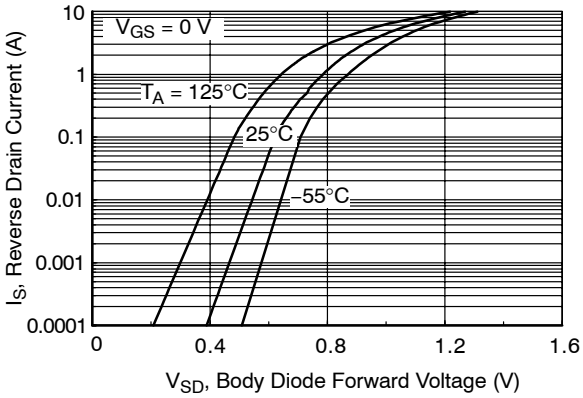


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: N−CHANNEL (continued)

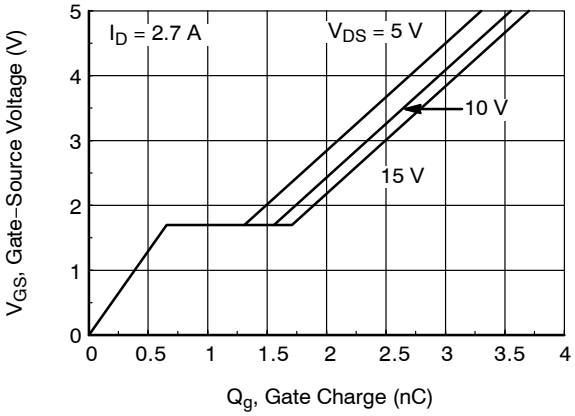


Figure 7. Gate Charge Characteristics

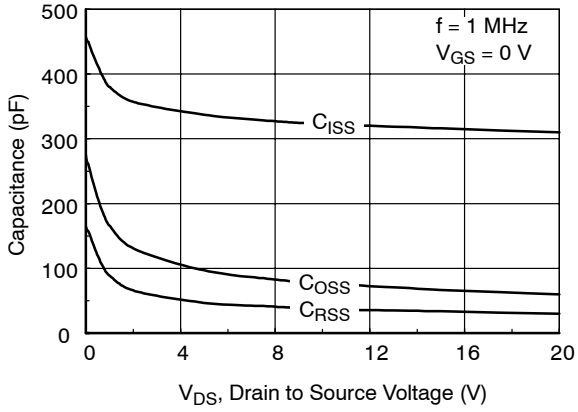


Figure 8. Capacitance Characteristics

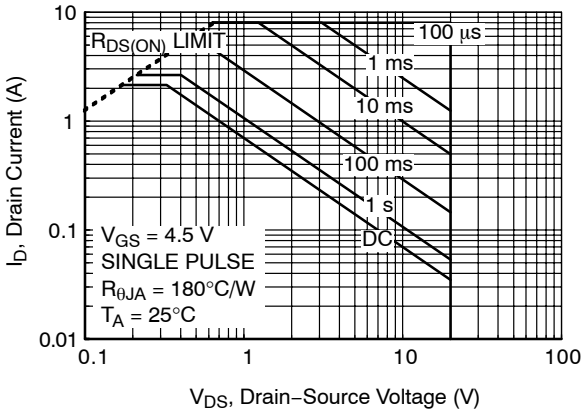


Figure 9. Maximum Safe Operating Area

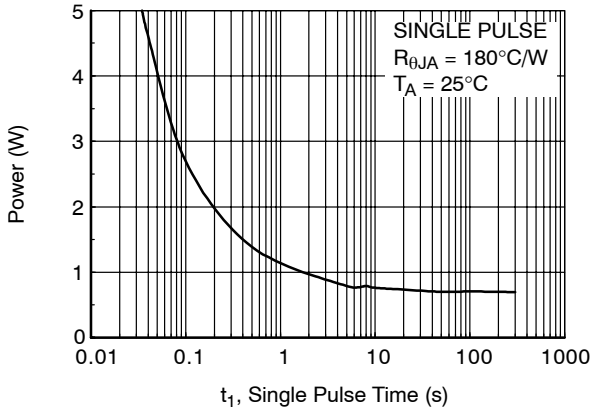


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: P−CHANNEL

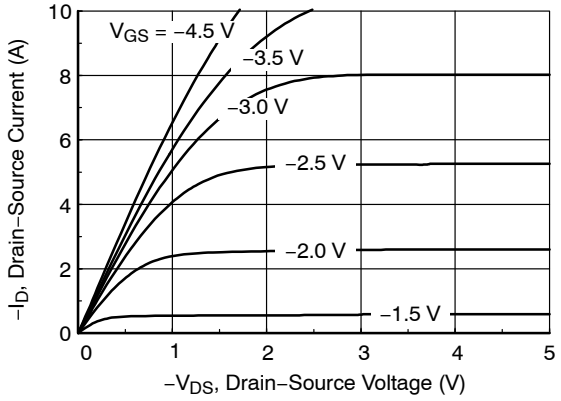


Figure 11. On−Region Characteristics

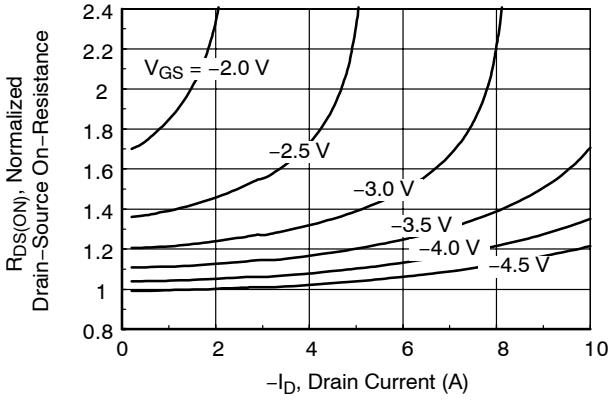


Figure 12. On−Resistance Variation with Drain Current and Gate Voltage

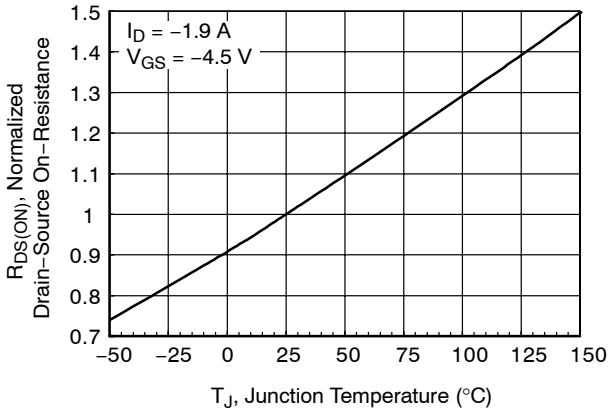


Figure 13. On−Resistance Variation with Temperature

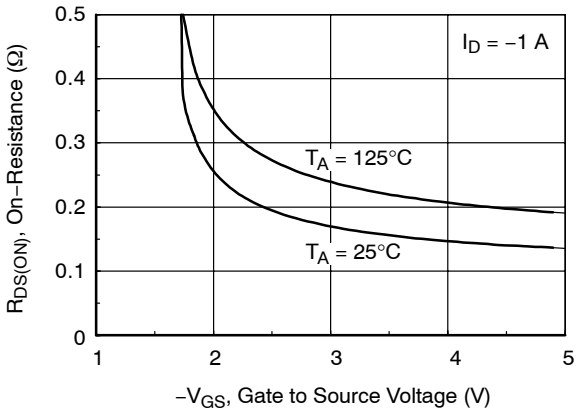


Figure 14. On−Resistance Variation with Gate−to−Source Voltage

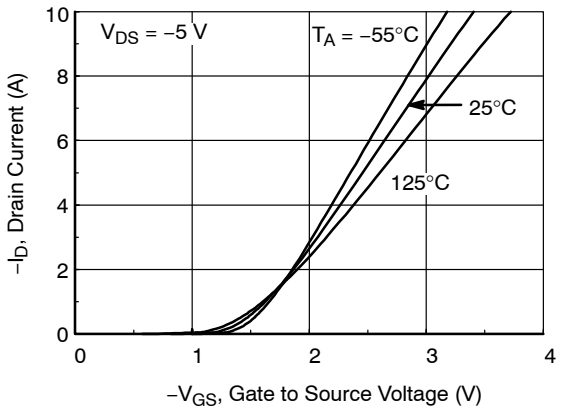


Figure 15. Transfer Characteristics

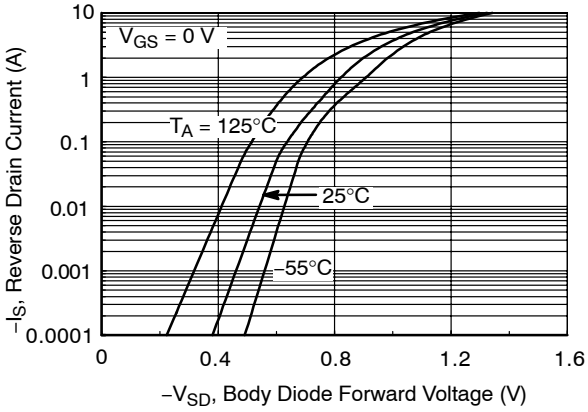


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: P−CHANNEL (continued)

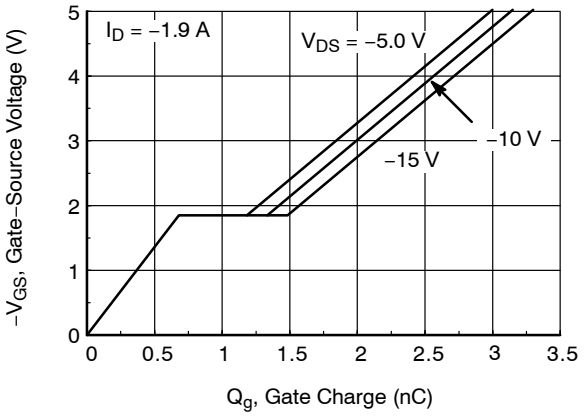


Figure 17. Gate Charge Characteristics

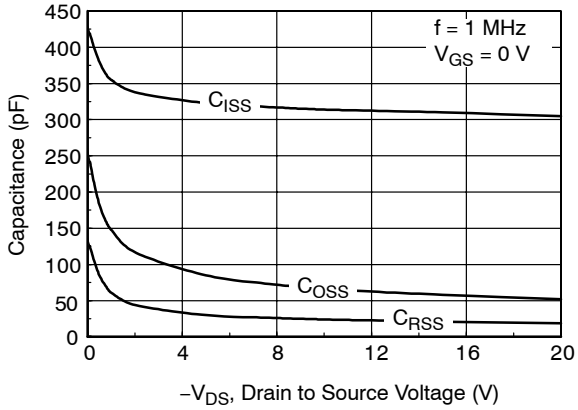


Figure 18. Capacitance Characteristics

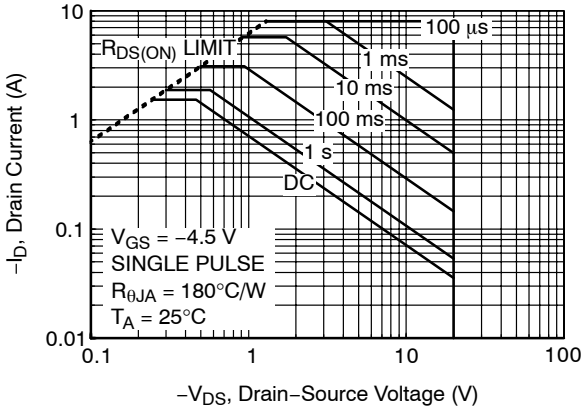


Figure 19. Maximum Safe Operating Area

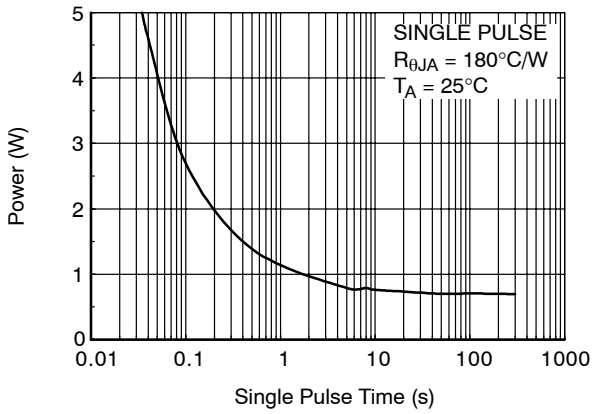


Figure 20. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: N & P−CHANNEL

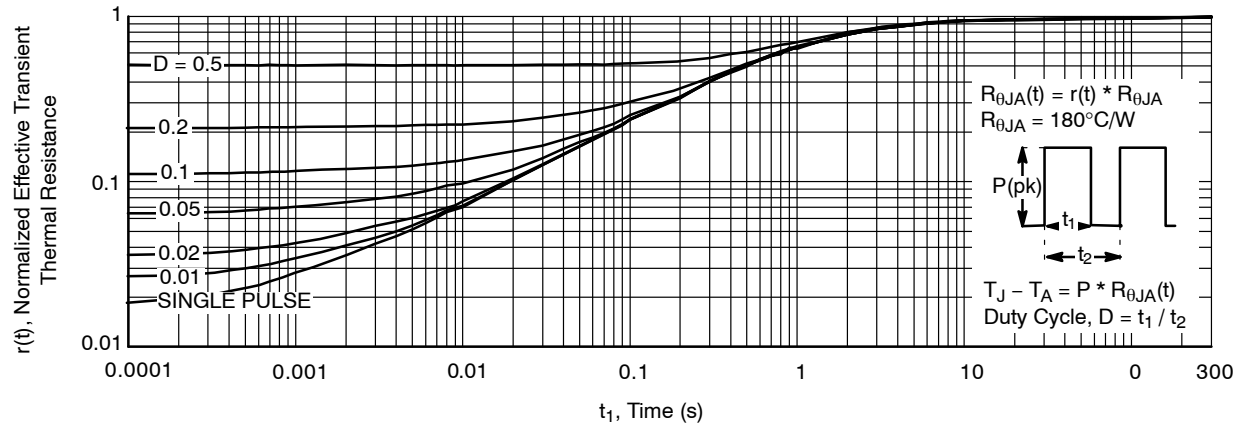


Figure 21. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

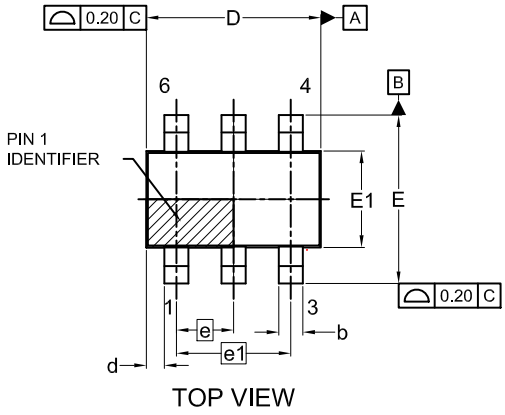
ON Semiconductor®

1

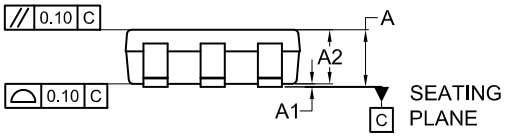
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

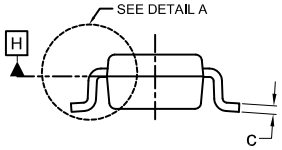


TOP VIEW

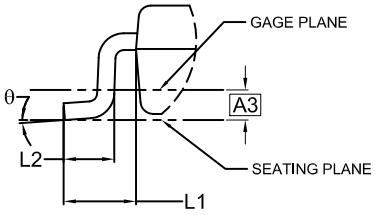


FRONT VIEW

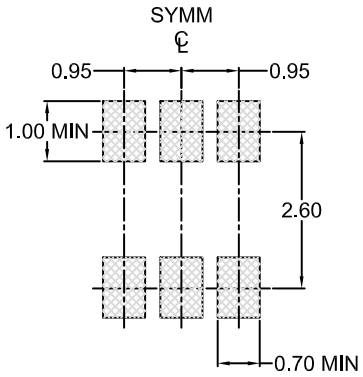
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

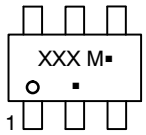
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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