

# MOSFET – N-Channel, POWERTRENCH® GreenBridge™ Series of High-Efficiency Bridge Rectifiers

60 V, 8 A, 17.5 mΩ

## FDMQ86530L

### General Description

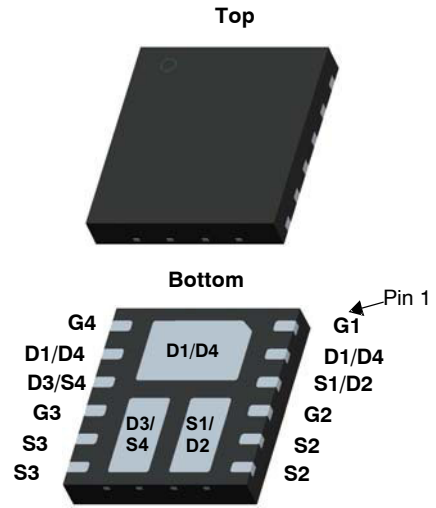
This Quad MOSFET solution provides ten-fold improvement in power dissipation over diode bridge.

### Features

- Max  $R_{DS(on)}$  = 17.5 mΩ at  $V_{GS} = 10$  V,  $I_D = 8$  A
- Max  $R_{DS(on)}$  = 23 mΩ at  $V_{GS} = 6$  V,  $I_D = 7$  A
- Max  $R_{DS(on)}$  = 25 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 6.5$  A
- Substantial Efficiency Benefit in PD Solutions
- This Device is Pb-Free, Halide Free, and RoHS Compliant

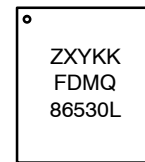
### Applications

- Active Bridge
- Diode Bridge Replacement in 24 V & 48 V AC Systems

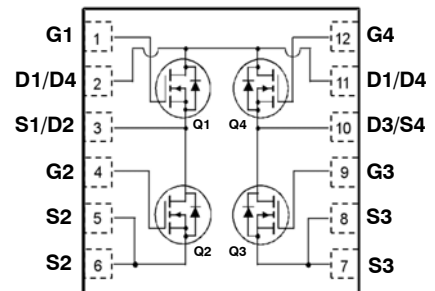


MLP 4.5x5

### MARKING DIAGRAM



Z = Assembly Plant Code  
 XY = Data Code (Year and Week)  
 KK = Lot Traceability Code  
 FDMQ86530L = Specific Device Code



### ORDERING INFORMATION

Device	Package	Shipping†
FDMQ86530L	WDFN-12 (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

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## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DS}$	Drain to Source Voltage	60	V	
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V	
$I_D$	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$	
		Pulsed		
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	22	W
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	1.9	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	135	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	27	-	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	-	-6	-	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$	-	12	17.5	m $\Omega$
		$V_{GS} = 6 \text{ V}, I_D = 7 \text{ A}$	-	15	23	
		$V_{GS} = 4.5 \text{ V}, I_D = 6.5 \text{ A}$	-	20	25	
		$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}, T_J = 125^\circ\text{C}$	-	18	26	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 8 \text{ A}$	-	28	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	1725	2295	pF
$C_{oss}$	Output Capacitance		-	299	400	
$C_{rSS}$	Reverse Transfer Capacitance		-	10	15	

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 8 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	-	8.8	18	ns
$t_r$	Rise Time		-	3.8	10	
$t_{d(off)}$	Turn-Off Delay Time		-	22	35	
$t_f$	Fall Time		-	2.8	10	

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}, V_{DD} = 30\text{ V}, I_D = 8\text{ A}$	-	23	33	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}, V_{DD} = 30\text{ V}, I_D = 8\text{ A}$	-	11	16	
$Q_{gs}$	Gate to Charge	$V_{DD} = 30\text{ V}, I_D = 8\text{ A}$	-	5.1	-	
$Q_{gd}$	Gate to Drain "Miller" Charge		-	2.3	-	

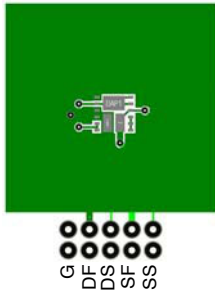
## DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 8\text{ A}$ (Note 2)	-	0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 1.6\text{ A}$ (Note 2)	-	0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	27	43	ns
$Q_{rr}$	Reverse Recovery Charge		-	12	22	nC

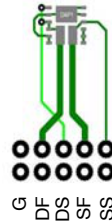
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $65^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper the board designed Q1 + Q3 or Q2 + Q4.



b.  $135^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper the board designed Q1 + Q3 or Q2 + Q4.

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

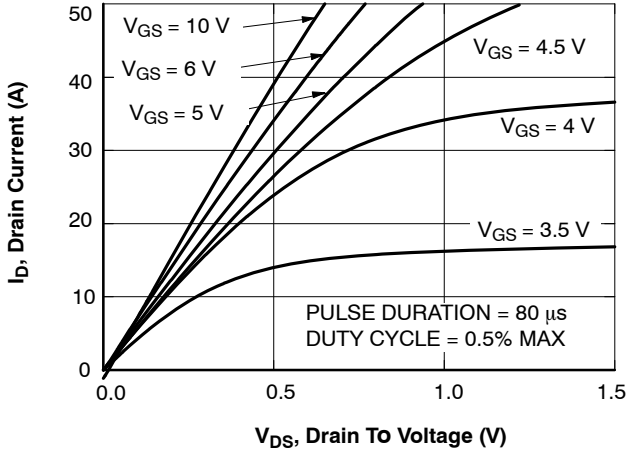


Figure 1. On-Region Characteristics

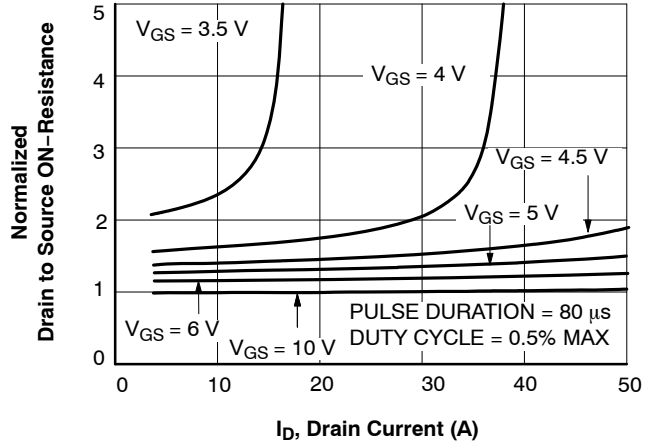


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

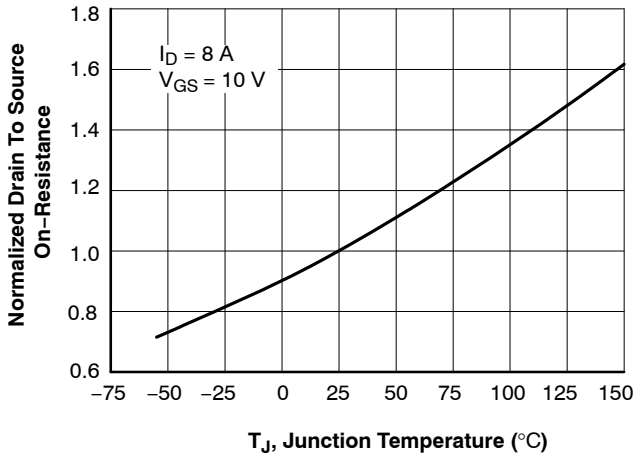


Figure 3. Normalized On-Resistance vs Junction Temperature

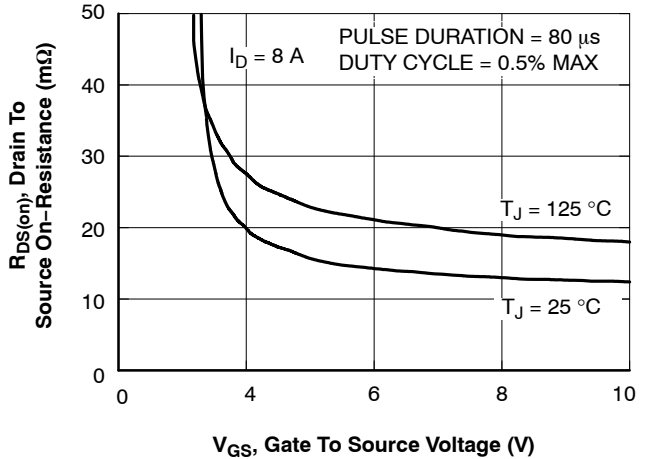


Figure 4. On-Resistance vs Gate to Source Voltage

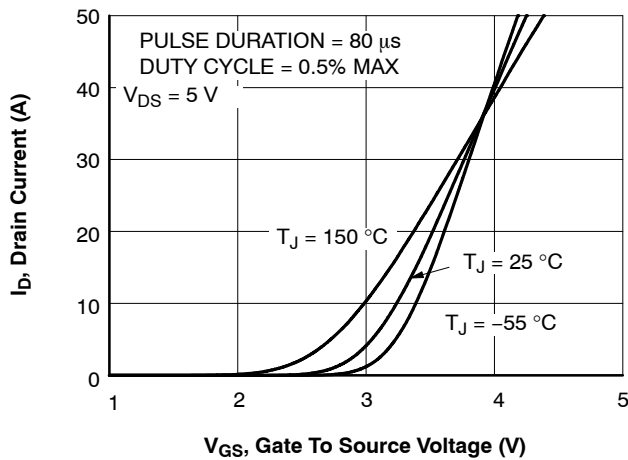


Figure 5. Transfer Characteristics

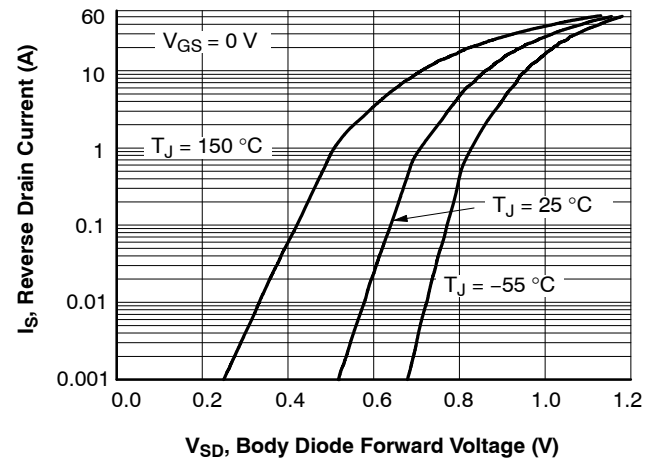


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

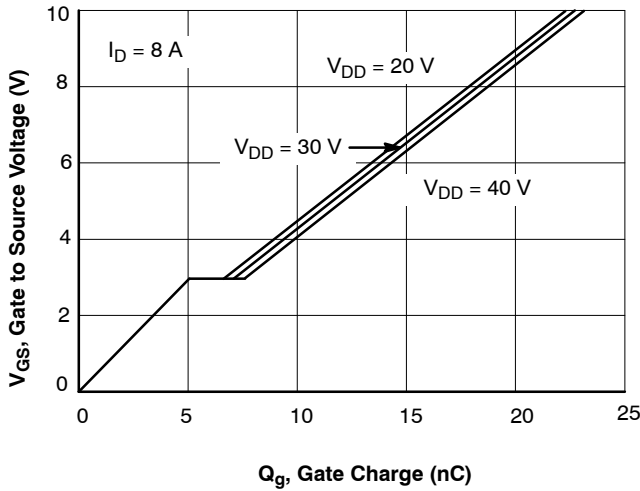


Figure 7. Gate Charge Characteristics

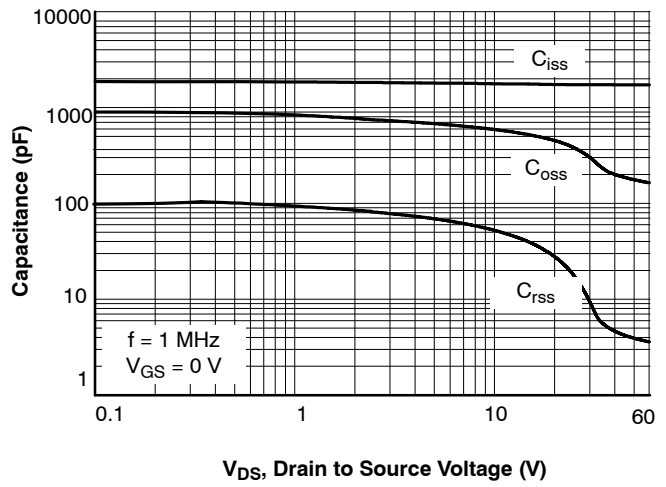


Figure 8. Capacitance vs Drain to Source Voltage

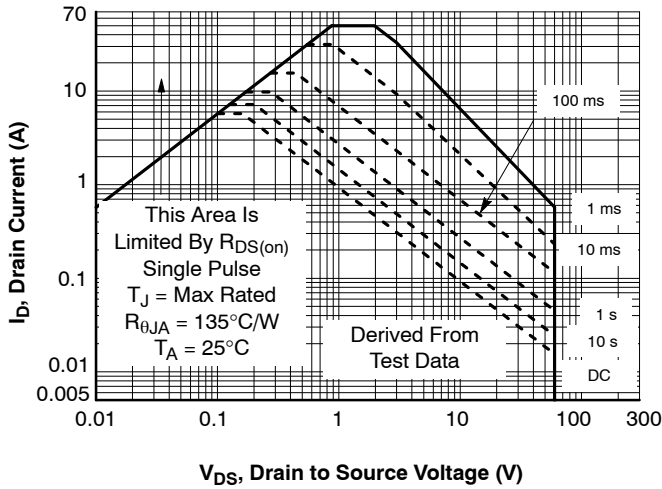


Figure 9. Forward Bias Safe Operating Area

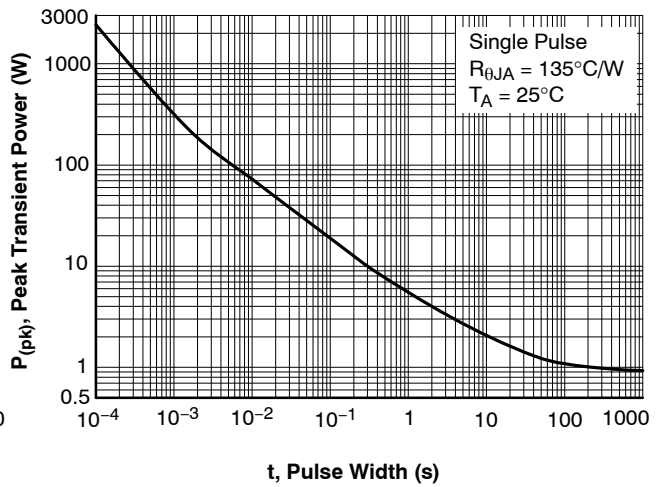


Figure 10. Single Pulse Maximum Power Dissipation

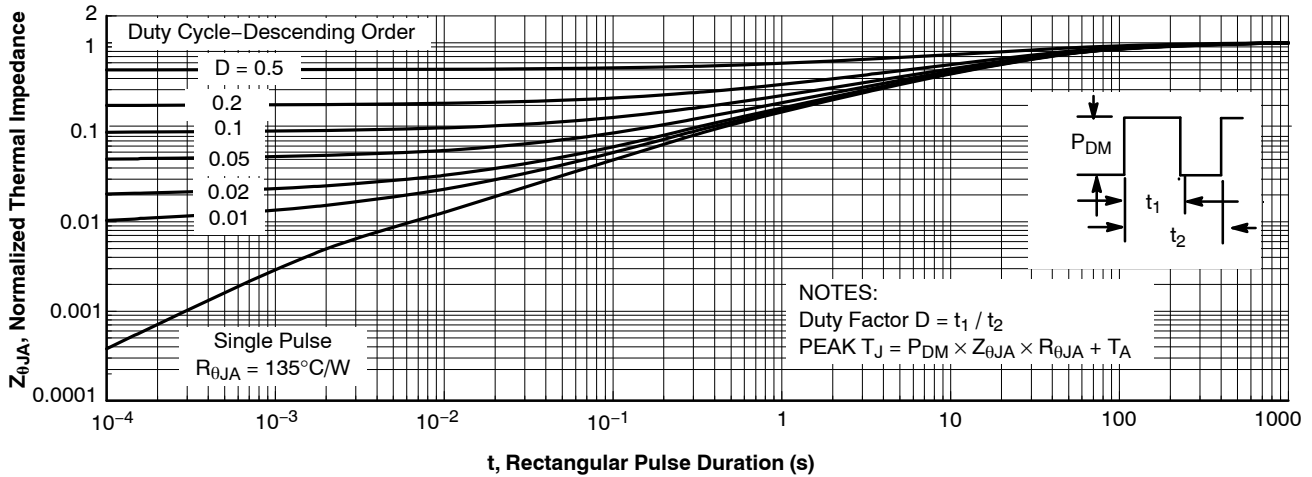


Figure 11. Junction-to-Ambient Transient Thermal Response Curve



# MECHANICAL CASE OUTLINE

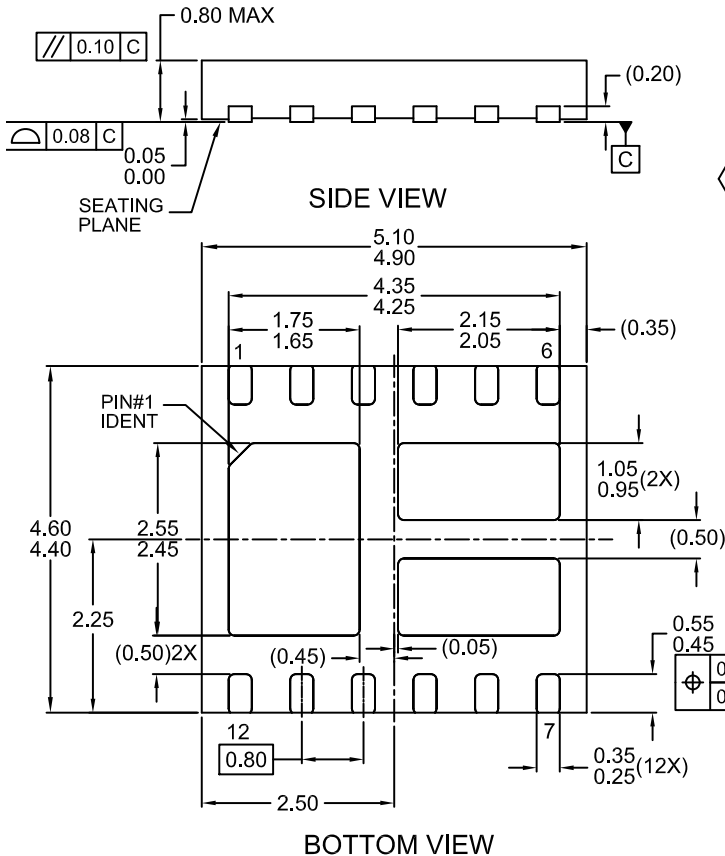
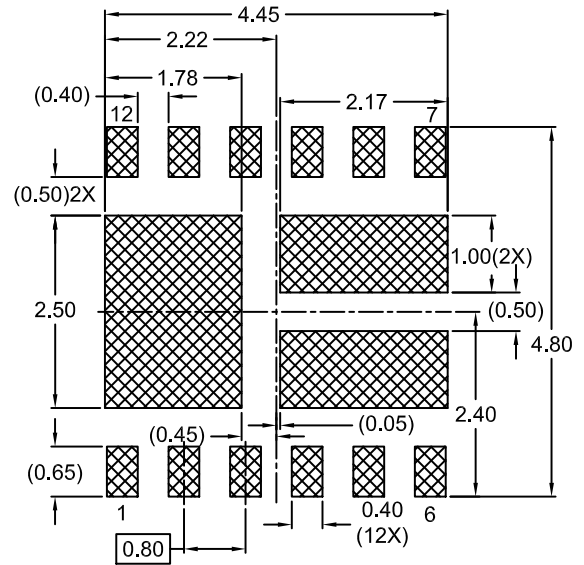
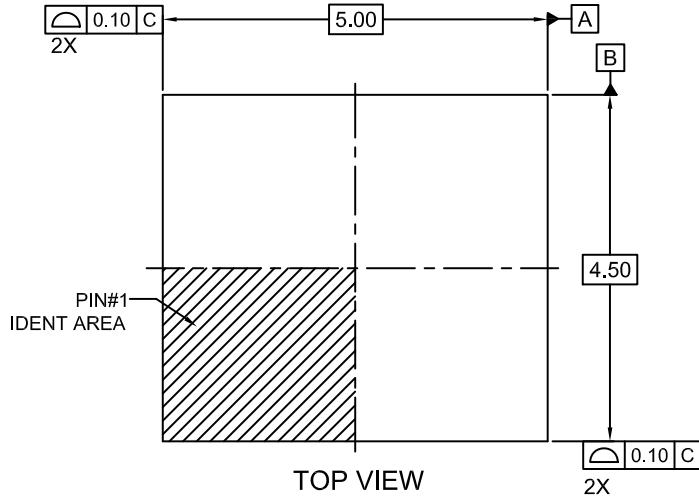
## PACKAGE DIMENSIONS

ON Semiconductor®



### WDFN12 5x4.5, 0.8P CASE 511CR ISSUE A

DATE 21 MAR 2017



**NOTES:**

- A. THIS MKT. DWG. DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

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