

# MOSFET - N-Channel, Shielded Gate, POWER trench<sup>®</sup>

100 V, 80 A, 4.85 mΩ

## FDMS86150A

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWER trench process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

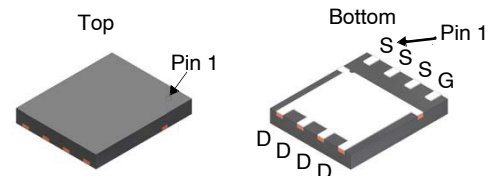
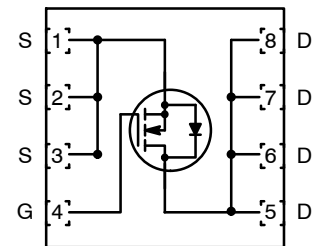
### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 4.85 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 16 \text{ A}$
- Max  $r_{DS(on)} = 7.8 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 13 \text{ A}$
- Advanced Package and Silicon Combination for Low  $r_{DS(on)}$  and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free and are RoHS Compliant

### Applications

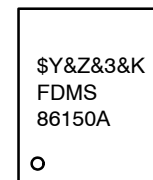
- Primary DC-DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch

### N-CHANNEL MOSFET



PQFN8 5X6, 1.27P  
Power 56  
CASE 483AF

### MARKING DIAGRAM



\$Y = onsemi Logo  
&Z = Assembly Plant Code  
&3 = 3-Digit Date code  
&K = 2-Digits Lot Run Traceability Code  
FDMS86150A = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS86150A

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

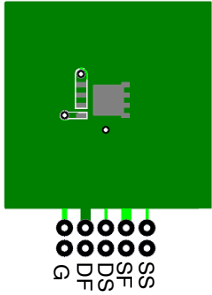
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current –Continuous $T_C = 25^\circ\text{C}$	80	A
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	16	
	–Pulsed (Note 3)	300	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	726	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	113	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

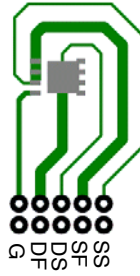
## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $45^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b)  $115^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2.  $E_{AS}$  of 726 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3$  mH,  $I_{AS} = 22$  A,  $V_{DD} = 100$  V,  $V_{GS} = 10$  V, 100% test at  $L = 0.1$  mH,  $I_{AS} = 69$  A.  
 3. Pulse  $I_D$  measured at  $t_d = 250$   $\mu\text{s}$ , refer to Fig 11 SOA graph for more details.

## ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMS86150A	FDMS86150A	PQFN8 5X6, 1.27P Power 56 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDMS86150A

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C	–	72	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25 °C	–	–10	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16 A	–	4.2	4.85	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 13 A	–	6	7.8	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 16 A, T <sub>J</sub> = 125 °C	–	7.8	9.1	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 16 A	–	53	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	3330	4665	pF
C <sub>oss</sub>	Output Capacitance		–	703	985	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	20	45	pF
R <sub>g</sub>	Gate Resistance		0.1	0.7	3.6	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 16 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	21	34	ns
t <sub>r</sub>	Rise Time		–	8.6	17	ns
t <sub>d(off)</sub>	Turn-off Delay Time		–	28	45	ns
t <sub>f</sub>	Fall Time		–	6	12	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 16 A	–	47	66	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 5 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 16 A	–	25	35	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 16 A	–	14	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 16 A	–	9.7	–	nC

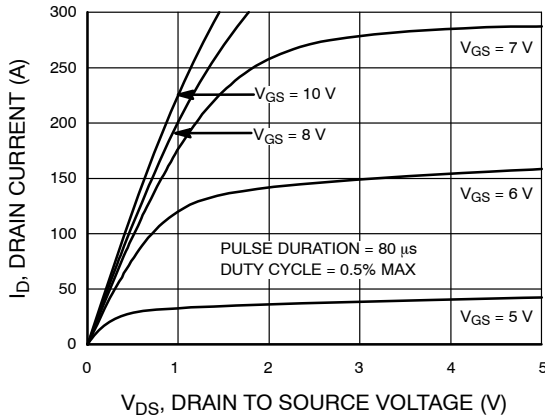
### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.1 A (Note 4)	–	0.69	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 16 A (Note 4)	–	0.78	1.3	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 16 A, di/dt = 100 A/μs	–	64	102	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	86	138	nC

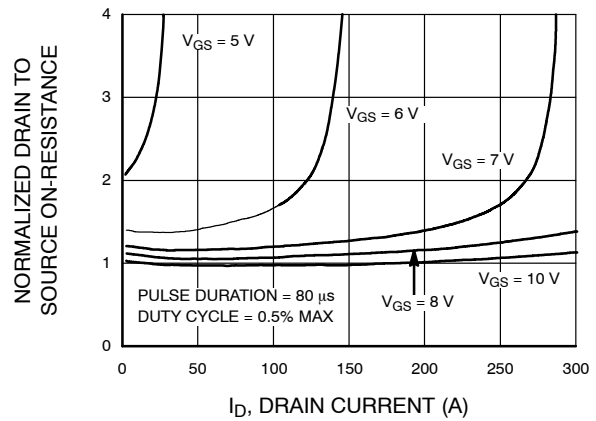
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width <300 μs, Duty cycle <2.0%.

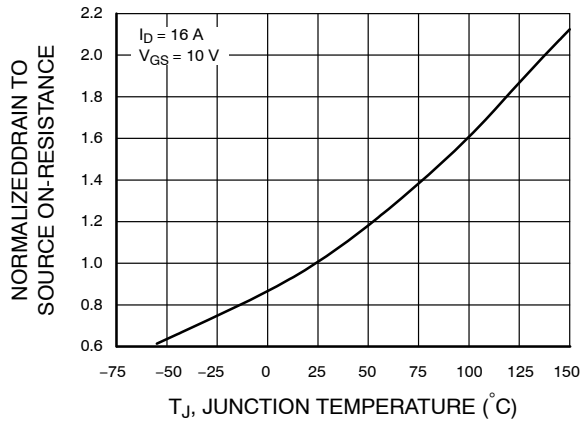
**TYPICAL CHARACTERISTICS**  
( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



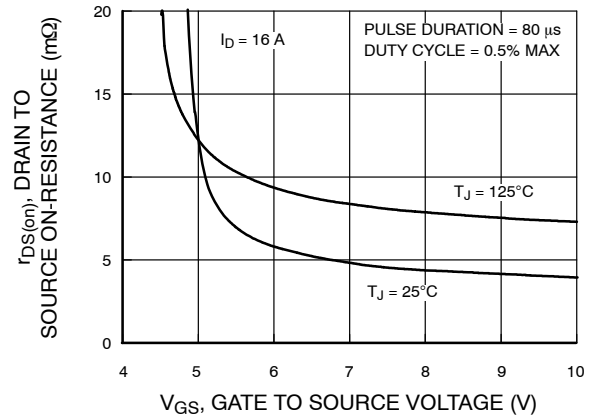
**Figure 1. On Region Characteristics**



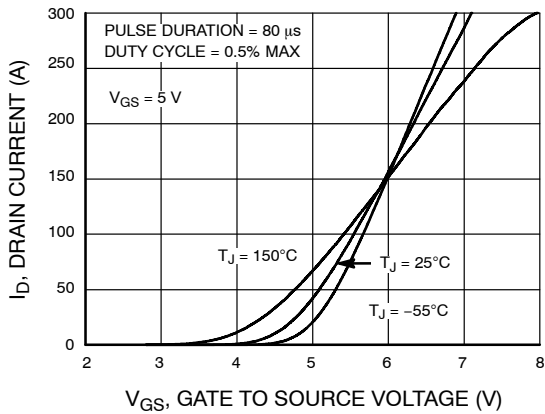
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



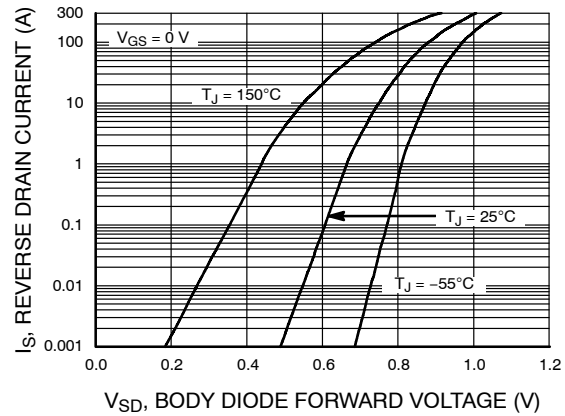
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**



**Figure 5. Transfer Characteristics**



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

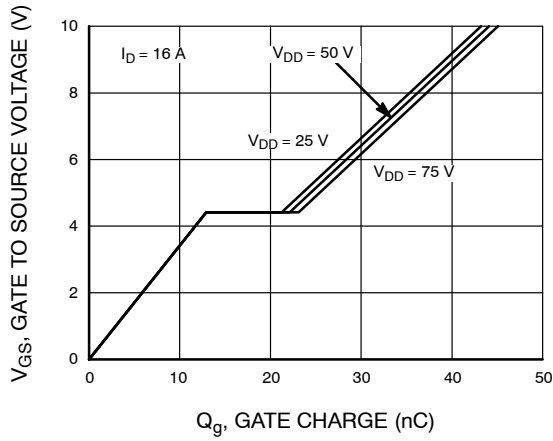


Figure 7. Gate Charge Characteristics

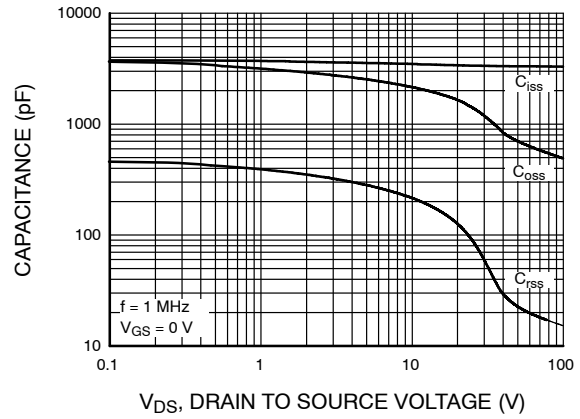


Figure 8. Capacitance vs Drain to Source Voltage

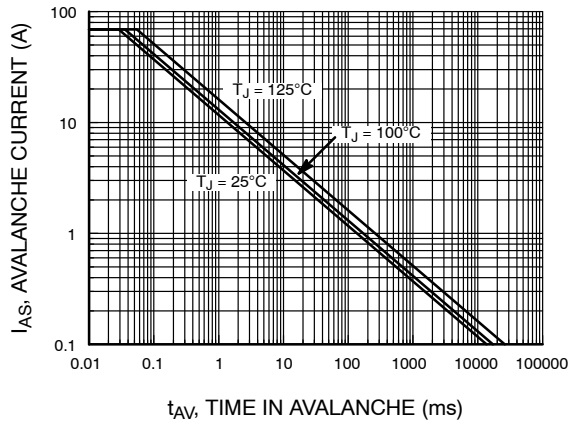


Figure 9. Unclamped Inductive Switching Capability

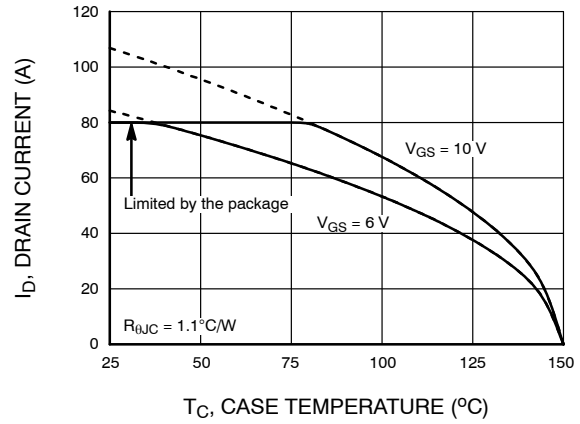


Figure 10. Maximum Continuous Drain Current vs Case Temperature

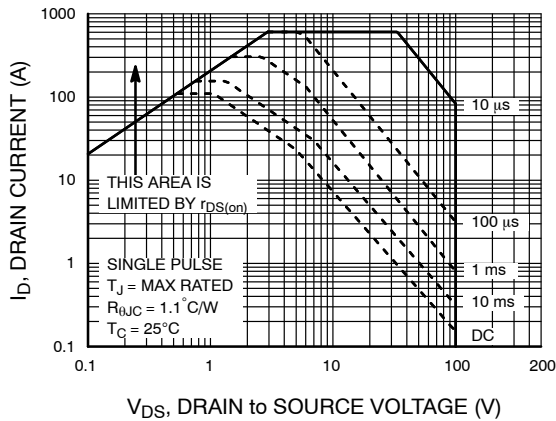


Figure 11. Forward Bias Safe Operating Area

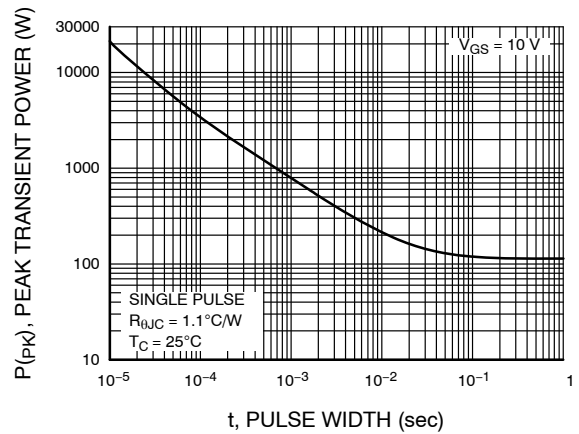


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

( $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted) (continued)

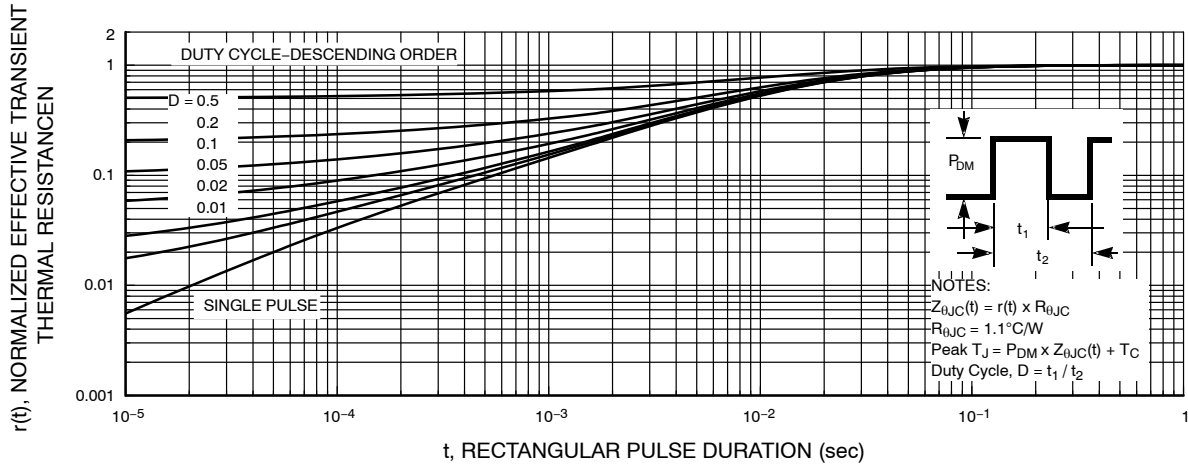


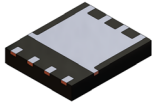
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

# FDMS86150A

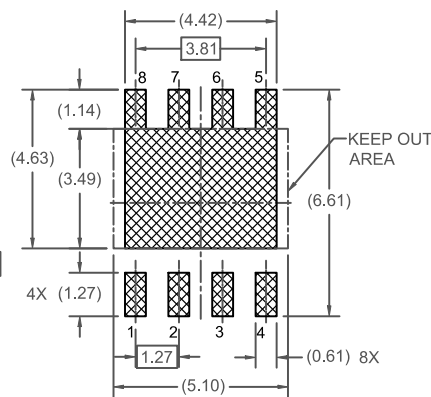
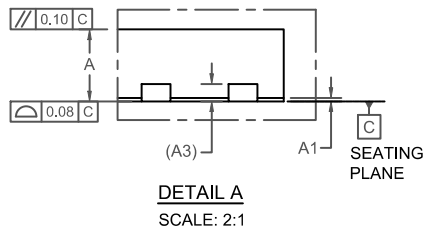
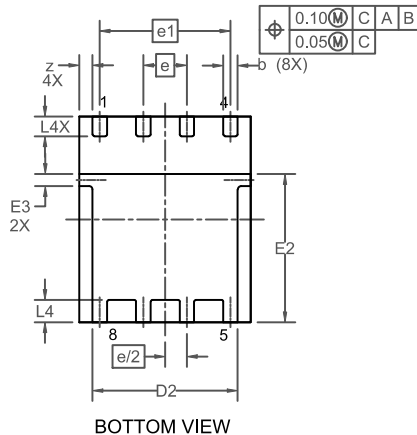
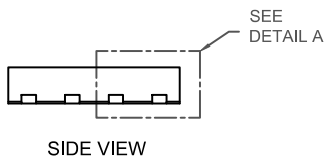
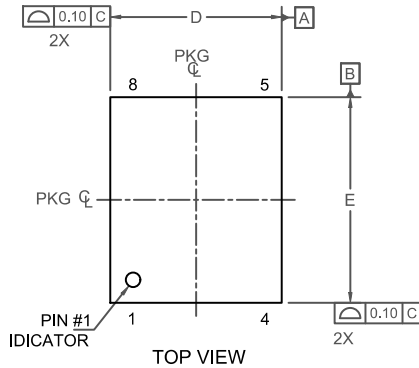
## REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the Data Sheet to <b>onsemi</b> format.	09/04/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.


**PQFN8 5X6, 1.27P**  
**CASE 483AF**  
**ISSUE A**

DATE 06 JUL 2021


**LAND PATTERN**  
**RECOMMENDATION**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE:  
JEDEC MO-240, ISSUE A, VAR. AA,  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.  
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	4.23	4.33	4.43
E3	0.35 REF.		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
L	0.52	0.57	0.62
L4	0.55	0.65	0.75
z	0.38 REF		

**DOCUMENT NUMBER:** 98AON13656G

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**PAGE 1 OF 1**

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