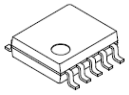
Constant-Voltage Primary-Side-Regulation PWM Controller for Power Factor Correction

FL7740



SOIC10
CASE 751EE

Description

The FL7740 provides accurate CV regulation in the steady state with differentiated dynamic function to minimize overshoot and undershoot of output voltage in line and load transient condition. Standby power is less than 0.3 W for smart lighting application and power factor is higher than 0.9 even at half load condition when enabling PF optimizer for wide output power scalability.

Startup time is less than 0.2 sec with built−in high voltage startup circuit and output voltage quickly reaches to the target CV level by loop gain transition technique during startup.

Various protections such as Overload, output diode short, sensing resistor short, output short and output over voltage protection guarantee high system reliability.

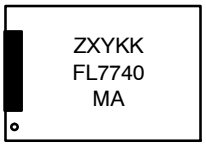
Features

- Wide Universal Input Range (90 V_{AC} ~ 305 V_{AC})
- Precise CV Regulation in the Steady State: < ±3 %
- CV Regulation in the load Transient: < ±10 %
- Overshoot−Less Fast HV Start Up Time (< 0.2 s)
- Low Standby Power
- PF Higher than 0.9 at High−Line and Half load by PF Optimizer
- Pulse−by−Pulse Current Limit
- Output Short Protection
- Output Over Voltage Protection
- Output Diode Short Protection
- Sensing Resistor Short & Open protection
- Over Load Protection
- These Devices are Pb−Free Devices

Typical Applications

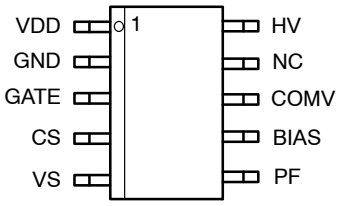
- LED Lighting System
- AC−DC Adapters, TVs, Monitors
- Off Line Appliances Requiring Power Factor Correction

MARKING DIAGRAM



Z = Plant code
X = 1 digit year code
Y = 1 digit week code
KK = 2 digit lot traceability code
M = Package code
A = Product version

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

BLOCK DIAGRAM

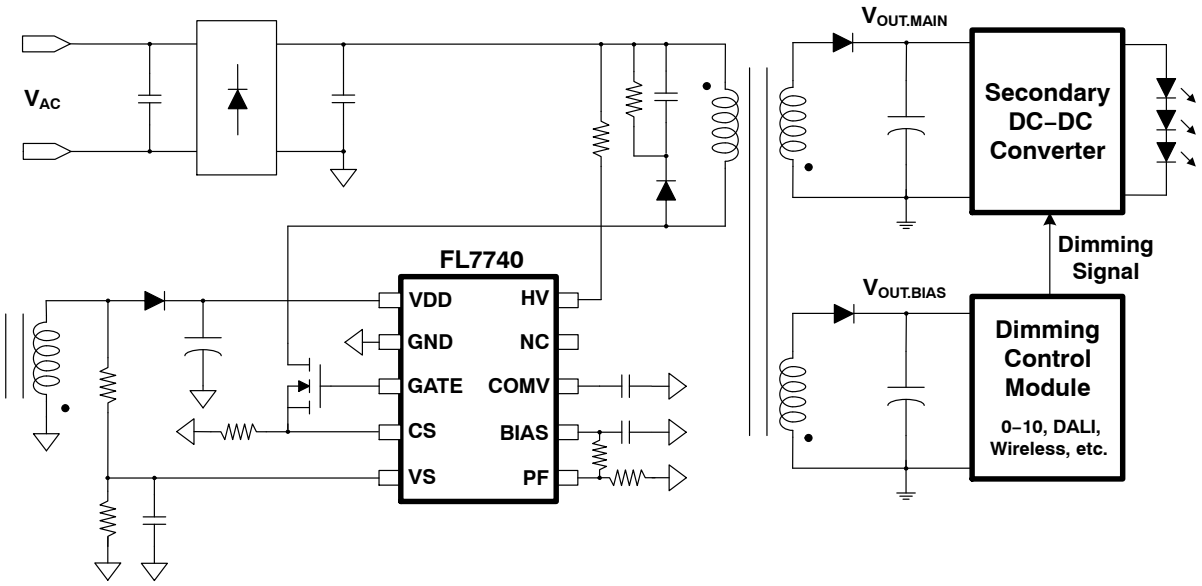


Figure 1. Application Schematic

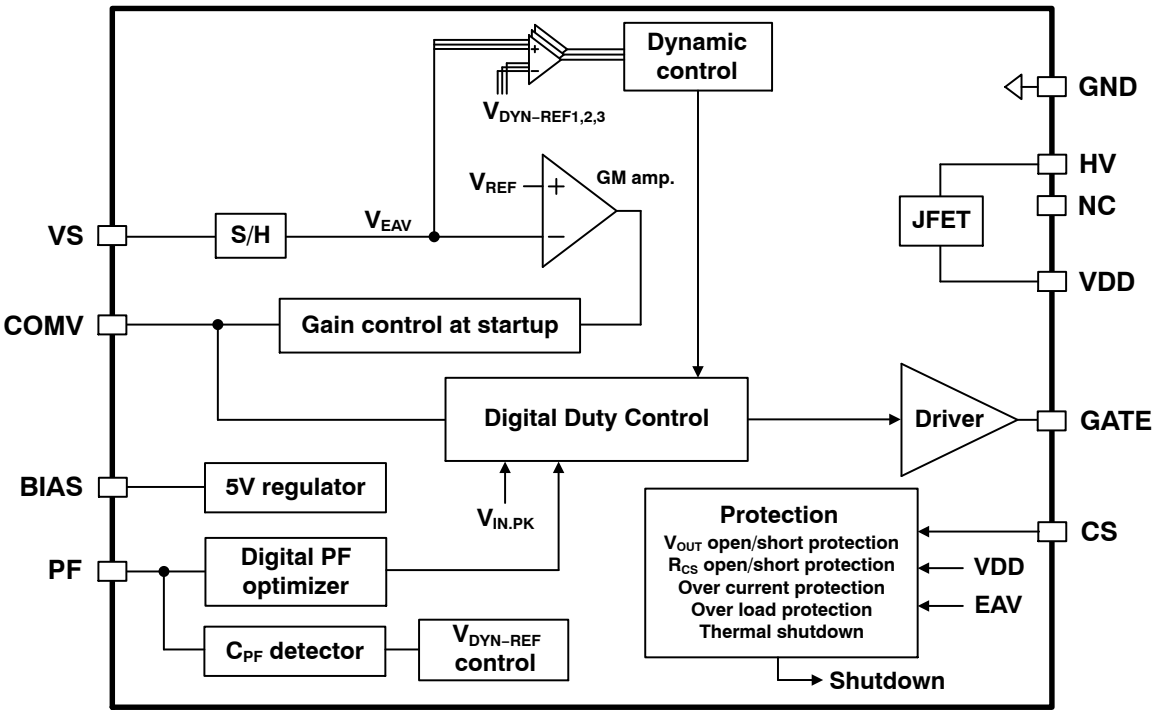


Figure 2. Simplified Block Diagram

FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	VDD	IC Supply	IC operating current and MOSFET driving current are supplied using this pin.
2	GND	Ground	Controller ground pin.
3	GATE	PWM Driver Output	This pin uses the internal totem−pole output driver to drive the power MOSFET.
4	CS	Current Sense	Connected to a current sense resistor to detect the MOSFET current for pulse−by− pulse current limit.
5	VS	Voltage Sense	This pin is connected to the auxiliary winding of the transformer via a resistor divider to detect the output voltage.
6	PF	Power Factor	This pin is connected to a resistor to optimize power factor.
7	BIAS	Internal Circuit BIAS	Bypass pin for the internal supply, which powers all control circuitry on the IC.
8	COMV	Loop Compensation	This pin is connected to a capacitor between COMV and GND for compensation.
9	NC	No Connection	
10	HV	High Voltage	This pin is connected to the rectified input voltage via a resistor for fast startup.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Units
$V_{HV(MAX)}$	HV Pin Voltage Range	560	V
$V_{MV(MAX)}$	VDD, GATE Pin Voltage Range	−0.3 to 30	V
$V_{LV(MAX)}$	COMV, PF, BIAS, VS, CS Pin Voltage Range	−0.3 to 6	V
$V_{LV(PULSE)}$	VS, CS Pin Negative Pulse Voltage at I_{LV} < 0.2 A and t_{PULSE} < 300 ns	−1.5	V
$P_{D(MAX)}$	Maximum Power Dissipation (T_A < 50°C)	663	mW
$T_{J(max)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
$R_{\theta JA}$	Junction−to−Ambient Thermal Impedance	158	°C/W
$R_{\theta JC}$	Junction−to−Case Thermal Impedance	39	°C/W
ESD_{HBM}	ESD Capability, Human Body Model (Note 2)	2	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 2)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 18 V and T_J = −40 ~ 125°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDD Section						
V_{DD-ON}	Turn−On Threshold Voltage		14.5	16.0	17.5	V
V_{DD-OFF}	Turn−Off Threshold Voltage		6.75	7.75	8.75	V
I_{DD-OP}	Operating Current	C_{LOAD} = 1 nF, V_{DD} = 18V	3	5	6.5	mA
I_{DD-AR}	Operating Current during Auto Restart		0.3		1	mA
V_{DD-OVP}	V_{DD} Over−Voltage−Protection		24	25	26	V
V_{BIAS}	V_{BIAS} Voltage		4.85	5.00	5.15	V
GATE Section						
V_{OL}	Output Voltage Low				0.2	V
V_{OH}	Output Voltage High	V_{DD} = 18 V	17.8			V
I_{source}	Peak Sourcing Current	Design guaranteed C_{LOAD} = 1 nF, V_{DD} = 20 V C_{LOAD} = 1 nF, V_{DD} = 23 V		 180 210		mA
I_{sink}	Peak Sinking Current	Design guaranteed C_{LOAD} = 1 nF, V_{DD} = 20 V C_{LOAD} = 1 nF, V_{DD} = 23 V		 385 435		mA
t_r	Rising Time	C_{LOAD} = 1 nF	110	150	190	ns
t_f	Falling Time	C_{LOAD} = 1 nF	40	60	80	ns
HW Section						
I_{HV}	Supply Current From HV Pin	V_{HV} = 560 V, V_{DD} = 0 V	3		9	mA

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 18 V and T_J = −40 ~ 125°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HW Section						
I_{HV-LC}	Leakage Current after Startup			1	10	μA
t_{R-JFET}	JFET Regulation Time at Startup	Design guaranteed	400	500	600	ms
$V_{DD-JFET-HL}$	V_{DD} High Limit during JFET Regulation		17.5	19.0	20.5	V
$V_{DD-JFET-LL}$	V_{DD} Low Limit during JFET Regulation		15.5	17.0	18.5	V
PWM Section						
$T_{ON-MIN-MIN}$	Min. Turn−on Time Min. Limit	Design guaranteed		0.40		μs
$T_{ON-MIN-MAX}$	Min. Turn−on Time Max. Limit	Design guaranteed		2.0		μs
T_{ON-MAX}	Max. Turn−on Time	Design guaranteed		23.3		μs
Oscillator Section						
f_{MAX}	Max. Frequency		60	65	70	kHz
f_{MIN}	Min. Frequency		0.72	0.80	0.88	kHz
Current Sense Section						
t_{LEB}	Leading−Edge Blanking Time	Design guaranteed		300		ns
t_{PD}	Propagation Delay to GATE	Design guaranteed	50	100	150	ns
Voltage Sense Section						
$t_{DIS-BNK}$	t_{DIS} Blanking Time at VS Sampling	Design guaranteed	0.95	1.00	1.05	μs
$V_{VS-CLAMP}$	VS Clamping Voltage	I_{VS}=1 mA I_{VS}=10 μA	−0.1		0.35	V
V_{REF}	Reference Voltage		3.465	3.5	3.535	V
$CV_{REGULATION}$	CV Regulation Tolerance	V_{VS} = 3.5 V, T_J = 25°C V_{VS} = 3.5 V, T_J = −40~125°C	−0.7 −1.2		+0.7 +1.2	%
g_M	Transconductance		16	20	24	μmho
$I_{COMV-SINK}$	COMV Sink Current	V_{VS} = 4 V	8	10	12	μA
$I_{COMV-SOURCE}$	COMV Source Current	V_{VS} = 3 V	8	10	12	μA
$V_{COMV-HGH}$	COMV High Voltage		4.7			V
$V_{COMV-LOW}$	COMV Low Voltage				0.1	V
Start Sequence Section						
$t_{SOFT-START}$	Soft Start Time	Design guaranteed		25.6		ms
$t_{SS1-MIN}$	SS1 Minimum Time	Design guaranteed		2		ms
$t_{SS1-MAX}$	SS1 Maximum Time	Design guaranteed		100		ms
t_{SS21}	SS21 Time	Design guaranteed		45		ms
t_{SS22}	SS22 Maximum Time	Design guaranteed		30		ms
Dynamic Section						
$V_{DYN-REF-SET}$	DYN Reference Set Threshold		0.72	0.80	0.88	V
$t_{DYN-REF-SET}$	DYN Reference Set Time	Design guaranteed		5		μs
$V_{OV-REF5}$	OV Reference 5	Design guaranteed		+20		%
$V_{OV-REF4}$	OV Reference 4		+14	+15	+16	%
$V_{OV-REF3}$	OV Reference 3		+9	+10	+11	%
$V_{OV-REF2}$	OV Reference 2		+4.7	+5.7	+6.7	%
$V_{OV-REF1}$	OV Reference 1		+1.86	+2.86	+3.86	%
$V_{UV-REF1}$	UV Reference 1		−3.86	−2.86	−1.86	%
$V_{UV-REF2}$	UV Reference 2		−6.7	−5.7	−4.7	%
$V_{UV-REF3}$	UV Reference 3	Design guaranteed		−10		%

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 18 V and T_J = −40 ~ 125°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Protection Section						
t_{AR}	Auto Restart Delay Time	Design guaranteed		3		s
$V_{VS-OS-H}$	'H' VS Ouptut Short Hys. Voltage		0.85	0.90	0.95	V
$V_{VS-OS-L}$	'L' VS Ouptut Short Hys. Voltage		0.65	0.70	0.75	V
$t_{OSP-DELAY}$	OSP Delay Time	Design guaranteed		35		ms
$V_{CS-HIGH-CL}$	High Current Limit Threshold		1.13	1.20	1.27	V
$V_{CS-LOW-CL}$	Low Current Limit Threshold		0.15	0.20	0.25	V
V_{CS-OCP}	Over Current Protection Voltage			1.8		V
$V_{CS-SRSP}$	CS Threshold Voltage for SRSP		0.040	0.075	0.125	V
$t_{TON-MAX-SRSP}$	Max. Turn−on Time for SRSP	I_{VS} = 100 μA I_{VS} = 700 μA	7.5 1.3	10.0 1.6	12.5 1.9	μs
T_{OTP}	Threshold Temperature for OTP	Design guaranteed		150		°C
$T_{OTP-HYS}$	Junction Temperature Hysteresis	Design guaranteed		30		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

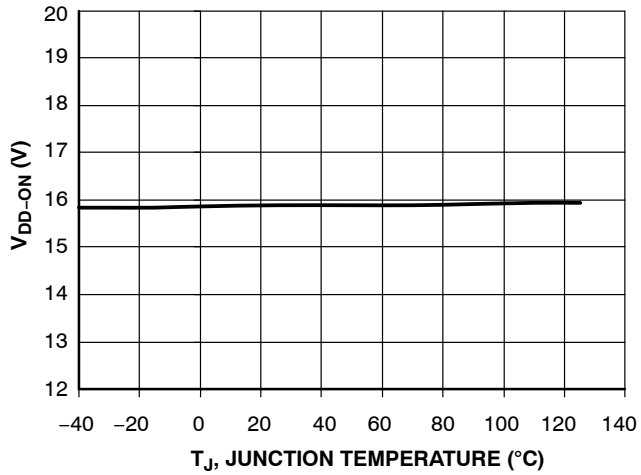


Figure 3. V_{DD-ON} vs. Temperature

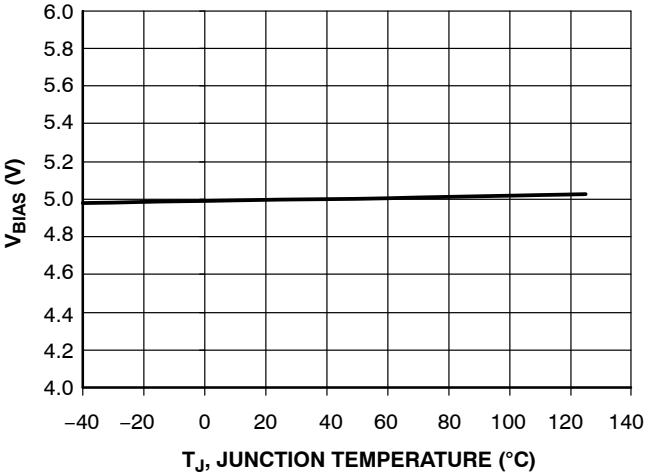


Figure 4. V_{BIAS} vs. Temperature

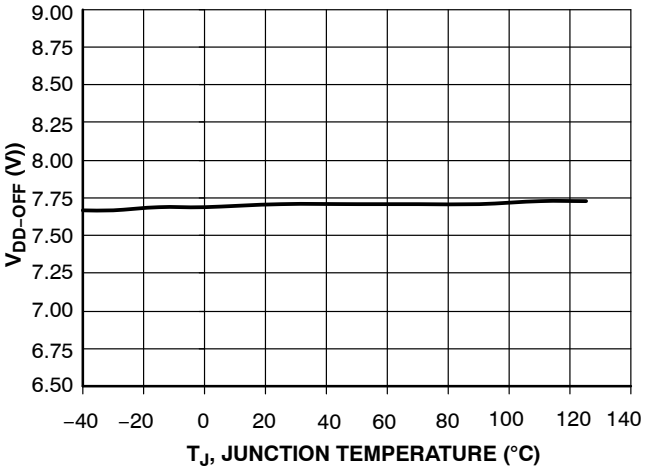


Figure 5. V_{DD-OFF} vs. Temperature

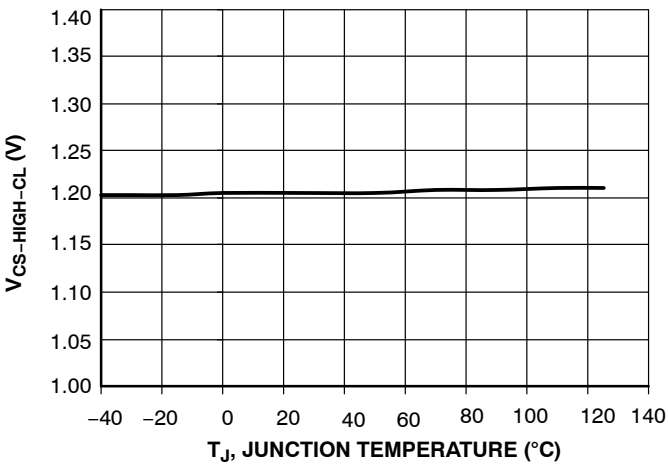


Figure 6. $V_{CS-HIGH-CL}$ vs. Temperature

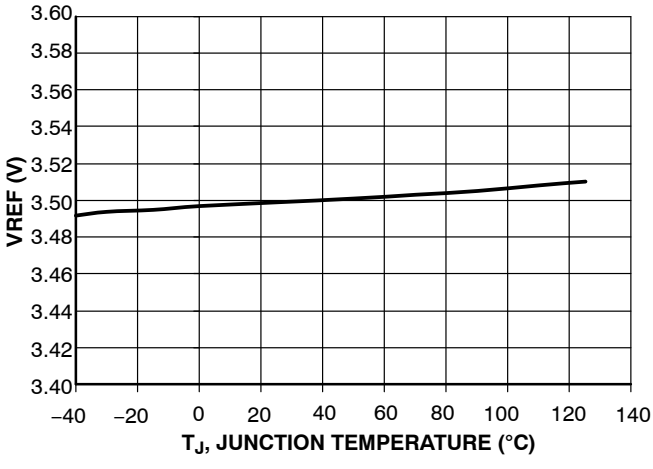


Figure 7. V_{REF} vs. Temperature

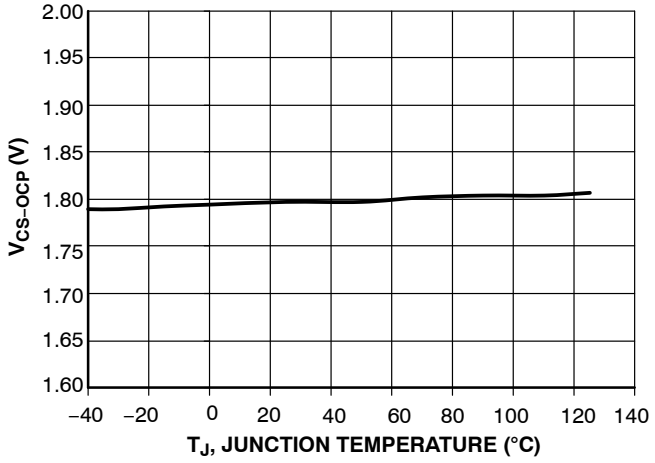


Figure 8. V_{CS-OCP} vs. Temperature

TYPICAL CHARACTERISTICS (continued)

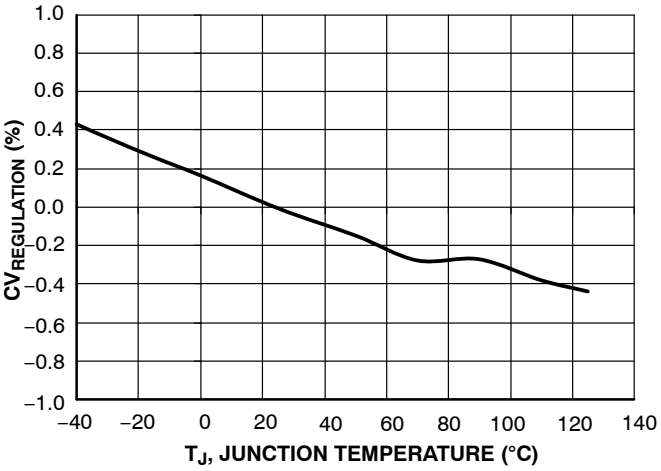


Figure 9. $CV_{REGULATIO\ N}$ vs. Temperature

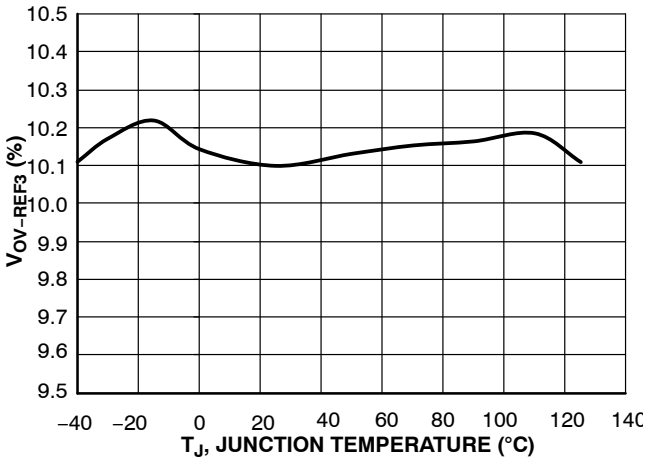


Figure 10. $VO_{V-REF}3$ vs. Temperature

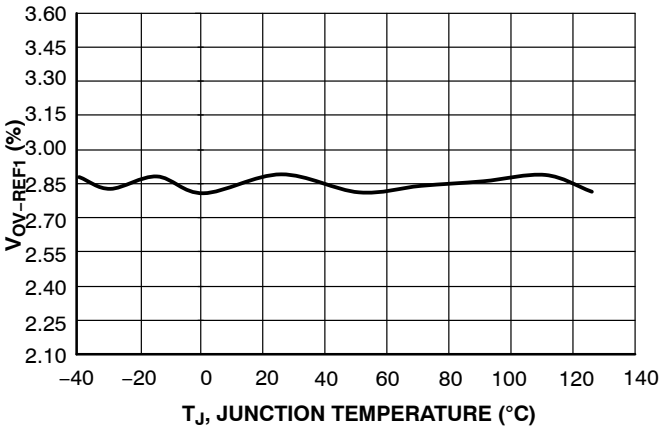


Figure 11. VOV_{-REF1} vs. Temperature

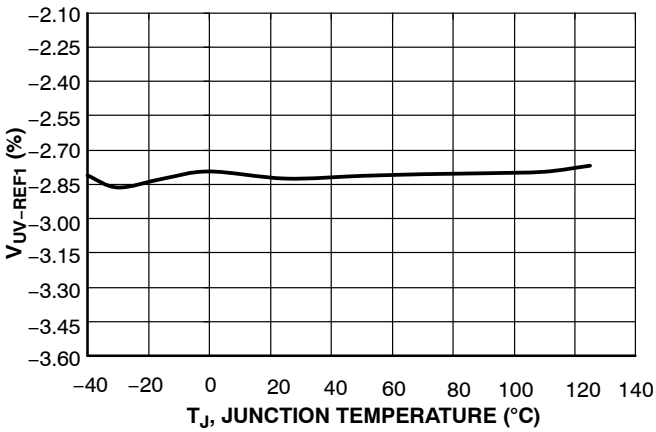


Figure 12. $V_{UV-REF1}$ vs. Temperature

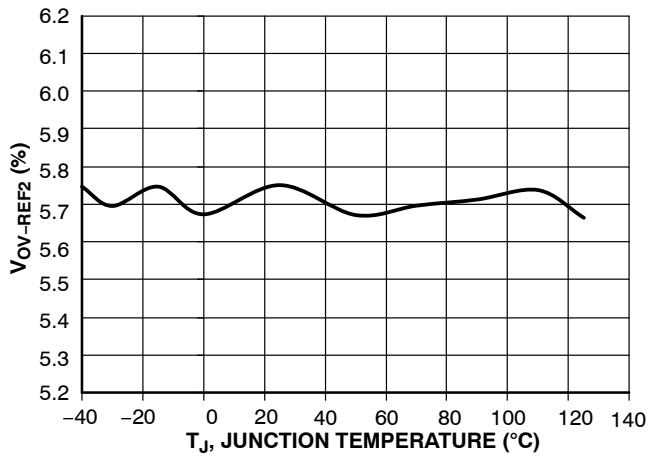


Figure 13. $V_{OV-REF2}$ vs. Temperature

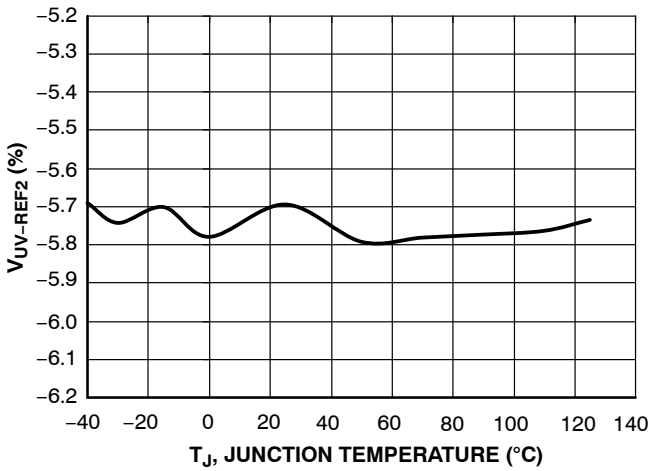


Figure 14. $V_{UV-REF2}$ vs. Temperature

APPLICATION INFORMATION

General

FL7740 is high power factor flyback controller with accurate primary side constant voltage regulation for smart LED lighting and ac−dc adapter, TV & monitors application. Precise output voltage detection and dynamic function manage good CV regulation. Startup is fast with internal HV biasing circuit with overshoot−less gain control. It guarantees high system reliable protection functions such as output over voltage, output short, over load, over current and thermal shut down protections.

Constant Voltage Regulation

VS pin detects output voltage information (= V_{EAV}) during secondary side diode conduction time and internal gm amplifier regulates the detected voltage at 3.5 V.

Dynamic Response at Load Transient

At load transient condition, V_{EAV} is shortly out of regulation due to the narrow PFC loop bandwidth. When V_{EAV} is far from 3.5 V regulation reference, duty is quickly changed to bring the V_{EAV} back to 3.5 V by dynamic control function.

HV Biasing at Startup

Internal HV biasing circuit quickly charges external VDD capacitor to begin IC operation at plug−in. After 500 ms initial time, HV biasing stops for low standby power.

Overshoot−Less Gain Control at Startup

Once IC operation starts, feedback loop is dominantly controlled in proportional gain to speed up the output capacitor charging. Once output voltage is settled down close to the regulation target, gain control is smoothly changed to integration gain with no output voltage overshoot.

Digital PF Optimizer

FL7740 compensates input current phase shift caused by EMI filter capacitor current in a half line period. With sophisticated digital PF optimizer, FL7740 significantly improves power factor in the wide load range.

Pulse−By−Pulse Current Limit

When CS pin voltage reaches to 1.2 V current limit reference, GATE turn−on is terminated to limit primary peak current.

Auto Restart at Protection

Once protection is triggered, IC operation stops for 3 sec and begin the operation for auto restart.

Output Short Protection

When V_{EAV} is less than 0.7 V continuously for 35 ms, output short protection is triggered.

Output Over Voltage Protection

When V_{EAV} is higher than $V_{VS−OVP}$ threshold or VDD is higher than $V_{DD−OVP}$, output over voltage protection is triggered.

Output Diode Short Protection

Once output diode is short circuited, high di/dt in the primary winding is occurred by leakage inductance. Once CS pin voltage reaches to 1.7 V, switching is shut down.

Sensing Resistor Short Protection

At first switching, sensing resistor short condition is monitored by detecting CS pin voltage. If CS is less than 75 mV during first GATE turn−on time, sensing resistor short protection is triggered.

Over Load Protection

When output is over loaded, pulse−by−pulse current limit event is occurred. If this event lasts for 60 half line cycles, over load protection is triggered.

Thermal Shut Down

If internal junction temperature is higher than 150°C, protection is triggered and released with 30°C hysteresis.

Primary Side Constant Voltage Regulation

FL7740 utilizes auxiliary winding to detect output voltage during secondary side diode conduction time (= T_{DIS}). The true output voltage level without secondary diode forward voltage drop is at the end of secondary diode conduction time. In order to detect the right output voltage, 85% of T_{DIS} at previous switching cycle is sampling time for V_{EAV} detection at current switching cycle.

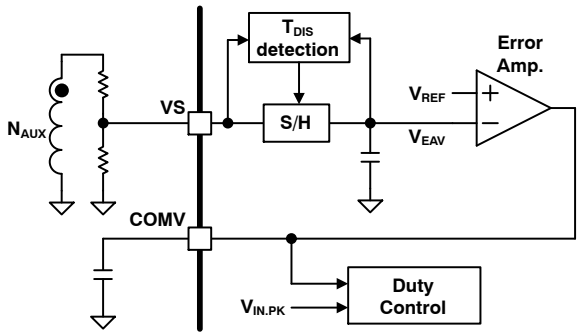


Figure 15. Primary Side Regulation

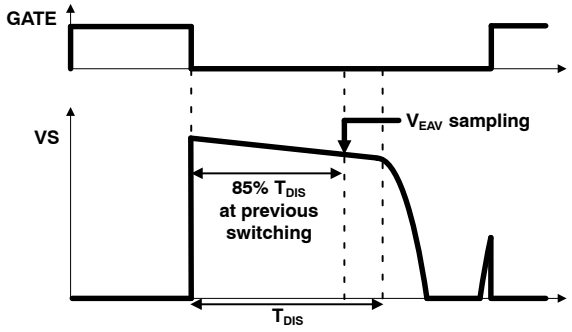


Figure 16. V_{EAV} Detection

The sampled V_{EAV} is compared with 3.5 V V_{REF} at the input of the error amplifier. Several hundreds nF capacitor is connected to the output of the error amplifier at COMV pin to keep feedback loop slow in PFC control. COMV voltage controls duty to regulate V_{EAV} same as V_{REF} in the system.

Turn−on time is controlled by both COMV voltage and $V_{IN.PK}$ information in line feedforward operation in order to keep the constant COMV voltage in the wide input voltage range. So, turn−on time is proportional to COMV voltage and inversely proportional to $V_{IN.PK}$.

Startup

After plug−in, external VDD capacitor is quickly charged by internal HV biasing supply. Even after VDD is higher than 16 V V_{DD-ON}, internal HV biasing is still enabled for 500 ms, so HV biasing can relieve VDD capacitor discharging until auxiliary winding builds up VDD voltage.

In order to speed up large output capacitor charging without overshoot, FL7740 starts with proportional gain during startup sequence (SS1 + SS2) by using internal resistive load at the output of the error amplifier.

In SS1, CCM prevent operation is enabled for the initial 2 ms. When output voltage is 0 V, deep CCM could be entered at initial startup and CS could touch OCP level with startup failure. So, pulse−by−pulse current limit is 0.2 V and switching frequency is 22 kHz during the 2 ms CCM prevent time. Also, duty is gradually increased for 26 ms for soft startup. Once 5 V pulled−up COMV voltage drops less than 4.5 V as V_{EAV} is close to V_{REF}, SS1 is ended. Maximum SS1 time is limited up to 100 ms.

In SS2, V_{COMV} drops from 5 V and goes into p−gain steady state in which V_{EAV} is little bit lower than V_{REF} due to the error amplifier input error in p−gain. Once p−gain steady state is settled down in 45 ms, SS2 is finished at min. V_{COMV} range not to make overshoot when transitioning to i−gain after SS2. FL7740 ends SS2 by monitoring V_{IN} 1.5 ms after $V_{IN.PK}$ detection moment where V_{COMV} is generally in the min range.

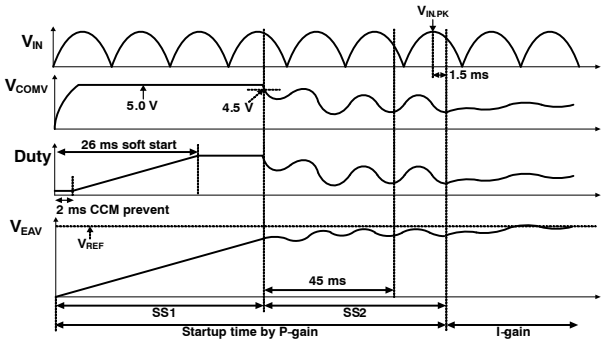


Figure 17. Start up sequnce

Dynamic CV Regulation

Due to the narrow loop bandwidth, PFC controller generally does not guarantee good CV regulation at load transient. Especially in secondary side regulation, primary side controller does not know the output voltage level and it only monitors the output of feedback signal through opto−coupler. Therefore, output voltage undershoot is severely happened at no to full load transient in the conventional SSR PFC control.

In order to overcome this, FL7740 utilizes the benefit of PSR with **onsemi**'s proprietary dynamic duty control by monitoring the output voltage. For example, when V_{EAV} is less than $V_{UVD.EN}$ (Under Voltage Dynamic Enable threshold), duty is quickly increased not to allow undershoot anymore. Once V_{EAV} rises higher than $V_{UVD.DIS}$ (Under Voltage Dynamic Disable threshold), duty quickly drops and follows COMV voltage. During the V_{EAV} hiccup operation, COMV voltage slowly increases and dynamic operation is terminated when COMV voltage is close to steady state level.

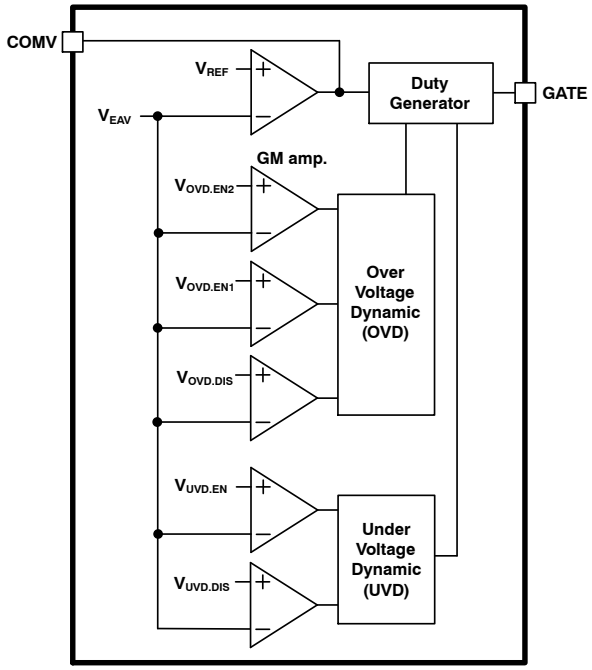


Figure 18. Dynamic Function Block

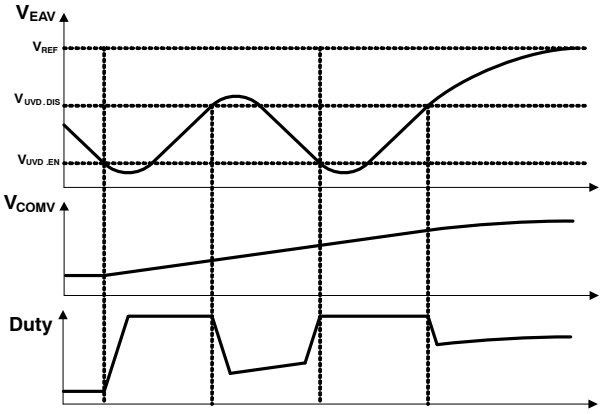


Figure 19. No to Full Load Transient

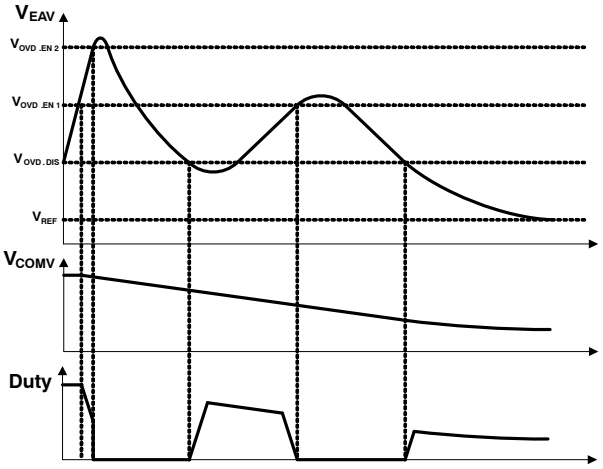


Figure 20. Full to No Load Transient

In case of OVD (Over Voltage Dynamic) function, it has two enable levels ($V_{OVD.EN1}$ and $V_{OVD.EN2}$). If output voltage overshoot at load transient is too high, VEAV increases to $V_{OVD.EN2}$ passing by $V_{OVD.EN1}$. Duty quickly drops when reaching $V_{OVD.EN1}$ and drops to min. level at once not to allow severe output over voltage when V_{EAV} increases higher than $V_{OVD.EN2}$.

FL7740 provides two sets of dynamic triggering threshold. When user prefers narrow output voltage variation at load transient with large output capacitor, SET0 can be selected without capacitor at PF pin. If wider output voltage variation is allowed and output capacitor should be small due to system size, SET1 can be selected with connection of capacitor around 0.5 nF at PF pin. FL7740 detects capacitance at PF pin at the beginning of switching startup and maintains the SET# until UVLO is triggered. During the 1st switching, PF pin is pulled down to 0 V. In the 2nd switching, PF pull down is disabled and PF voltage is monitored 5 μs after 2nd switching period begins. If the PF voltage is higher than 0.8 V $V_{DYN-REF-SET}$, SET0 is decided. If not, SET1 is determined.

Table 1. DYNAMIC THRESHOLD AT SET0 AND SET1

	$V_{VS.OVP}$	$V_{OVD.EN2}$	$V_{OVD.EN1}$	$V_{OVD.DIS}$	$V_{UVD.DIS}$	$V_{UVD.EN}$
$V_{OV-REF5}$ + 20% V_{REF}	SET1					
$V_{OV-REF4}$ + 15% V_{REF}	SET0	SET1				
$V_{OV-REF3}$ + 10% V_{REF}		SET0	SET1			
$V_{OV-REF2}$ + 5.7% V_{REF}			SET0	SET1		
$V_{OV-REF1}$ + 2.9% V_{REF}				SET0		
$V_{UV-REF1}$ − 2.9% V_{REF}					SET0	
$V_{UV-REF2}$ − 5.7% V_{REF}					SET1	SET0
$V_{UV-REF3}$ − 10% V_{REF}						SET1

Digital PF Optimizer

As line voltage increases and output load decreases, PF is degraded due to the effect of EMI filter capacitor charging/discharging current. Input current is the sum of EMI Filter capacitor current and flyback input current. Whether the flyback input current is exactly in−phase sinusoidal current with line voltage, 90° phase shifted EMI filter cap current worsens displacement factor of the overall system input current.

The **onsemi**'s proprietary PF optimizer accurately compensates the EMI filter capacitor current and improves PF more than 0.1 at high line and half load condition.

The calculation coefficient in the PF optimizer is externally programmable by supplying a certain level of voltage at PF pin with external resistive divider from 5 V BIAS pin. Before 1st switching, FL7740 converts the PF voltage into digital value without switching noise and keeps the digital value for the coefficient until UVLO is triggered.

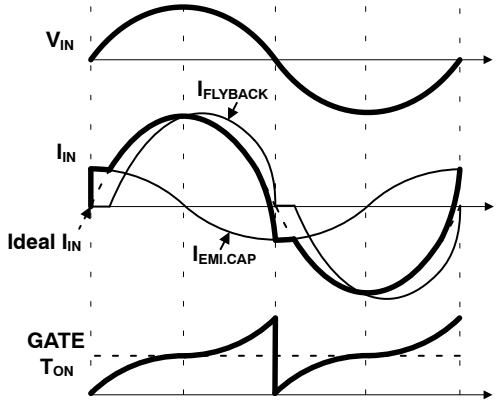


Figure 21. With PF Optimizer

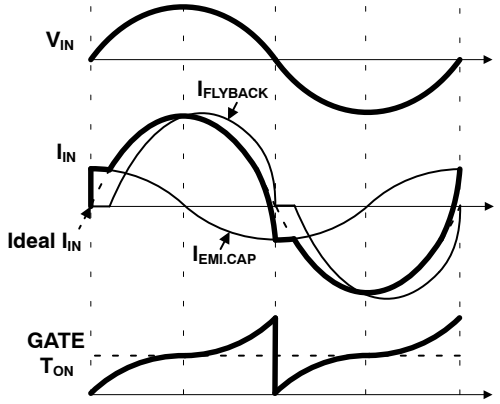


Figure 22. With PF Optimizer

Recommended V_{PF} is in Equation 1, where L_M is magnetizing inductance and C_{EMI} is total EMI filter capacitance.

$$V_{PF} = 5 \times 10^9 \times L_M \times C_{EMI} + 1.5 \qquad \text{(eq. 1)}$$

As V_{PF} increases, the coefficient in the PF optimizer calculation is larger with better PF, but THD is worse due to the input current distortion at input voltage zero cross. Therefore, V_{PF} adjustment by changing PF resistors is recommended to bring the best PF and THD performance to meet user's target. When V_{PF} is lower than 1.5 V, PF optimizer is disabled.

Protection

- Auto−restart:
  Once protection is triggered, FL7740 terminates switching and internal 3 sec counter makes delay time. In 3 sec, VDD voltage is regulated between 17 V and 19 V by internal HV biasing not to fall in UVLO. After 3 sec, VDD falls down to 7.75 V V_{DD-OFF} and IC is reset with released protection. When VDD voltage is up again to 16 V V_{DD-ON}, FL7740 begins startup sequence.

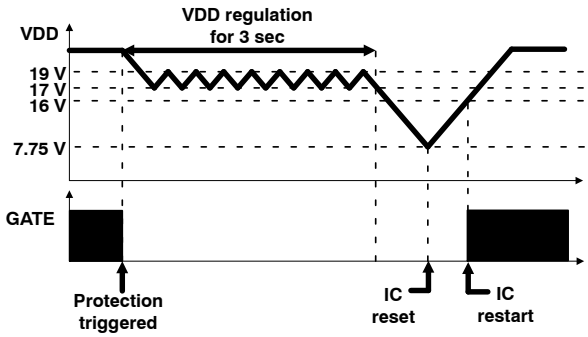


Figure 23. Auto Restart

- Output Over Voltage Protection:
  Output over voltage is hardly triggered due to the powering limit by dynamic function. But, in the abnormal condition, output OVP is triggered when V_{EAV} is higher than 4.0 V @ SET0 / 4.2 V @ SET1 for 4 switching cycles or VDD voltage is higher than 25 V for 10 μs delay.
- Output Short Protection:
  At output short condition, V_{EAV} is less than 0.7 V. If this condition lasts for continuous 35 ms switching time, OSP is triggered.
- Over Current Protection:
  When CS voltage is higher than 1.8 V over the 1.2 V pulse−by−pulse current limit, protection is immediately triggered. OCP protects output diode short, sensing resistor open and transformer saturation condition.
- Sensing Resistor Short Protection:
  1st switching is 0.2 V current mode. If CS doesn't reach over 75 mV threshold during 1st turn−on time, SRSP is triggered. Max. turn−on time at 1st switching is inversely proportional to input voltage to limit the primary peak current.
- Over Load Protection:
  At over load condition, CS reaches to 1.2 V pulse−by−pulse current limit. FL7740 generates internal ZC (Zero

Cross) signal and OLP is triggered if the event (1.2 V current limit event between the two close ZC signals) is occurred for consecutive 60 ZC signals.

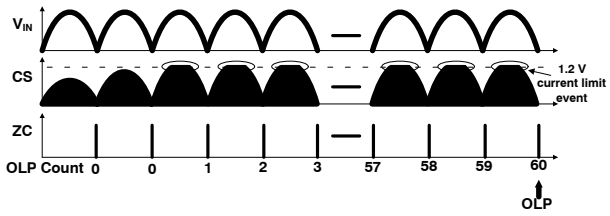
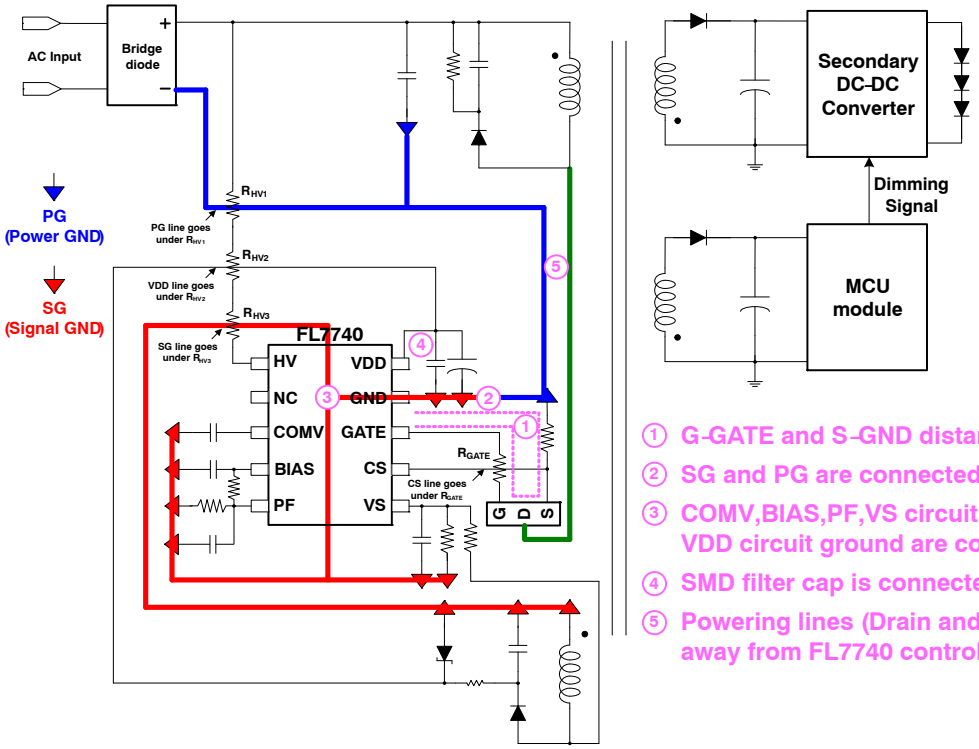


Figure 24. Over Load Protection

- Thermal Shut Down:
  When internal junction temperature is higher than 150°C, TSD is triggered and protection is released when the junction temperature drops under 120°C.



① G-GATE and S-GND distance should be short.
② SG and PG are connected close at GND pin.
③ COMV,BIAS,PF,VS circuit ground and aux. winding VDD circuit ground are connected close at GND pin
④ SMD filter cap is connected close at VDD and GND pin.
⑤ Powering lines (Drain and PG) are closely placed and away from FL7740 control circuits

Figure 25. Single Layer PCB Layout Guidance

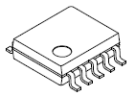
ORDERING INFORMATION

Product Number	Package	Shipping†
FL7740MX	10 Lead SOIC, JDEC MS−012, 150” Narrow Body (Pb−Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

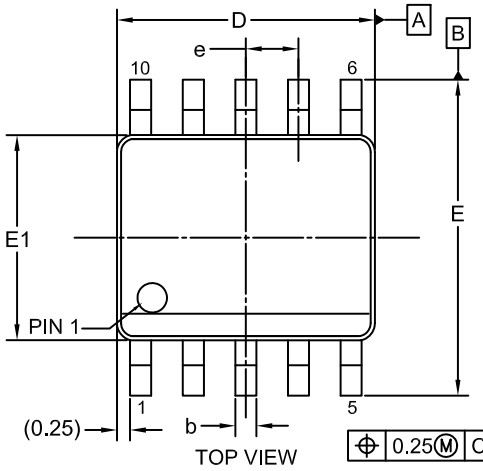
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

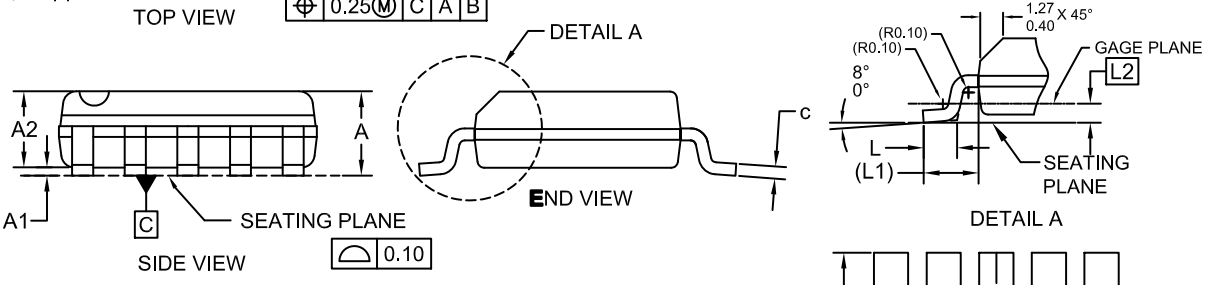


SOIC10, 4.9x6.0, 1.0P
CASE 751EE
ISSUE A

DATE 28 MAY 2019



DIM	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.50
b	0.30	0.40	0.45
c	0.10	0.20	0.25
D	4.80	4.90	5.00
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.00 BSC		
L	0.40	0.65	1.27
L1	1.04 Reference only		
L2	0.36 BSC		

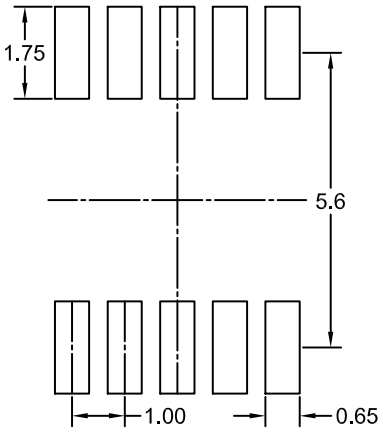


NOTES:
A. THIS PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MS-012.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
E. LAND PATTERN STANDARD : SOIC127P600X175.10M

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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