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FSA3341 — High-Speed 4:1 USB2.0 / MHL™ Switch

Features

- Low On Capacitance: 4.2 pF / 5 pF MHL / USB (Typical)
- Low Power Consumption: 30 μ A Maximum
- Supports MHL Rev. 2.0
- Three USB2.0 Paths
- MHL Data Rate: 4.0 Gbps
- Packaged in 16-Lead UMLP (1.8 x 2.6 mm)
- Over-Voltage Tolerance on All USB Ports: Up to 5.25 V without External Components

Applications

- Cell Phones and Digital Cameras

Description

The FSA3341 is a bi-directional, low-power, high-speed, 4:1, USB2.0 and MHL™ switch. Configured as a Double-Pole, Four-Throw (DP4T) switch; it is optimized for switching between high- or full-speed USB and Mobile High-Definition Link sources (MHL Rev. 2.0 specification). In addition, the USB2.0 paths can be used as UART paths.

The FSA3341 contains circuitry on the switch I/O pins that allows the device to withstand an over-voltage condition for applications where the V_{CC} supply is powered off ($V_{CC} = 0V$). This switch is designed to minimize current consumption even when the control voltage applied to the control pins is lower than the supply voltage (V_{CC}). This is especially valuable in mobile applications, such as cell phones, allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switch sharing in portable cell phones, digital cameras, and notebook computers.

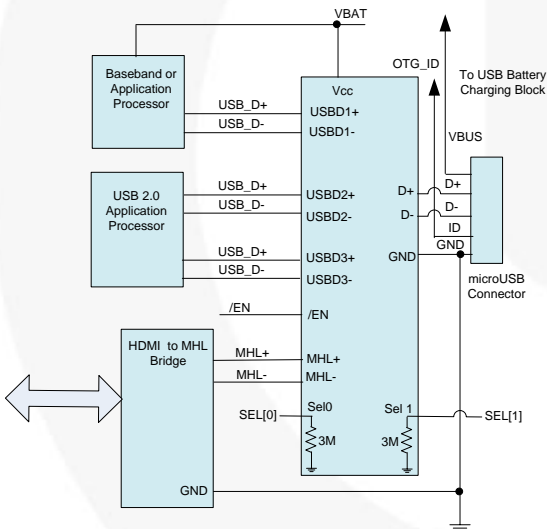


Figure 1. Typical Application

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3341UMX	LY	-40 to +85°C	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm

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Pin Configuration

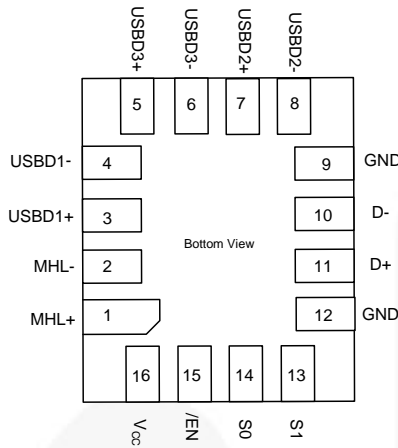


Figure 2. Pin Assignments

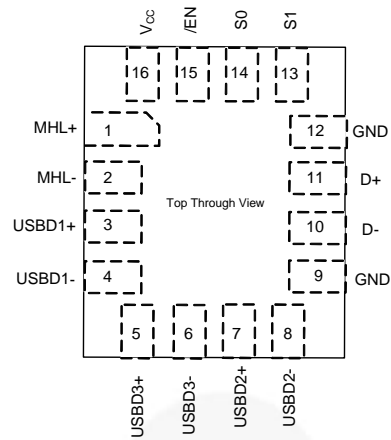


Figure 3. Top Through View

Pin Definitions

Pin#	Name	Description
1	MHL+	MHL Differential Data (Positive)
2	MHL-	MHL Differential Data (Negative)
3	USB1+	USB Differential Data (Positive); also can be used as additional UART
4	USB1-	USB Differential Data (Negative); also can be used as additional UART
5	USB3+	USB Differential Data (Positive); also can be used as additional UART
6	USB3-	USB Differential Data (Negative); also can be used as additional UART
7	USB2+	USB Differential Data (Positive); can be used as a UART port (see Figure 1)
8	USB2-	USB Differential Data (Negative); can be used as a UART port (see Figure 1)
9	GND	Ground
10	D-	USB Differential Data (Negative), Common Port
11	D+	USB Differential Data (Positive), Common Port
12	GND	Ground
13	S1	Data Switch Select (see Table 1)
14	S0	Data Switch Select (see Table 1)
15	/EN	Enable Pin - Active LOW
16	V _{CC}	Device Power from System (Typically V _{BAT})

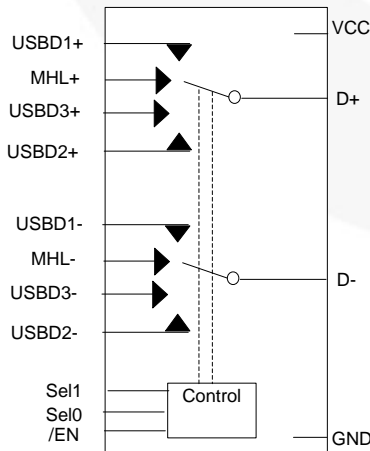


Figure 4. Analog Symbol

Table 1. Data Switch Select Truth Table

SEL1 ⁽¹⁾	SEL0 ⁽¹⁾	/EN ⁽¹⁾	Function
0	0	0	D+/D- connected to USB1+/USB1- (or UART) path
0	1	0	D+/D- connected to USB2+/USB2- (or UART) path
1	0	0	D+/D- connected to MHL+/MHL- path
1	1	0	D+/D- connected to USB3+/USB3- (or UART) path
X	X	1	D+/D- high impedance

Note:

- Control inputs should never be left floating or unconnected. To guarantee default switch closure to the USB position, the SEL[0:1] pins are tied to GND with internal weak pull-down resistors (3 MΩ) to minimize static current draw.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.5	5.5	V
V _{CNTRL}	DC Input Voltage (/EN, SEL[1:0]) ⁽²⁾	-0.5	V _{CC}	V
V _{SW} ⁽³⁾	DC Switch I/O Voltage ⁽²⁾			
	USB, MHL	-0.5	V _{CC}	V
I _{IK}	DC Input Diode Current	-50		mA
I _{OUT}	Switch DC Output Current (Continuous)		60	mA
	USB, MHL			
I _{OUTPEAK}	Switch DC Output Peak Current (Pulsed at 1 ms Duration, <10% Duty Cycle)		150	mA
	USB, MHL			
T _{STG}	Storage Temperature	-65	+150	°C
MSL	Moisture Sensitivity Level: JEDEC J-STD-020A		1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	4	kV
	IEC 61000-4-2, Level 4, for D+/D- and V _{CC} Pins ⁽⁴⁾	Contact	8	
	IEC 61000-4-2, Level 4, for D+/D- and V _{CC} Pins ⁽⁴⁾	Air	15	
	Charged Device Model, JESD22-C101		2	

Notes:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
- V_{SW} refers to analog data switch paths (USB, MHL, and audio).
- Testing performed in a system environment using TVS diodes.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	2.5	4.5	V
t _{RAMP(VCC)}	Power Supply Slew Rate	100	1000	µs/V
V _{CNTRL}	Control Input Voltage (/EN, SEL[1:0]) ⁽⁵⁾	0	4.5	V
V _{SW(USB)}	Switch I/O Voltage (USB Switch Path)	-0.5	3.6	V
Θ _{JA}	Thermal Resistance		273	C°/W
V _{SW(MHL)}	Switch I/O Voltage (MHL Switch Path)	1.65	3.45	V
T _A	Operating Temperature	-40	+85	°C

Note:

- The control inputs must be held HIGH or LOW; they must not float.

DC Electrical Characteristics

All typical values are at $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	V _{CC} (V)	T _A =-40°C to +85°C			Unit
				Min.	Typ.	Max.	
V _{IK}	Clamp Diode Voltage	I _{IN} =-18 mA	2.5			-1.2	V
V _{IH}	Control Input Voltage HIGH	SEL[1:0]	2.5	1.3			V
			3.6	1.4			V
			4.5	1.5			V
V _{IL}	Control Input Voltage LOW	SEL[1:0]	2.5			0.4	V
			3.6			0.4	V
			4.5			0.4	V
I _{IN}	Control Input Leakage SEL[1:0]	V _{SW} (MHL & USB)=0 to 3.6 V, V _{CNTRL} =0 to V _{CC}	4.5	-2.5		2.5	μA
I _{OZ(MHL)}	Off-State Leakage for Open MHL Data Paths	V _{SW} =1.65 ≤ MHL ≤ 3.45 V, /EN=V _{CC} , Figure 6	4.5	-0.5		0.5	μA
I _{OZ(USB)}	Off-State Leakage for Open USB Data Paths	V _{SW} =0 ≤ USB ≤ 3.6 V, /EN=V _{CC} , Figure 6	4.5	-0.5		0.5	μA
I _{CL(MHL)}	On-State Leakage for Closed MHL Data Paths ⁽⁶⁾	V _{SW} =1.65 ≤ MHL ≤ 3.45 V, /EN=GND, SEL0=GND, SEL1=V _{CC}	4.5	-0.5		0.5	μA
I _{CL(USB)}	On-State Leakage for Closed USB Data Paths ⁽⁶⁾	V _{SW} =0 ≤ USB ≤ 3.6 V, /EN=GND, SEL[1:0]=GND and SEL1=GND, SEL0=V _{CC}	4.5	-0.5		0.5	μA
I _{OFF}	Power-Off Leakage Current (USB & MHL Paths)	V _{SW} =0 V or 3.6 V, Figure 6	0	-0.5		0.5	μA
R _{ON(USB)}	HS Switch On Resistance (USB _{Dn} to D _n Path)	V _{SW} =0.4 V, I _{ON} =-8 mA, SEL[1:0]=GND, and SEL1=GND, SEL0=V _{CC} Figure 5	2.5 to 4.5		8		Ω
R _{ON(MHL)}	HS Switch On Resistance (MHL to D Path)	V _{SW} =V _{CC} -1050 mV, SEL0=GND, SEL1=V _{CC} , I _{ON} =-8 mA, Figure 5	2.5 to 4.5		5		Ω
ΔR _{ON(MHL)}	Difference in R _{ON} Between MHL Positive-Negative	V _{SW} =V _{CC} -1050 mV, SEL0=GND, SEL1=V _{CC} , I _{ON} =-8 mA, Figure 5,	2.5 to 4.5		0.03		Ω
ΔR _{ON(USB)}	Difference in R _{ON} Between USB Positive-Negative	V _{SW} =0.4V, I _{ON} =-8 mA, SEL[1:0]=GND and SEL1=GND, SEL0=V _{CC} , Figure 5	2.5 to 4.5		0.18		Ω
R _{ONF(MHL)}	Flatness for R _{ON} MHL Path	V _{SW} =1.65 V to 3.45 V, SEL0=GND, SEL1=V _{CC} , I _{ON} =-8 mA, Figure 5	2.5 to 4.5		1		Ω
R _{ONFD(USB)}	Flatness for R _{ON} USB Path	V _{SW} =0 V to 3.6 V, SEL[1:0]=GND and SEL1=GND, SEL0=V _{CC} , I _{ON} =-8 mA, Figure 5	2.5 to 4.5		2.1		Ω
R _{PD}	Internal Pull -Down Resistors on SEL0 & SEL1		2.5 to 4.5		3		MΩ
I _{CC}	Quiescent Current	V _{CNTRL} =0 or 4.5 V, I _{OUT} =0	4.5			30	μA
I _{CCZ}	Quiescent Current-High Impedance	V _{/EN} =4.5 V, I _{OUT} =0	4.5			1	μA
I _{CCCT}	Delta Increase in Quiescent Current per Control Pin	V _{CNTRL} =1.65 V, I _{OUT} =0	4.5			10	μA
		V _{CNTRL} =2.5 V, I _{OUT} =0	4.5			5	

Note:

6. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical values are for $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	V _{CC} (V)	T _A =-40°C to +85°C			Unit
				Min.	Typ.	Max.	
t _{ONUSB}	USB Turn-On Time, SEL[1:0] to Output	R _L =50 Ω, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	700	ns
t _{OFFUSB}	USB Turn-Off Time, SEL[1:0] to Output	R _L =50 Ω, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t _{ONMHL}	MHL Turn-On Time, SEL[1:0] to Output	R _L =50 Ω to 3.3 V, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t _{OFFMHL}	MHL Turn-Off Time, SEL[1:0] to Output	R _L =50 Ω to 3.3 V, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		445	600	ns
t _{ENABLE}	Enable Turn-On Time, /EN to Output	R _L =50 Ω, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		80		μs
t _{DISABLE}	Disable Turn-Off Time, /EN to Output	R _L =50 Ω, C _L =5 pF, V _{SW(USB)} =0.8 V, V _{SW(MHL)} =3.3 V, Figure 7, Figure 8	2.5 to 4.5		35		ns
t _{PD}	Propagation Delay ⁽⁷⁾	C _L =5 pF, R _L =50 Ω, Figure 7, Figure 9	2.5 to 4.5		0.25		ns
t _{BMM}	Break-Before-Make ⁽⁷⁾	R _L =50 Ω, C _L =50 pF, V _{MHL} =3.3 V, V _{USB} =0.8 V, Figure 11	2.5 to 4.5	50	120	600	ns
O _{IRR(MHL)}	Off Isolation ⁽⁷⁾	V _S =1 V _{pk-pk} , R _L =50 Ω, f=24 MHz, Figure 13	2.5 to 4.5		-36		dB
O _{IRR(USB)}		V _S =400 mV _{pk-pk} , R _L =50 Ω, f=240 MHz, Figure 13	2.5 to 4.5		-38		dB
O _{IRR(UART)}		V _S =40 mV _{pk-pk} , R _L =50 Ω, f=10 MHz, Figure 13	2.5 to 4.5		-40		dB
Xtalk _{MHL}	Non-Adjacent Channel Crosstalk ⁽⁷⁾	V _S =1 V _{pk-pk} , R _L =50 Ω, f=240 MHz, Figure 14	2.5 to 4.5		-44		dB
Xtalk _{USB}		V _S =400 mV _{pk-pk} , R _L =50 Ω, f=240 MHz, Figure 14	2.5 to 4.5		-36		dB
Xtalk _{UART}		V _S =400 mV _{pk-pk} , R _L =50 Ω, f=10 MHz, Figure 14	2.5 to 4.5		-36		dB
THD	Total Harmonic Distortion - LINOUT ⁽⁷⁾	R _T =600 Ω, V _{SW} =2 V _{pk-pk} , f=20 Hz to 20 kHz, V _{BIAS} =0 V	2.5 to 4.5		0.01		%
BW	S _{DD21} Differential -3db Bandwidth ⁽⁷⁾	V _{IN} =1 V _{pk-pk} , Common Mode Voltage=V _{CC} - 1.1 V, MHL Path, R _L =50 Ω, C _L =0 pF, Figure 12	2.5 to 4.5		2.0		GHz
		V _{IN} =400 mV _{pk-pk} , Common Mode Voltage=0.2 V, USB Path, R _L =50 Ω, C _L =0 pF, Figure 12			650 ⁽⁸⁾		MHz

Note:

7. Guaranteed by characterization.
8. 650 MHz USB Bandwidth, passed USB2.0-Compliant testing.

USB High-Speed AC Electrical Characteristics

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.0$ to 3.6 V.

Symbol	Parameter	Condition	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output ⁽⁹⁾	$C_L=5$ pF, $R_L=50$ Ω , Figure 10	3	ps
t_J	Total Jitter ⁽⁹⁾	$R_L=50$ Ω , $C_L=5$ pF, $t_R=t_F=500$ ps (10-90%) at 480 Mbps, PN7	20	ps

Note:

9. Guaranteed by characterization.

MHL™ AC Electrical Characteristics

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{CC}=3.0$ to 3.6 V.

Symbol	Parameter	Condition	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output ⁽¹⁰⁾	$R_{PU}=50$ Ω to V_{CC} , $C_L=0$ pF	2	ps
t_J	Total Jitter ⁽¹⁰⁾	$f=2.25$ Gbps, PN7, $R_{PU}=50$ Ω to V_{CC} , $C_L=0$ pF	15	ps

Note:

10. Guaranteed by characterization.

Capacitance

Typical values are at $T_A = 25^{\circ}\text{C}$.

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Control Pin Input Capacitance ⁽¹¹⁾	$V_{CC}=0\text{V}$, $f=1$ MHz	2.5	pF
$C_{ON(USB)}$	USB Path On Capacitance ⁽¹¹⁾	$V_{CC}=3.3$ V, $f=240$ MHz, Figure 16	5.0	
$C_{OFF(USB)}$	USB Path Off Capacitance ⁽¹¹⁾	$V_{CC}=3.3$ V, $f=240$ MHz, Figure 15	2.5	
$C_{ON(MHL)}$	MHL Path On Capacitance ⁽¹¹⁾	$V_{CC}=3.3$ V, $f=240$ MHz, Figure 16	4.2	
$C_{OFF(MHL)}$	MHL Path Off Capacitance ⁽¹¹⁾	$V_{CC}=3.3$ V, $f=240$ MHz, Figure 15	2.5	

Note:

11. Guaranteed by characterization.

Test Diagrams

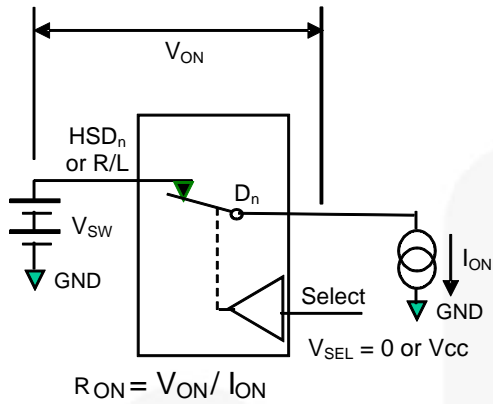
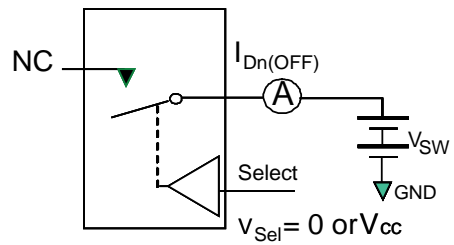


Figure 5. On Resistance



**Each switch port is tested separately

Figure 6. Off Leakage

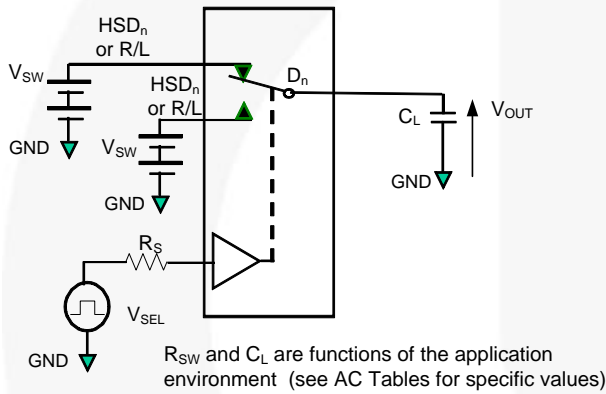


Figure 7. AC Test Circuit Load

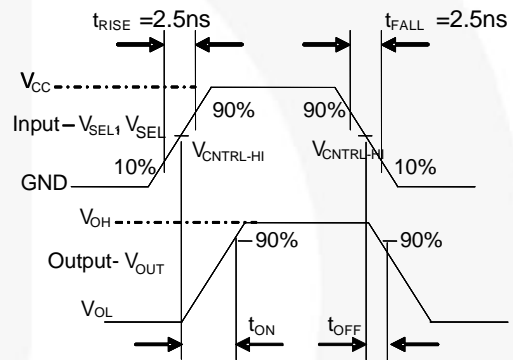


Figure 8. Turn-On / Turn-Off Waveforms

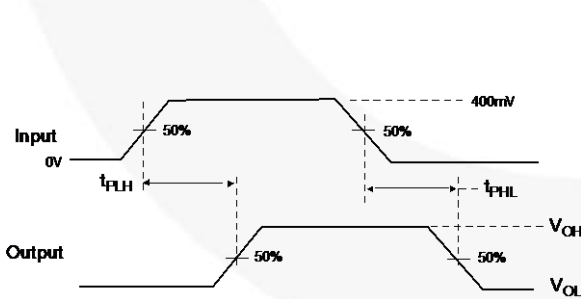


Figure 9. Propagation Delay ($t_{rF} = 500$ ps)

Note:

12. HSD_n refers to the high-speed data USB or MHL paths.

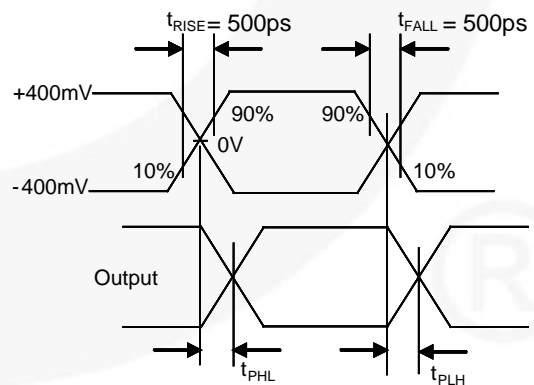


Figure 10. Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams (Continued)

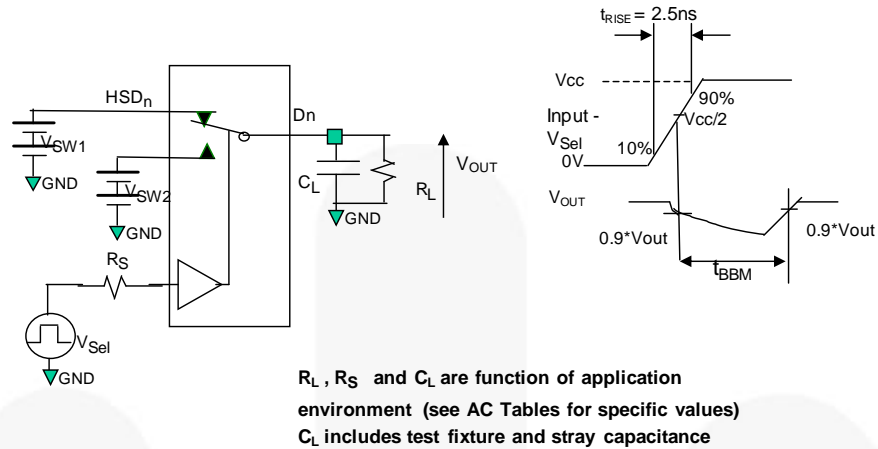


Figure 11. Break-Before-Make Interval Timing

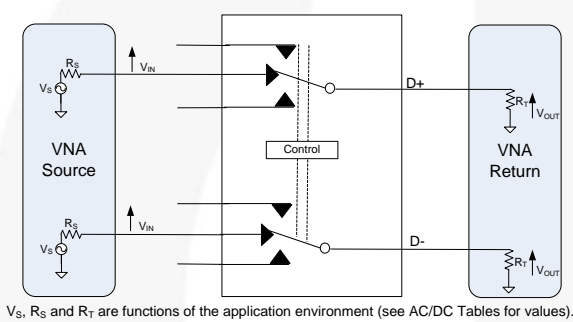


Figure 12. Insertion Loss (SDD21)

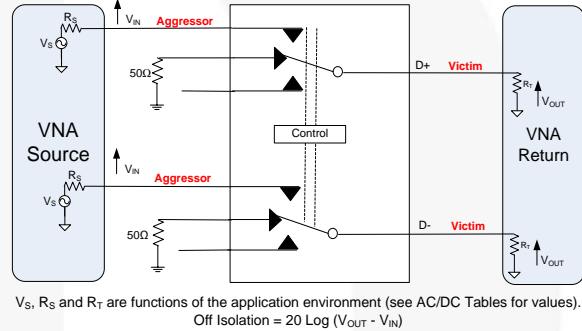


Figure 13. Channel Off Isolation (SDD21)

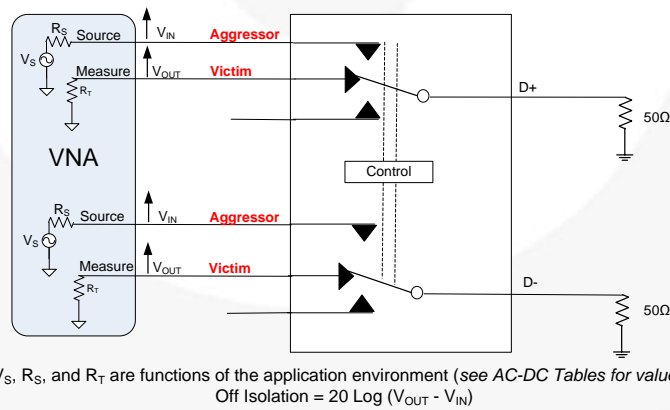


Figure 14. Non-Adjacent Channel-to-Channel Crosstalk (SDD21)

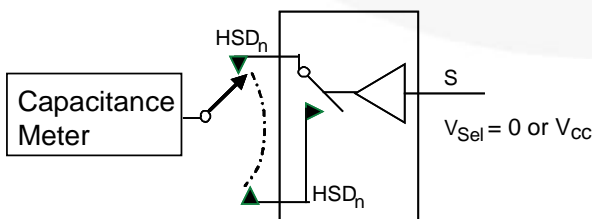


Figure 15. Channel Off Capacitance

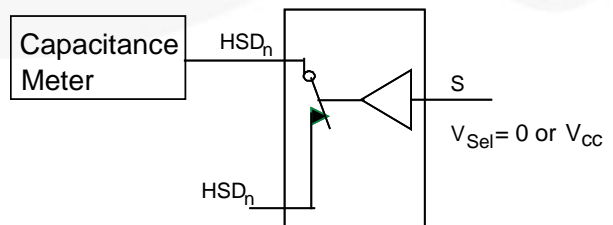


Figure 16. Channel On Capacitance

Functional Description

Insertion Loss

One of the key advantages of using the FSA3341 in mobile digital-video applications is the small amount of insertion loss experienced by the received signal as it passes through the switch. This results in minimal degradation to the received eye. One of the ways to measure the quality of the high-data-rate channels is using balanced ports and four-port differential S-parameter analysis, particularly SDD21.

Bandwidth is measured using the S-parameter SDD21 methodology.

Typical Applications

Figure 19 shows the FSA3341 utilizing the V_{BAT} connection. The 3 MΩ resistors are used to ensure, for manufacturing test via the micro-USB connector, that the FSA3341 configures for connectivity to the baseband or application processor.

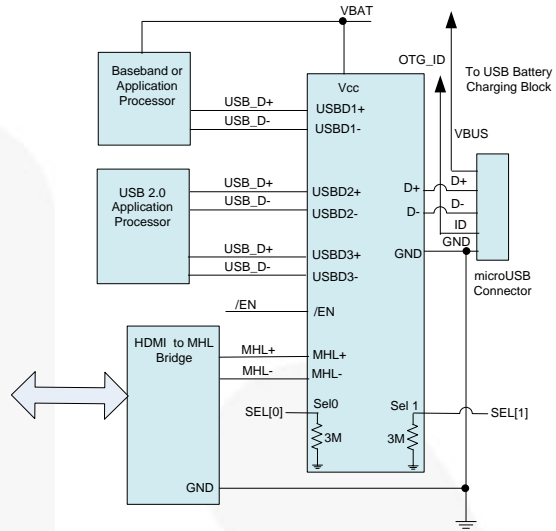


Figure 19. Typical Application



Figure 17. MHL Path SDD21 Insertion Loss Curve

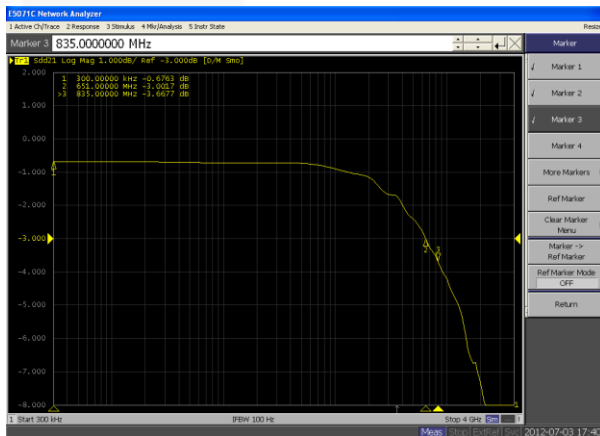
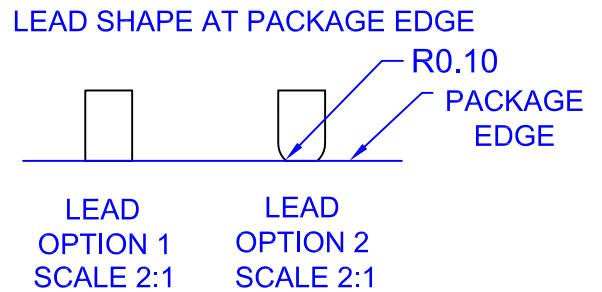
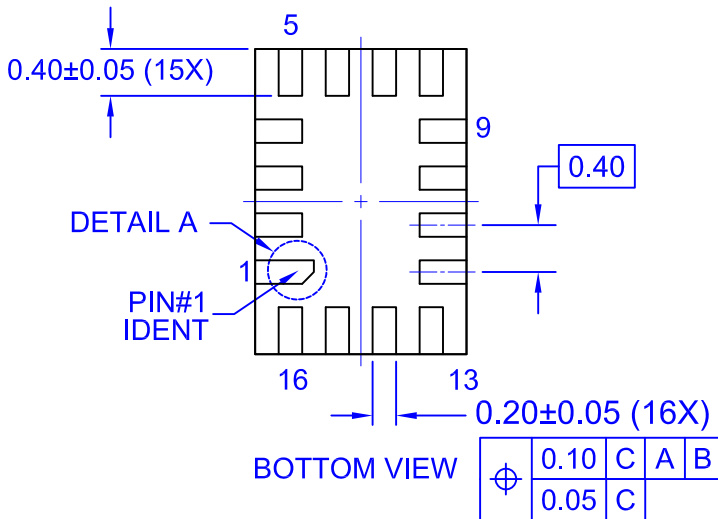
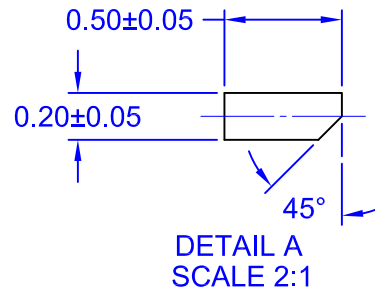
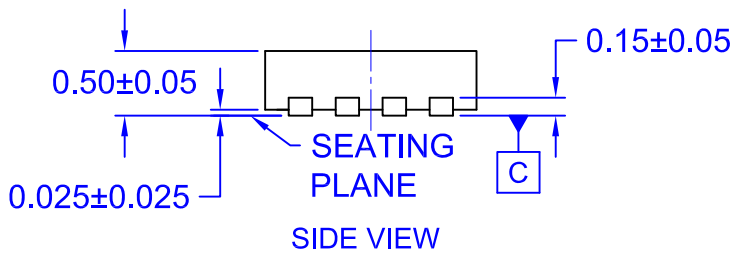
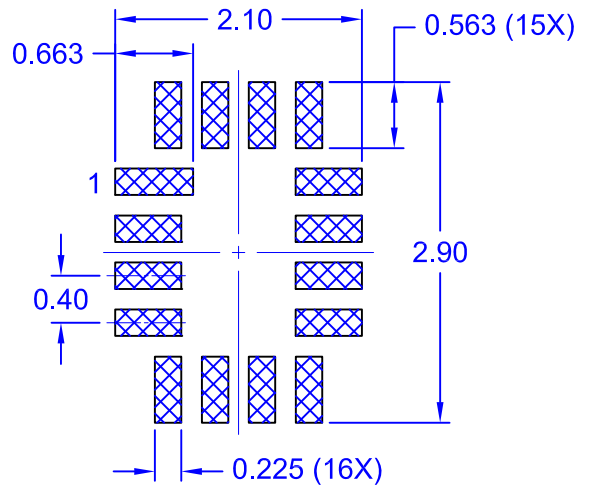
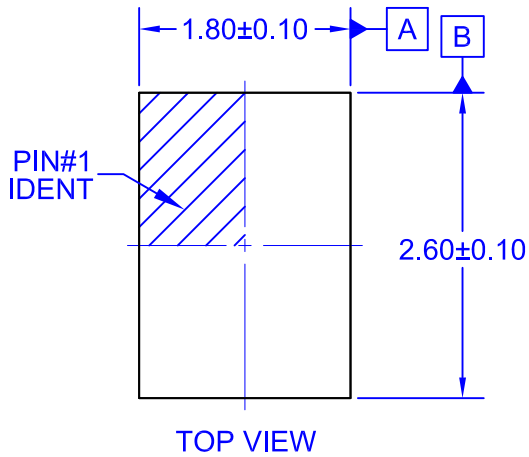


Figure 18. USB Path SDD21 Insertion Loss Curve



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- D. DRAWING FILENAME: MKT-UMLP16ArevG.
- E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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