

Octal D Flip-Flop with Clock Enable

MC74AC377, MC74ACT377

The MC74AC377/74ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

- Ideal for Addressable Register Applications
- Clock Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Outputs Source/Sink 24 mA
- See MC74AC273 for Master Reset Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- ACT377 Has TTL Compatible Inputs
- MSL = 1 for all Surface Mount
- Chip Complexity: 292 FETs or 73 Gates
- These are Pb-Free Devices

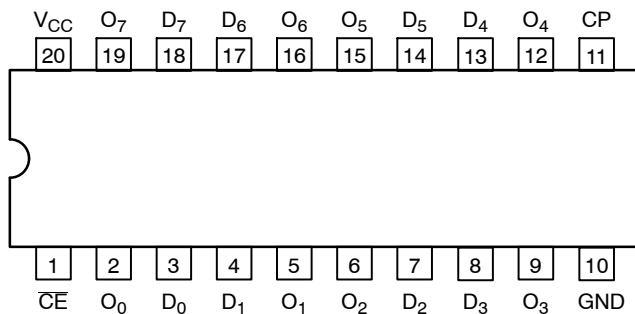
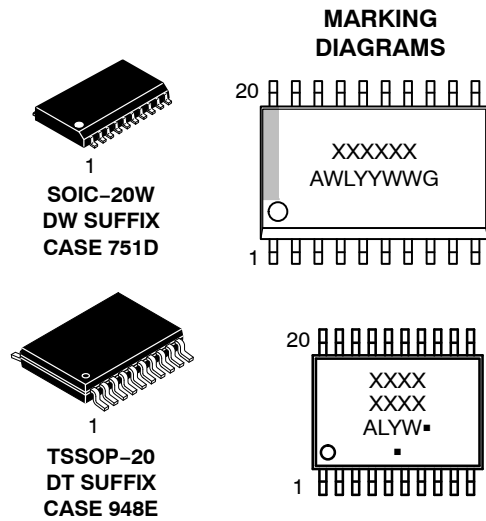


Figure 1. Pinout: 20-Lead Packages Conductors
(Top View)

PIN NAMES

PIN	FUNCTION
D ₀ –D ₇	Data Inputs
\overline{CE}	Clock Enable (Active LOW)
Q ₀ –Q ₇	Data Outputs
CP	Clock Pulse Input



XXXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

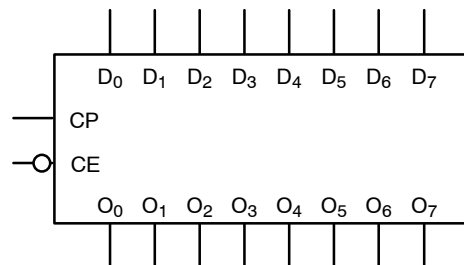


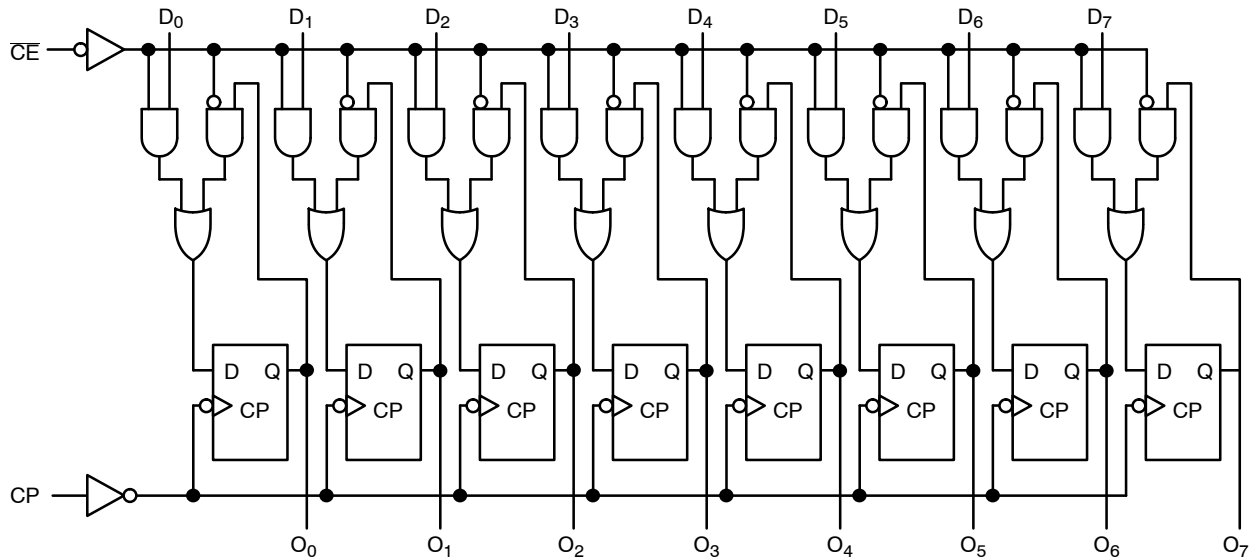
Figure 2. Logic Symbol

MC74AC377, MC74ACT377

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	CE	D _n	Q _n
Load '1'	⌋	L	H	H
Load '0'	⌋	L	L	L
Hold (Do Nothing)	⌋	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌋ = LOW-to-HIGH Clock Transition



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MC74AC377, MC74ACT377

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +6.5	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND) (Note 1)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_{OUT}	DC Output Sink/Source Current	± 50	mA
I_{CC}	DC Supply Current, per Output Pin	± 50	mA
I_{GND}	DC Ground Current, per Output Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	140	°C
θ_{JA}	Thermal Resistance (Note 2) SOIC TSSOP	96 150	°C/W
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Charged Device Model (Note 4)	> 2000 > 1000	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 85°C (Note 5)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_{OUT} absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. Tested to EIA/JESD22-A114-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 6) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0\text{ V}$	–	150	ns/V
		$V_{CC} @ 4.5\text{ V}$	–	40	
		$V_{CC} @ 5.5\text{ V}$	–	25	
t_r, t_f	Input Rise and Fall Time (Note 7) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5\text{ V}$	–	10	ns/V
		$V_{CC} @ 5.5\text{ V}$	–	8.0	
T_A	Operating Ambient Temperature Range	-40	25	85	°C
I_{OH}	Output Current – High	–	–	-24	mA
I_{OL}	Output Current – Low	–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. V_{in} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
7. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC377, MC74ACT377

74AC – DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.50 2.25 2.75	2.10 3.15 3.85	2.10 3.15 3.85	V V V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.50 2.25 2.75	0.90 1.35 1.65	0.90 1.35 1.65	V V V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V V V	I _{OUT} = –50 μA
		3.0 4.5 5.5	– – –	2.56 3.86 4.86	2.46 3.76 4.76	V V V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
V _{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V V V	I _{OUT} = 50 μA
		3.0 4.5 5.5	– – –	0.36 0.36 0.36	0.44 0.44 0.44	V V V	*V _{IN} = V _{IL} or V _{IH} –12 mA I _{OH} –24 mA –24 mA
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OLD} I _{OHD}	Maximum Input Leakage Current	5.5 5.5	– –	– –	75 –75	mA mA	V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

74AC – AC CHARACTERISTICS For Figures and Waveforms, See Figures 4, 5, and 6.

Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF			T _A = –40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	3.3 5.0	90 140	–	–	75 125	–	MHz
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	3.0 2.0	–	13.0 9.0	1.5 1.5	14.0 10.0	ns
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	3.5 2.5	–	13.0 10.0	2.0 1.5	14.5 11.0	ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V; Voltage Range 5.0 V is 5.0 V ±0.5 V.

74AC – AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF		T _A = –40°C to +85°C	Unit
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	–	5.5 4.07	6.0 4.5	ns
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	–	0 1.0	0 1.0	ns
t _s	Setup Time, HIGH or LOW CE to CP	3.3 5.0	–	6.0 4.0	7.5 4.5	ns
t _h	Hold Time, HIGH or LOW CE to CP	3.3 5.0	–	0 1.0	0 1.0	ns
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	–	5.5 4.0	6.0 4.5	ns

* Voltage Range 3.3 V is 3.3 V ±0.3 V; Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC377, MC74ACT377

74ACT – DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1 V or V _{CC} – 0.1 V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = –50 μA
		4.5 5.5	–	3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5	–	0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} –24 mA I _{OH} –24 mA
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max I _{CC} /Input	5.5	0.6	–	1.5	mA	V _I = V _{CC} – 2.1 V
I _{OLD} I _{OHD}	†Minimum Dynamic Output Current	5.5	–	–	75 –75	mA	V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

74ACT – AC CHARACTERISTICS For Figures and Waveforms — See Figures 4, 5, and 6.

Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF			T _A = –40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	140	–	–	125	–	MHz
t _{PLH}	Propagation Delay CP to Q _n	5.0	3.0	–	9.0	2.5	10	ns
t _{PHL}	Propagation Delay CP to Q _n	5.0	3.5	–	10	2.5	11	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

74ACT – AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	T _A = +25°C C _L = 50 pF		T _A = –40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	–	4.5	5.5	ns
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	–	1.0	1.0	ns
t _s	Setup Time, HIGH or LOW $\overline{\text{CE}}$ to CP	5.0	–	4.5	5.5	ns
t _h	Hold Time, HIGH or LOW $\overline{\text{CE}}$ to CP	5.0	–	1.0	1.0	ns
t _w	CP Pulse Width HIGH or LOW	5.0	–	4.0	4.5	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	90	pF	V _{CC} = 5.0 V

MC74AC377, MC74ACT377

SWITCHING WAVEFORMS

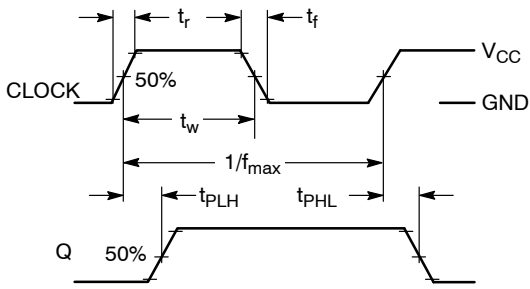


Figure 4.

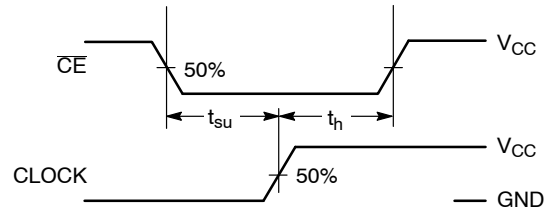


Figure 5.

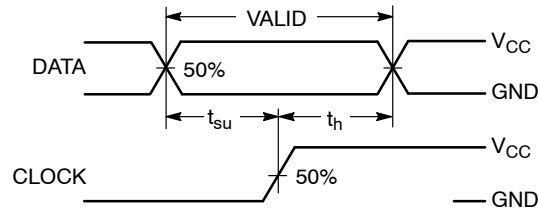
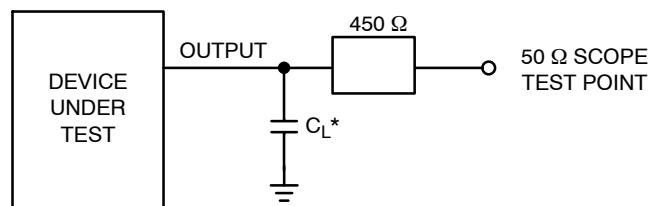


Figure 6.



*Includes all probe and jig capacitance

Figure 7. Test Circuit

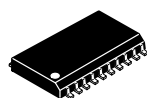
MC74AC377, MC74ACT377

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MC74AC377DWR2G	AC377	SOIC-20	1000 / Tape & Reel
MC74ACT377DWR2G	ACT377	SOIC-20	1000 / Tape & Reel
MC74AC377DTG	AC 377	TSSOP-20	75 Units / Rail
MC74AC377DTR2G	AC 377	TSSOP-20	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

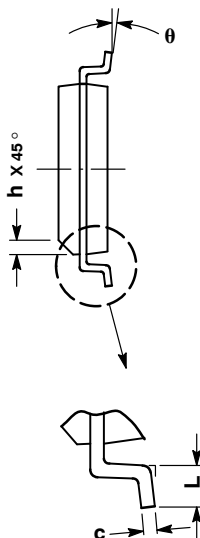
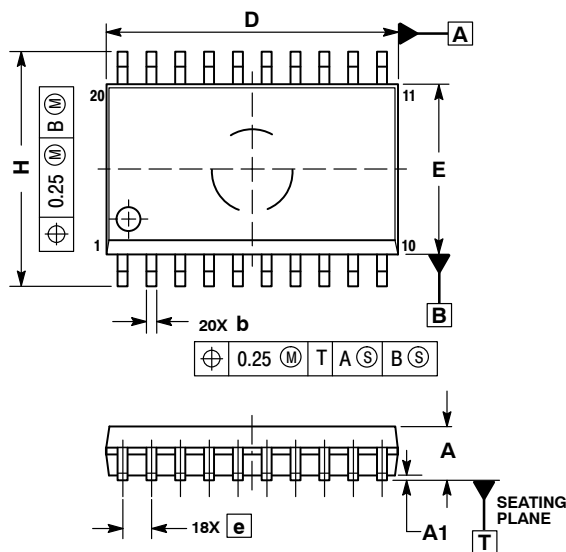
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

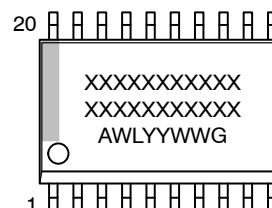


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

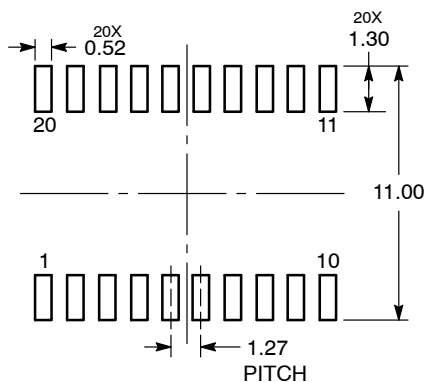
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

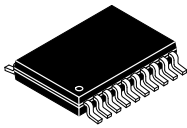
DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

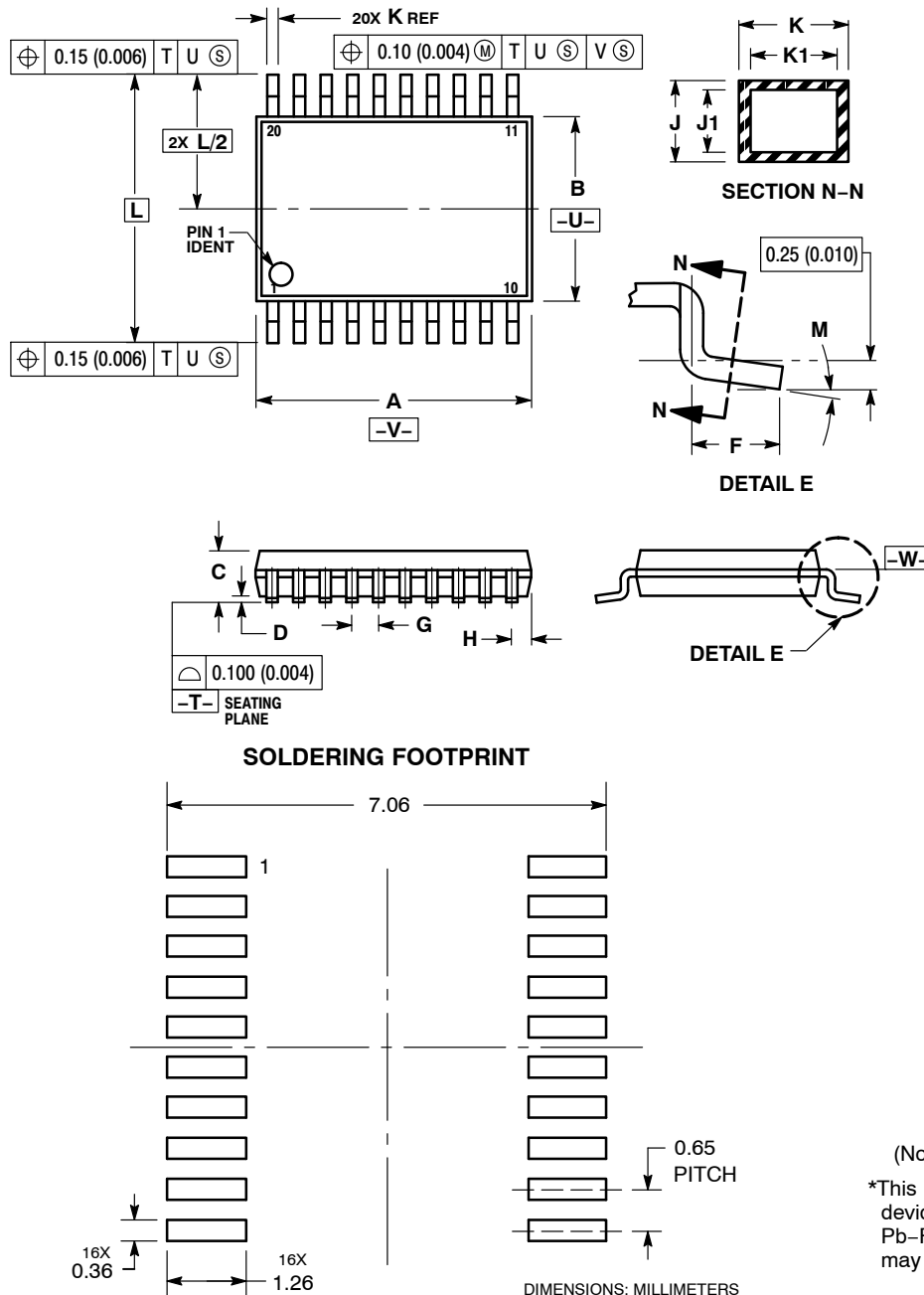
ON



SCALE 2:1

TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER: 98ASH70169A

Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: TSSOP-20 WB

PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales