

# Quad 2-Channel Multiplexer

With 5 V-Tolerant Inputs

## MC74LVX157

The MC74LVX157 is an advanced high speed CMOS quad 2-channel multiplexer. The inputs tolerate voltages up to 5.5 V, allowing the interface of 5.0 V systems to 3.0 V systems.

It consists of four 2-input digital multiplexers with common select (S) and enable ( $\bar{E}$ ) inputs. When  $\bar{E}$  is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the I0 n or I1 n inputs get routed to the corresponding Z n outputs.

### Features

- High Speed:  $t_{PD} = 5.1$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25$  °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:  
Human Body Model > 2000 V
- These Devices are Pb-Free and are RoHS Compliant

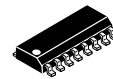
### PIN NAMES

Pins	Function
I0n	Source 0 Data Inputs
I1n	Source 1 Data Inputs
$\bar{E}$	Enable Input
S	Select Input
Zn	Outputs

### TRUTH TABLE

INPUTS				OUTPUT
$\bar{E}$	S	I0n	I1n	Zn
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level; For  $I_{CC}$  Reasons DO NOT FLOAT Inputs

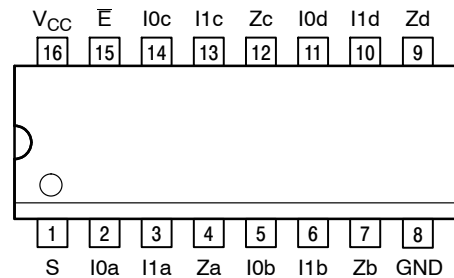


SOIC-16  
D SUFFIX  
CASE 751B



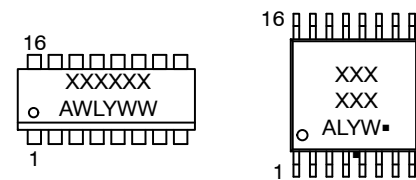
TSSOP-16  
DT SUFFIX  
CASE 948F

### PIN ASSIGNMENT



16-Lead (Top View)

### MARKING DIAGRAMS



SOIC-16

TSSOP-16

XXXXXX = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

## MC74LVX157

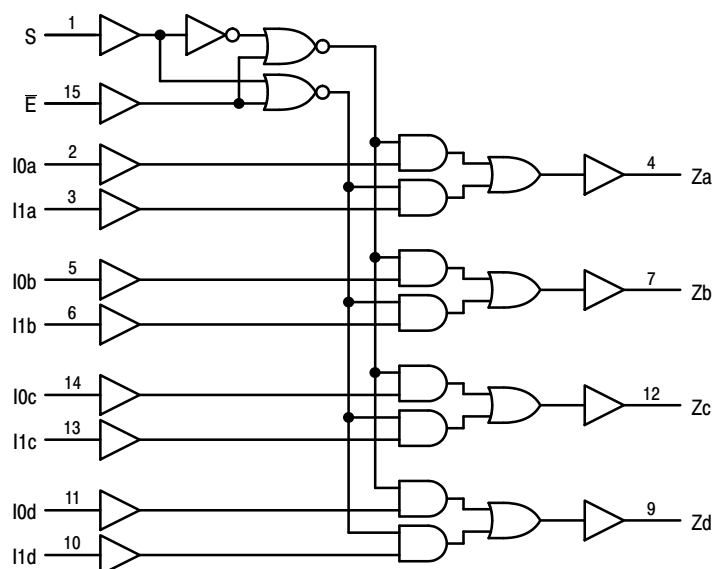


Figure 1. Logic Diagram

### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage	−0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
I <sub>IK</sub>	Input Clamp Current	−20	mA
I <sub>OK</sub>	Output Clamp Current	±20	mA
T <sub>STG</sub>	Storage Temperature Range	−65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 1)	SOIC-16 TSSOP-16 126 159	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25 °C	SOIC-16 TSSOP-16 995 787	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.

2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4	– – –	– – –	1.5 2.0 2.4	– – –	V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6	– – –	– – –	0.5 0.8 0.8	– – –	0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0 –	– – –	1.9 2.9 2.48	– – –	V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0	– – –	0.0 0.0 –	0.1 0.1 0.36	– – –	0.1 0.1 0.44	V
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	3.6	–	–	±0.1	–	±1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6	–	–	4.0	–	40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Input to Output	V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF	–	6.6	12.5	1.0	15.5	ns
		C <sub>L</sub> = 50pF	–	9.1	16.0	1.0	19.0	
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF	–	5.1	7.9	1.0	9.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, S to Zn	C <sub>L</sub> = 50pF	–	7.6	11.4	1.0	13.0	ns
		V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF	–	8.9	16.9	1.0	20.5	
		C <sub>L</sub> = 50pF	–	11.4	20.4	1.0	24.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, $\bar{E}$ to Zn	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF	–	7.0	11.0	1.0	13.0	ns
		C <sub>L</sub> = 50pF	–	9.5	14.5	1.0	16.5	
		V <sub>CC</sub> = 2.7V C <sub>L</sub> = 15pF	–	9.1	17.6	1.0	20.5	
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output-to-Output Skew (Note 3)	C <sub>L</sub> = 50pF	–	11.6	21.1	1.0	24.0	ns
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF	–	7.2	11.5	1.0	13.5	
		C <sub>L</sub> = 50pF	–	9.7	15.0	1.0	17.0	
t <sub>OSSL</sub> , t <sub>OSLH</sub>	Output-to-Output Skew (Note 3)	V <sub>CC</sub> = 2.7V C <sub>L</sub> = 50pF	–	–	1.5	–	1.5	ns
		V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 50pF	–	–	1.5	–	1.5	

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

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## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T <sub>A</sub> = 25 °C			T <sub>A</sub> = -40 to 85 °C		Unit
		Min	Typ	Max	Min	Max	
C <sub>in</sub>	Input Capacitance	–	4	10	–	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 4)	–	20	–	–	–	pF

4. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/4$  (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 3.3V, Measured in SOIC Package)

Symbol	Characteristic	T <sub>A</sub> = 25 °C		Unit
		Typ	Max	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.5	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	–0.3	–0.5	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage	–	2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage	–	0.8	V

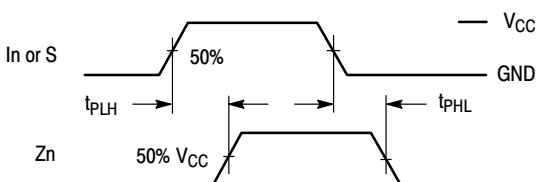


Figure 2.

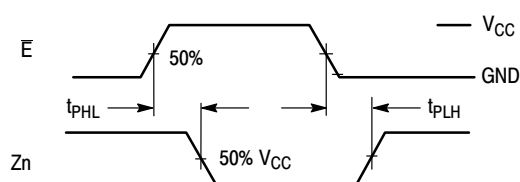


Figure 3.

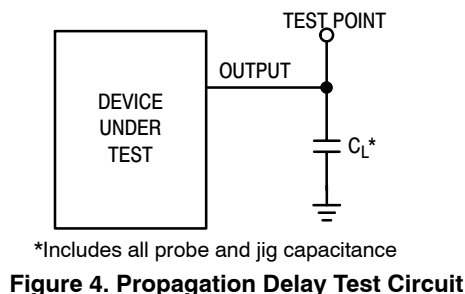


Figure 4. Propagation Delay Test Circuit

## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
MC74LVX157DR2G	LVX157G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LVX157DTR2G	LVX 157	TSSOP-16 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

## MC74LVX157

### REVISION HISTORY

Revision	Description of Changes	Date
6	Revision to change the value in the text (the inputs tolerate voltages) from 7.0 V to 5.5 V, replace the pictures of the marking Diagrams and remove "Machine Model > 200 V" from the Features on page 1, replace the Max. Rating table on page 2, add a new column to the Ordering Inf. table on page 4, add the revision history table on the last page.	05/06/2024


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

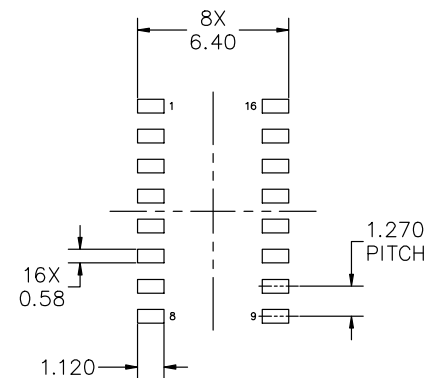
DATE 18 OCT 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

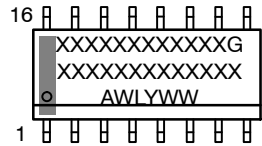
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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 1 OF 2</b>

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SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

DATE 18 OCT 2024

GENERIC  
MARKING DIAGRAM\*

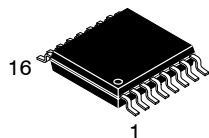


XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006

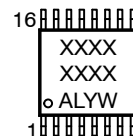

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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