Plastic Medium-Power PNP Silicon Transistor

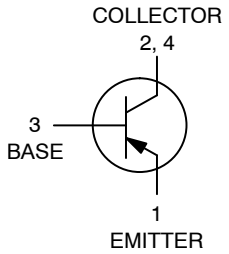
MJE350G

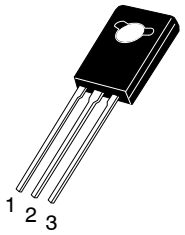
0.5 AMPERE POWER TRANSISTOR PNP SILICON 300 VOLTS, 20 WATTS

This device is designed for use in line−operated applications such as low power, line−operated series pass and switching regulators requiring PNP capability.

Features

- High Collector−Emitter Sustaining Voltage
- Excellent DC Current Gain
- Complement to MJE340
- These Devices are Pb−Free and are RoHS Compliant*





TO−225
CASE 77−09
STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Emitter−Base Voltage	V_{EB}	3.0	Vdc
Collector Current − Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 20 0.16	 W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	6.25	°C/W

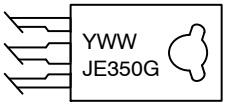
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



Y = Year
WW = Work Week
JE350 = Device Code
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE350G	TO−225 (Pb−Free)	500 Units/Box

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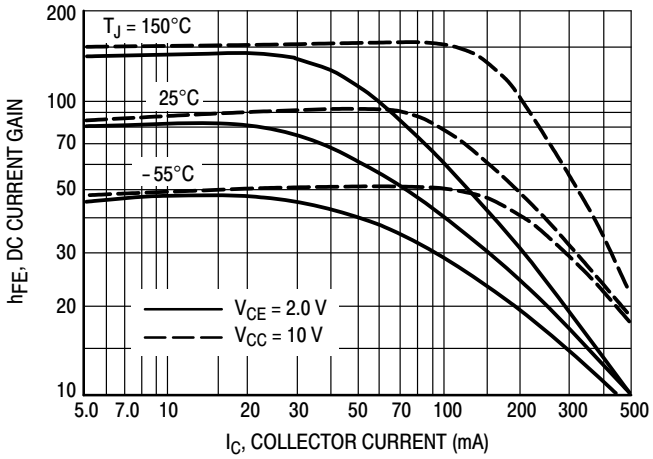


Figure 1. DC Current Gain

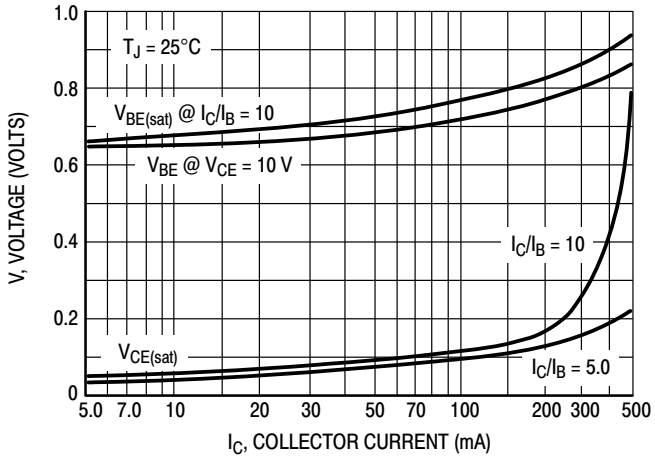


Figure 2. "On" Voltages

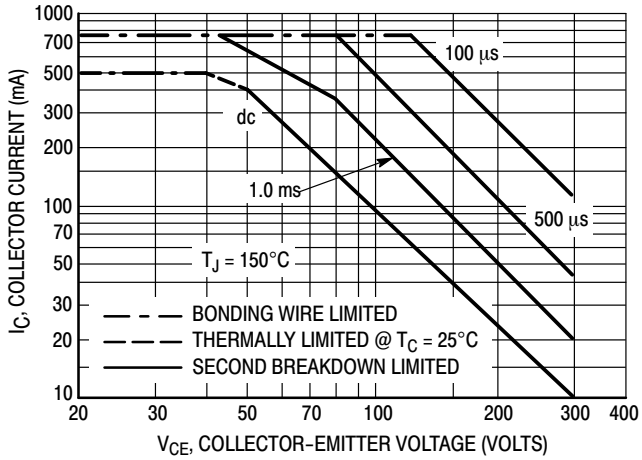


Figure 3. Active−Region Safe Operating Area

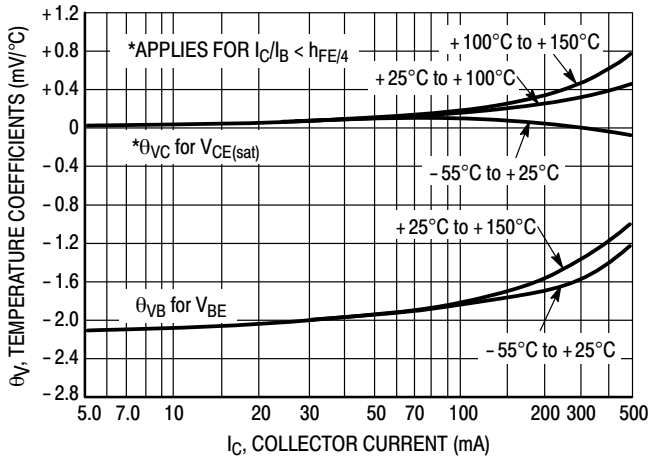


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

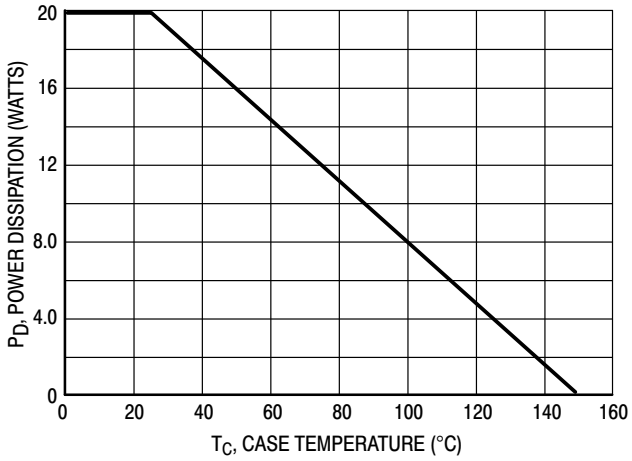
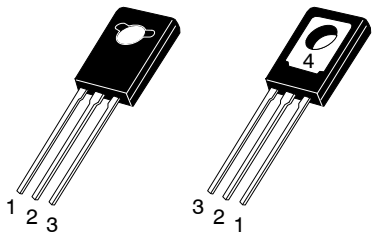


Figure 5. Power Derating



FRONT VIEW BACK VIEW

SCALE 1:1

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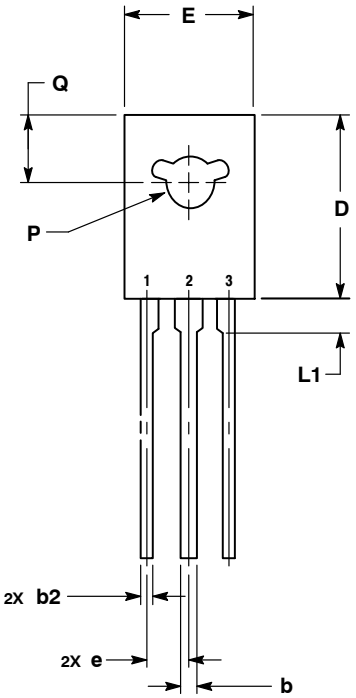
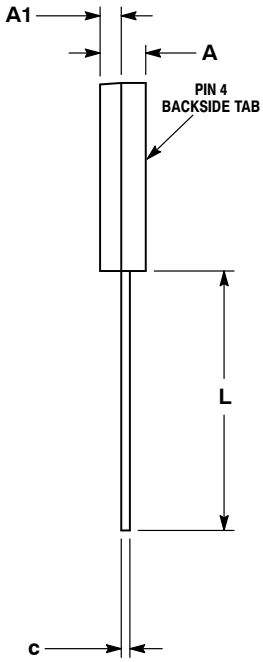
CASE 77−09
ISSUE AD

DATE 25 MAR 2015



FRONT VIEW

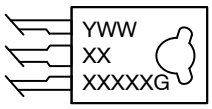


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. NUMBER AND SHAPE OF LUGS OPTIONAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	2.40	3.00
A1	1.00	1.50
b	0.60	0.90
b2	0.51	0.88
c	0.39	0.63
D	10.60	11.10
E	7.40	7.80
e	2.04	2.54
L	14.50	16.63
L1	1.27	2.54
P	2.90	3.30
Q	3.80	4.20

GENERIC MARKING DIAGRAM*



Y = Year
WW = Work Week
XXXXX = Device Code
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. EMITTER
2., 4. COLLECTOR
3. BASE

STYLE 2:
PIN 1. CATHODE
2., 4. ANODE
3. GATE

STYLE 3:
PIN 1. BASE
2., 4. COLLECTOR
3. EMITTER

STYLE 4:
PIN 1. ANODE 1
2., 4. ANODE 2
3. GATE

STYLE 5:
PIN 1. MT 1
2., 4. MT 2
3. GATE

STYLE 6:
PIN 1. CATHODE
2., 4. GATE
3. ANODE

STYLE 7:
PIN 1. MT 1
2., 4. GATE
3. MT 2

STYLE 8:
PIN 1. SOURCE
2., 4. GATE
3. DRAIN

STYLE 9:
PIN 1. GATE
2., 4. DRAIN
3. SOURCE

STYLE 10:
PIN 1. SOURCE
2., 4. DRAIN
3. GATE

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