MMJT9410

Bipolar Power Transistors

NPN Silicon

Features

- SOT−223 Surface Mount Packaging
- Epoxy Meets UL 94 V−0 @ 0.125 in
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	30	Vdc
Collector − Base Voltage	V_{CB}	45	Vdc
Emitter − Base Voltage	V_{EB}	± 6.0	Vdc
Base Current − Continuous	I_B	1.0	Adc
Collector Current − Continuous	I_C	3.0	Adc
Collector Current − Peak	I_{CM}	5.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	3.0 24 1.7 0.75	W mW/°C W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

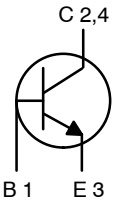
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	42	°C/W
Thermal Resistance, Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	$R_{\theta JA}$	165	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

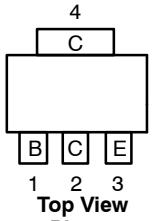
ON Semiconductor®

http://onsemi.com

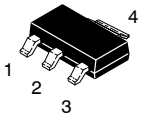
POWER BJT
I_C = 3.0 AMPERES
BV_{CEO} = 30 VOLTS
$V_{CE(sat)}$ = 0.2 VOLTS



Schematic

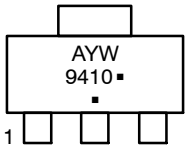


Top View
Pinout



SOT−223
CASE 318E
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
9410 = Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MMJT9410G	SOT−223 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0 Adc)	$V_{CEO(sus)}$	30	–	–	Vdc
Emitter−Base Voltage (I_E = 50 μAdc, I_C = 0 Adc)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 25 Vdc, R_{BE} = 200 Ω) (V_{CE} = 25 Vdc, R_{BE} = 200 Ω, T_J = 125°C)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	–	–	10	μAdc
ON CHARACTERISTICS (Note 1)					
Collector−Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 20 mAdc) (I_C = 1.2 Adc, I_B = 20 mAdc) (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	– – –	0.105 0.150 –	0.150 0.200 0.450	Vdc
Base−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base−Emitter On Voltage (I_C = 1.2 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.2 Adc, V_{CE} = 1.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	85 80 60	200 – –	– – –	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0 Adc, f = 1.0 MHz)	C_{ob}	–	85	135	pF
Input Capacitance (V_{EB} = 8.0 Vdc)	C_{ib}	–	200	–	pF
Current−Gain − Bandwidth Product (Note 2) (I_C = 500 mA, V_{CE} = 10 Vdc, F_{test} = 1.0 MHz)	f_T	–	72	–	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{FE}| \bullet f_{test}$

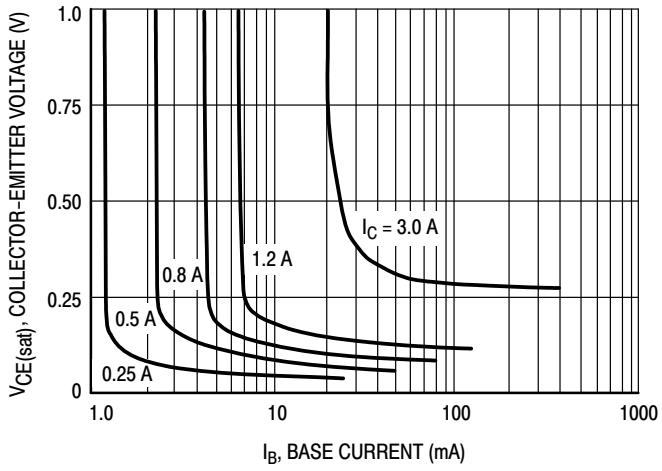


Figure 1. Collector Saturation Region

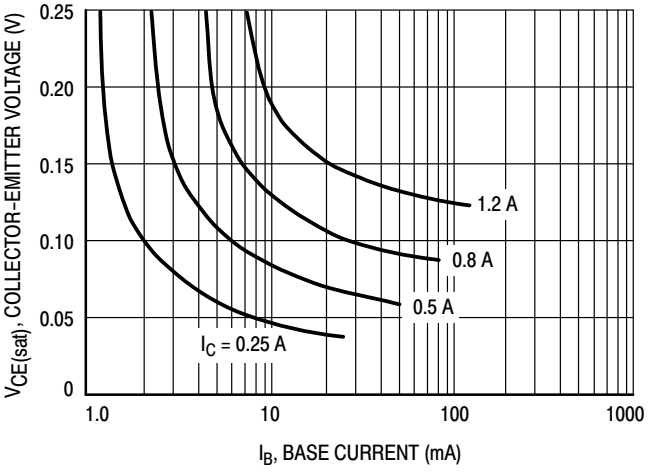


Figure 2. Collector Saturation Region

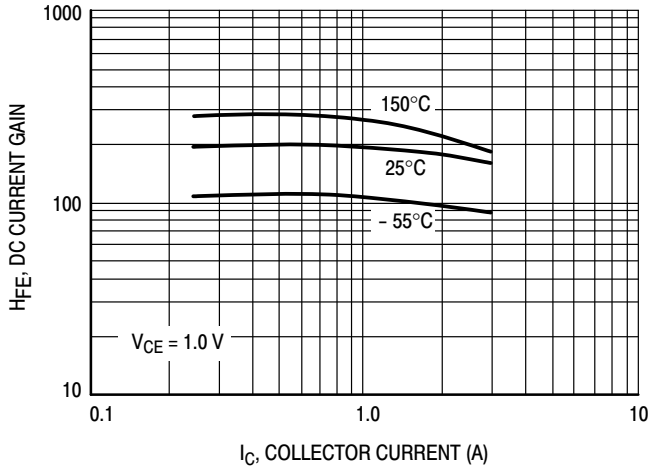


Figure 3. DC Current Gain

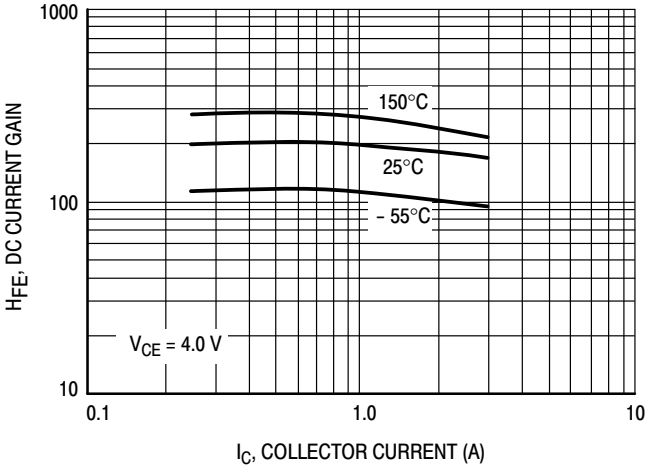


Figure 4. DC Current Gain

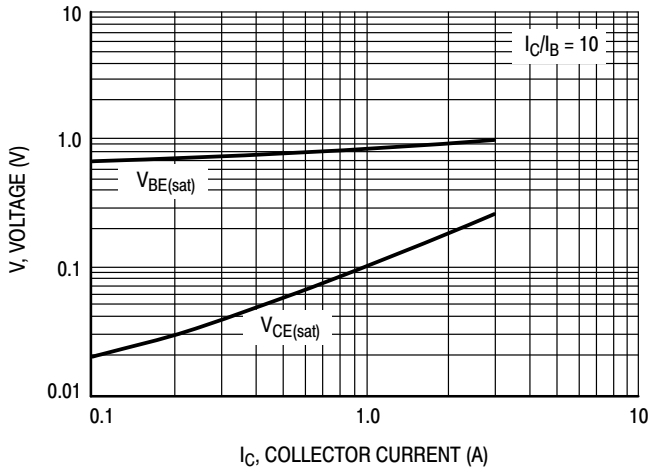


Figure 5. “On” Voltages

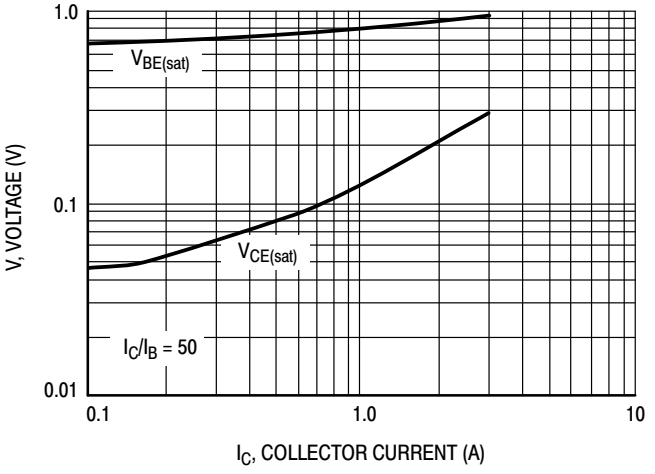


Figure 6. “On” Voltages

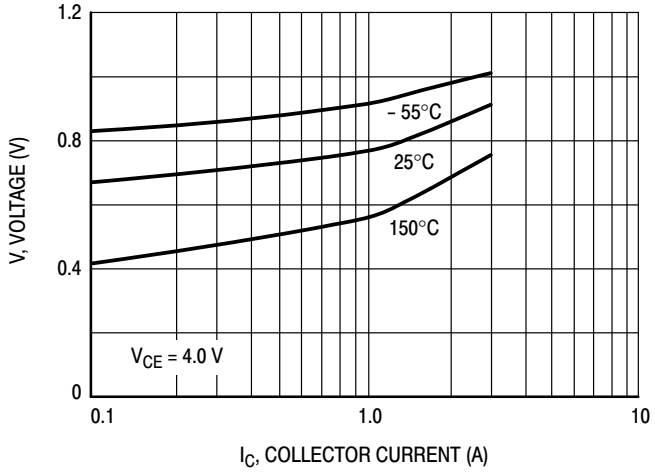


Figure 7. $V_{BE(on)}$ Voltage

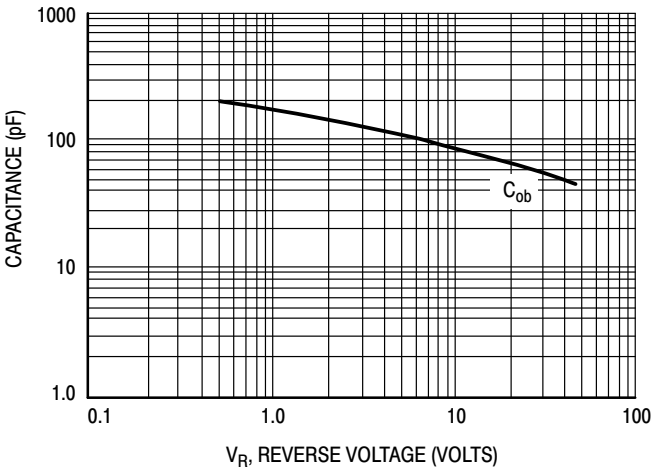


Figure 8. Capacitance

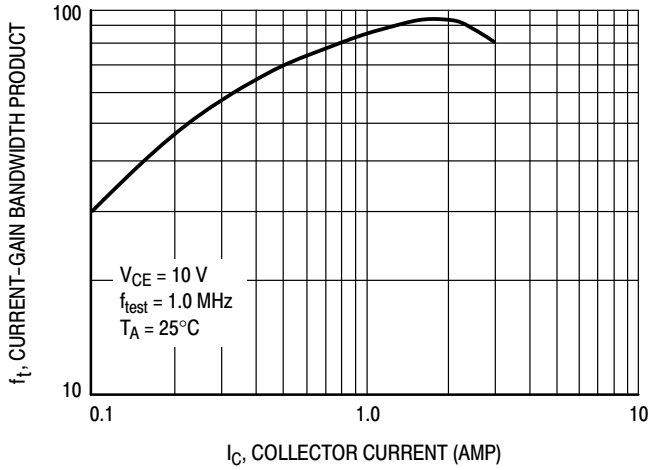


Figure 9. Current−Gain Bandwidth Product

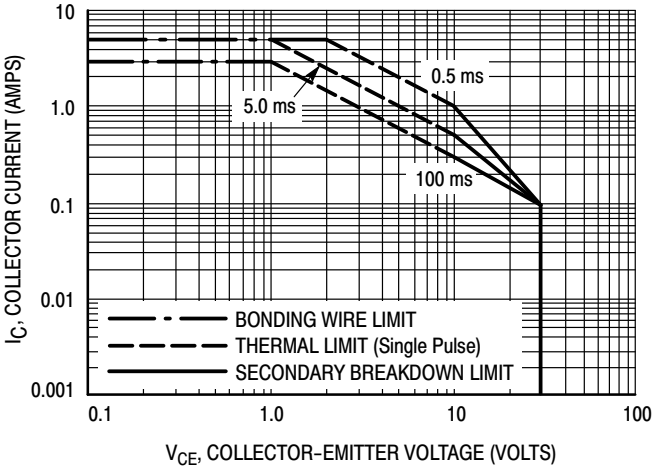


Figure 10. Active Region Safe Operating Area

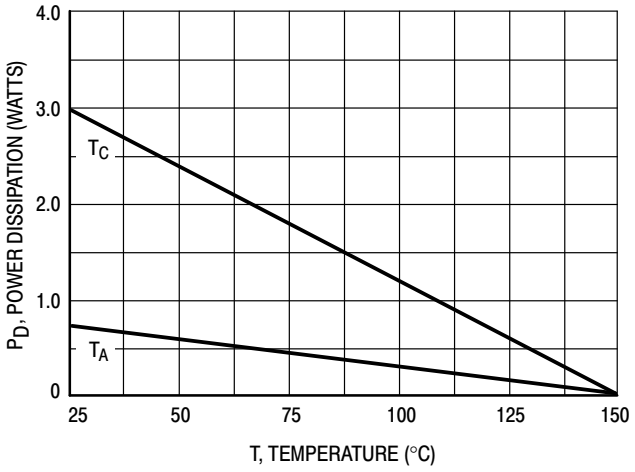


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

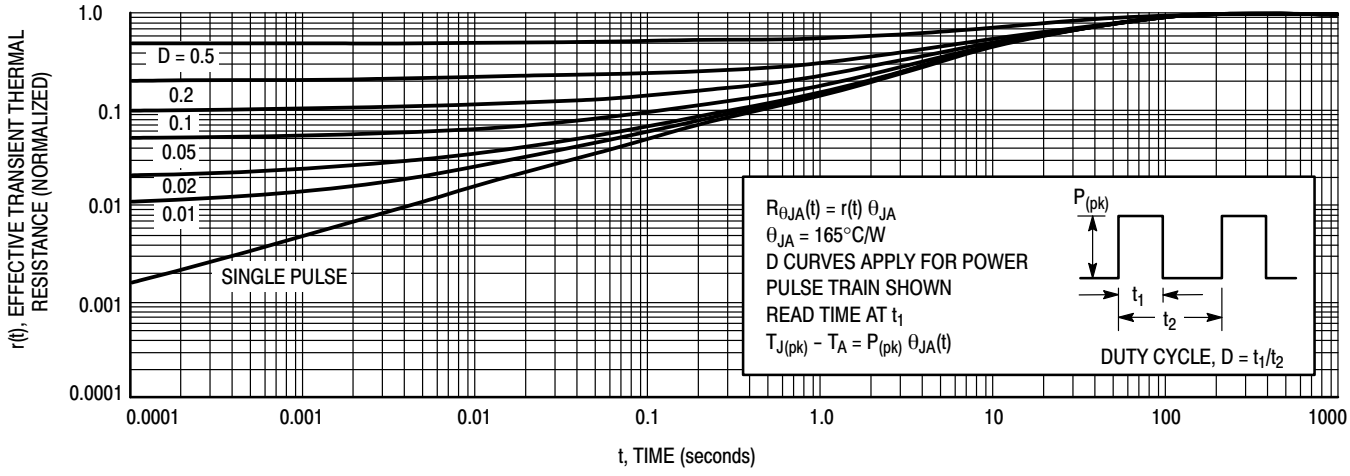
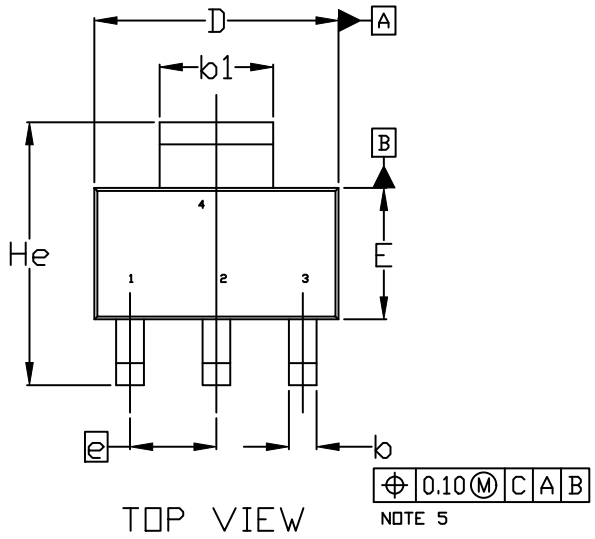


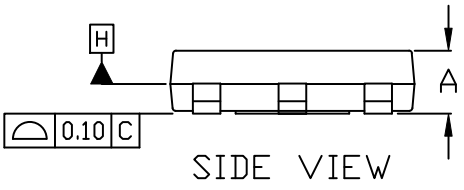
Figure 12. Thermal Response

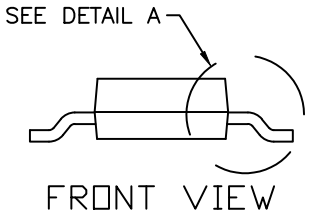
SCALE 1:1

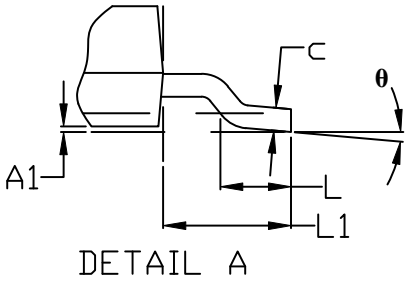
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



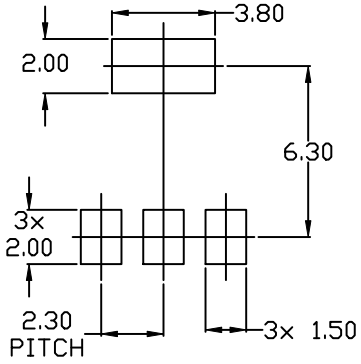






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

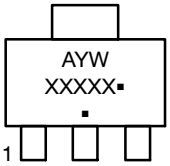
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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