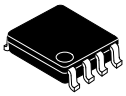
TinyLogic UHS Triple Inverter

NC7NZ04

MARKING DIAGRAMS



US8
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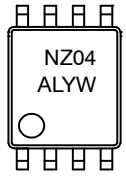

UQFN8 1.6X1.6, 0.5P
CASE 523AY

NZ04, T3	= Specific Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

Desription

The NC7NZ04 is a triple inverter from **onsemi**'s Ultra−High Speed (UHS) series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra−high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V_{CC} operating voltage.

Features

- Ultra−High Speed: t_{PD} = 2.4 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V Power−Down, High−Impedance Inputs / Outputs
- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Space−Saving MicroPak™ and US8 Surface Mount Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

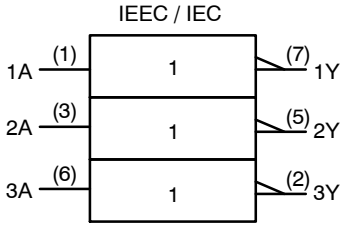

Figure 1. Logic Symbol

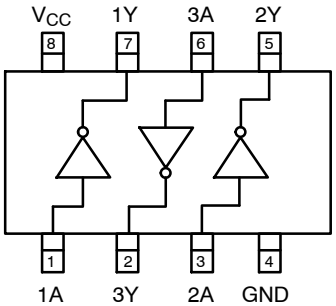

Figure 2. Connection Diagram

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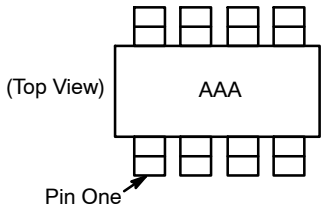
Pin Configurations



NOTES:
1. AAA represents product code top mark (see ordering table).
2. Orientation of top mark determines pin one location. Reading the top product code mark left to right, pin one is the lower left pin.

Figure 3. US8

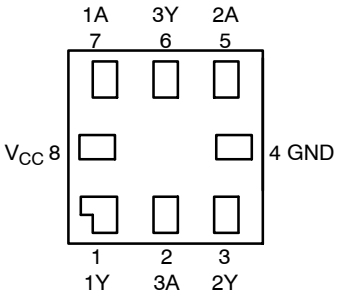


Figure 4. MicroPak (Top Through View)

PIN DEFINITIONS

Pin # US8	Pin # MicroPak	Name	Description
1	7	1A	Input
2	6	3Y	Output
3	5	2A	Input
4	4	GND	Ground
5	3	2Y	Output
6	2	3A	Input
7	1	1Y	Output
8	8	V_{CC}	Supply Voltage

FUNCTION TABLE

Inputs	Output
A	**Y**
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	–	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	–	−50	mA
I_{OUT}	DC Output Current		–	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		–	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		–	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		–	+260	°C
P_D	Power Dissipation in Still Air	US8	–	500	mW
		MicroPak−8	–	539	
ESD	Human Body Model, JEDEC: JESD22−A114		–	4000	V
	Charge Device Model, JEDEC: JESD22−C101		–	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} at 3.3 V ±0.3 V	0	10	
		V_{CC} at 5.0 V ±0.5 V	0	5	
θ_{JA}	Thermal Resistance	US8	–	250	°C/W
		MicroPak−8	–	232	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Conditions	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
		2.30 to 5.50		0.70 V_{CC}	–	–	0.70 V_{CC}	–	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95		–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
		2.30 to 5.50		–	–	0.30 V_{CC}	–	0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL}, I_{OH} = −100 μA	1.55	1.65	–	1.55	–	V
		2.30		2.20	2.30	–	2.20	–	
		3.00		2.90	3.00	–	2.90	–	
		4.50		4.40	4.50	–	4.40	–	
		1.65	I_{OH} = −4 mA	1.29	1.52	–	1.29	–	
		2.30	I_{OH} = −8 mA	1.90	2.15	–	1.90	–	
		3.00	I_{OH} = −16 mA	2.40	2.80	–	2.40	–	
		3.00	I_{OH} = −24 mA	2.30	2.68	–	2.30	–	
		4.50	I_{OH} = −32 mA	3.80	4.20	–	3.80	–	
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IH} or V_{IL}, I_{OH} = −100 μA	–	0.00	0.10	–	0.10	V
		2.30		–	0.00	0.10	–	0.10	
		3.00		–	0.00	0.10	–	0.10	
		4.50		–	0.00	0.10	–	0.10	
		1.65	I_{OH} = 4 mA	–	0.80	0.24	–	0.24	
		2.30	I_{OH} = 8 mA	–	0.10	0.30	–	0.30	
		3.00	I_{OH} = 16 mA	–	0.15	0.40	–	0.40	
		3.00	I_{OH} = 24 mA	–	0.22	0.55	–	0.55	
		4.50	I_{OH} = 32 mA	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	V_{IN} = 5.5 V, GND	–	–	±1	–	±1	μA
I_{OFF}	Power−Off Leakage Current	0	V_{IN} or V_{OUT} = 5.5 V	–	–	1	–	10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN} = 5.5 V, GND	–	–	1	–	10	μA

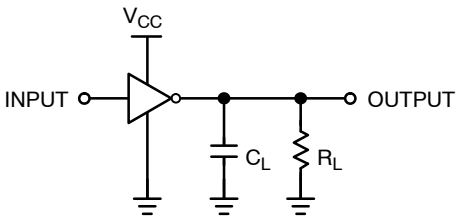
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Conditions	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 5, 6)	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ	–	4.4	9.5	–	10.0	ns
		2.50 ±0.20		–	2.9	5.1	–	5.6	
		3.30 ±0.30		–	2.1	3.4	–	3.8	
		5.00 ±0.50		–	1.8	2.8	–	3.1	
		3.30 ±0.30	C_L = 50 pF, R_L = 500 Ω	–	2.9	4.5	–	5.0	
		5.00 ±0.50		–	2.4	3.6	–	4.0	
C_{IN}	Input Capacitance	0		–	2.5	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Note 4) (Figure 7)	3.30		–	9	–	–	–	pF
		5.00		–	11	–	–	–	

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output lading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	Unit
				Typ	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 5.0 V, V_{IL} = 0 V	5.0	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}		5.0	−0.8	V



NOTE:
5. C_L includes load and stray capacitance; inputs PRR = 1.0 MHz, t_W = 500 ns.

Figure 5. AC Test Circuit

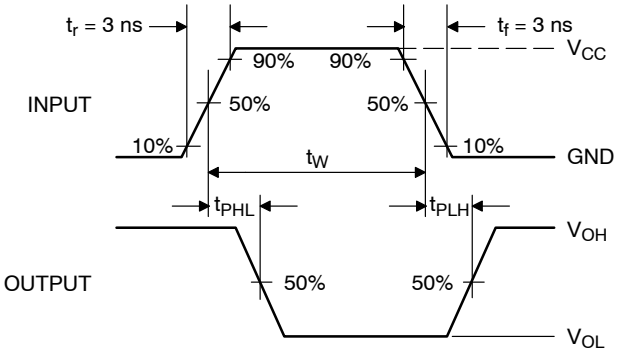
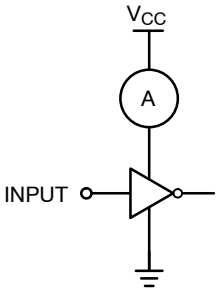


Figure 6. AC Waveforms



NOTE:
6. Input = AC Waveform; $t_r = t_f$ = 1.8 ns; PRR = 10 MHz; Duty Cycle = 50%.

Figure 7. I_{CCD} Test Circuit

DEVICE ORDERING INFORMATION

Device	Top Mark	Packages	Shipping†
NC7NZ04K8X	NZ04	8−Lead US8, JEDEC MO−187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7NZ04K8X−L22236	NZ04	8−Lead US8, JEDEC MO−187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7NZ04L8X	T3	8−Lead MicroPak, 1.6 mm Wide	5000 / Tape & Reel
NC7NZ04L8X−L22185	T3	8−Lead MicroPak, 1.6 mm Wide	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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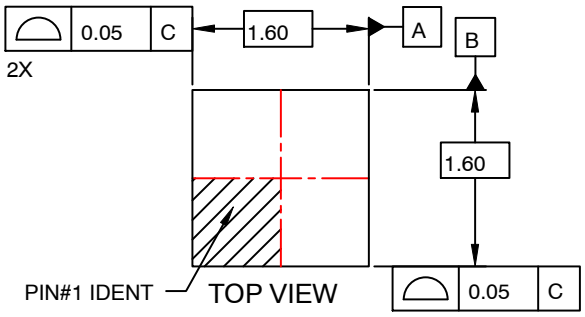
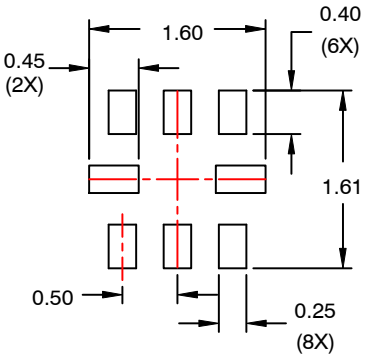
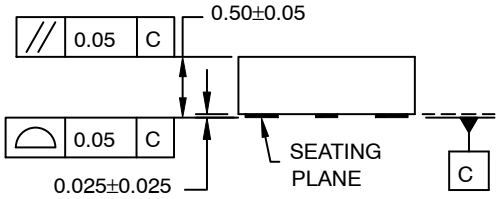




RECOMMENDED
LAND PATTERN



SIDE VIEW

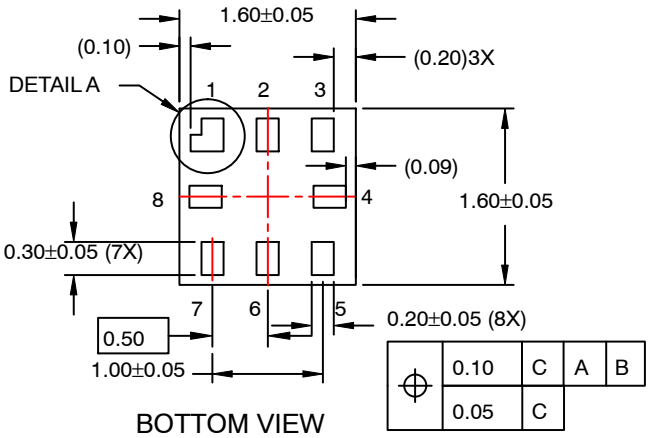
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

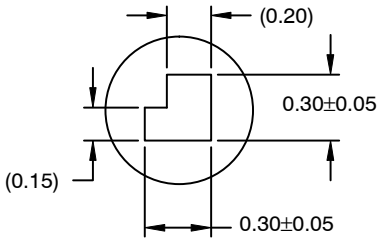
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



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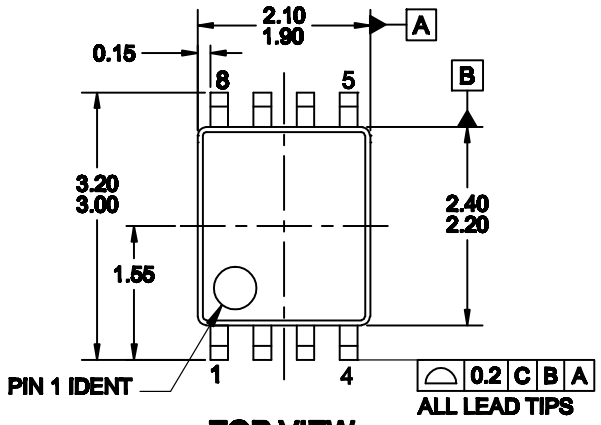
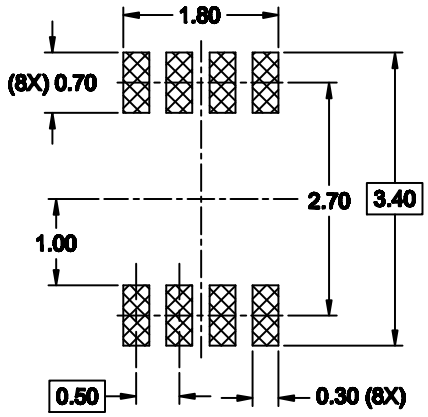


TOP VIEW



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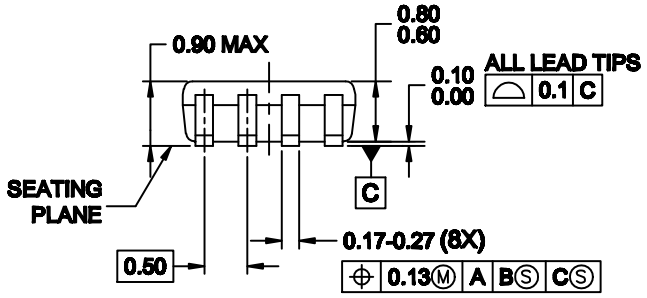

SIDE VIEW

NOTES:

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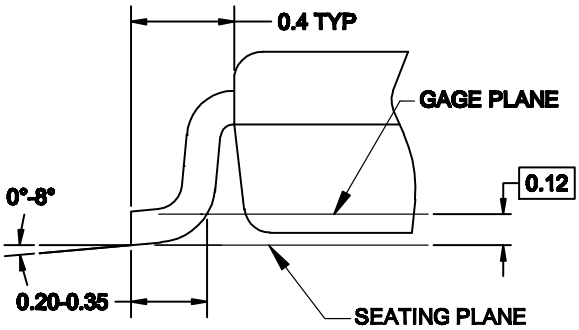

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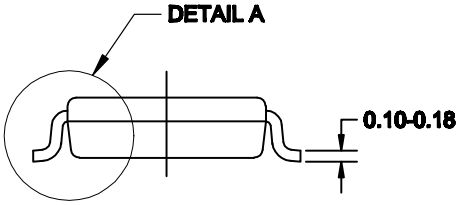

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