NCP1589L

Low Voltage Synchronous Buck Controller with Light Load Efficiency and Transient Enhancement

The NCP1589L is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V and converting voltage from as low as 2.5 V. It is easy to operate and provides an optimal level of integration to reduce size and cost of the power supply. It operates in Ramp Pulse Modulation mode for superior load step and release response. In addition to fast transient response, it also includes a 1.5 A gate driver design and light load efficiency features such as adaptive non−overlap circuitry and diode emulation. It normally operates at a range of 200−500 kHz in continuous current conduction mode, which reduces with current at light load for further power saving. Protection features include programmable overcurrent protection, output overvoltage and undervoltage protection and input undervoltage lockout (UVLO).

Features

- V_{CC} Range from 4.5 V to 13.2 V
- Adjustable Operating frequency
- Boost Pin Operates to 35 V
- Ramp Pulse Modulation Control
- Precision 0.8 V Internal Reference
- Adjustable Output Voltage
- Internal 1.5 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- Adaptive Diode Mode Emulation in Light Load
- This is a Pb−Free Device

Applications

- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC−DC Regulator Modules

ON Semiconductor®

http://onsemi.com

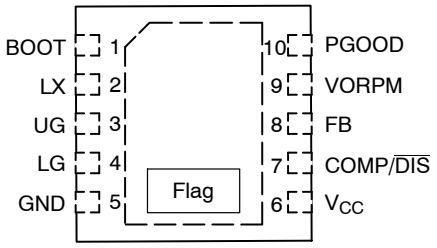
DFN10
CASE 485C

MARKING DIAGRAM

1589L	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Device

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1589LMNTWG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

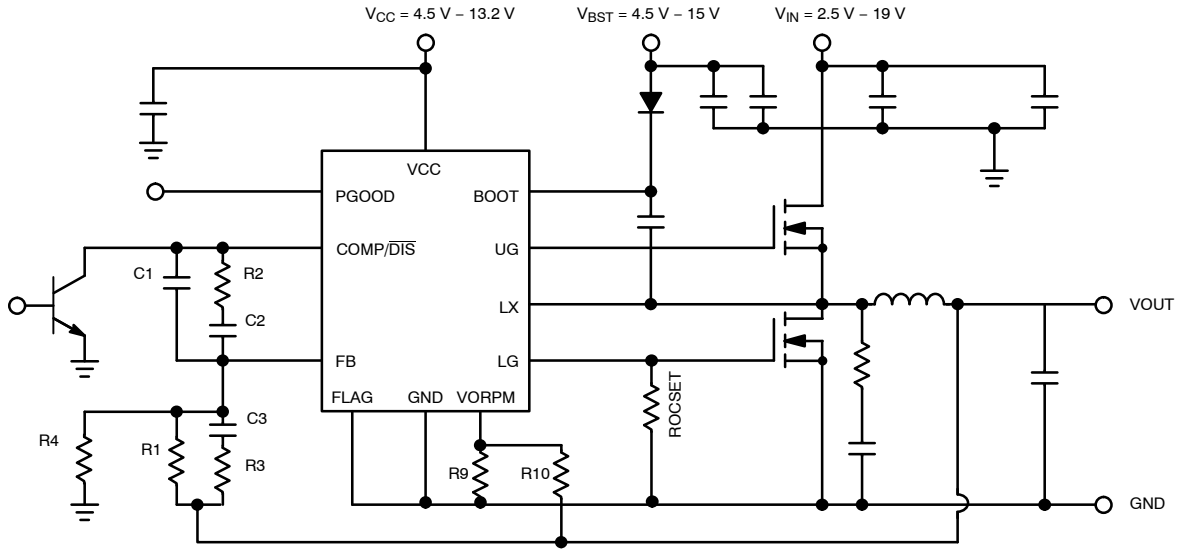


Figure 1. Typical Application Diagram

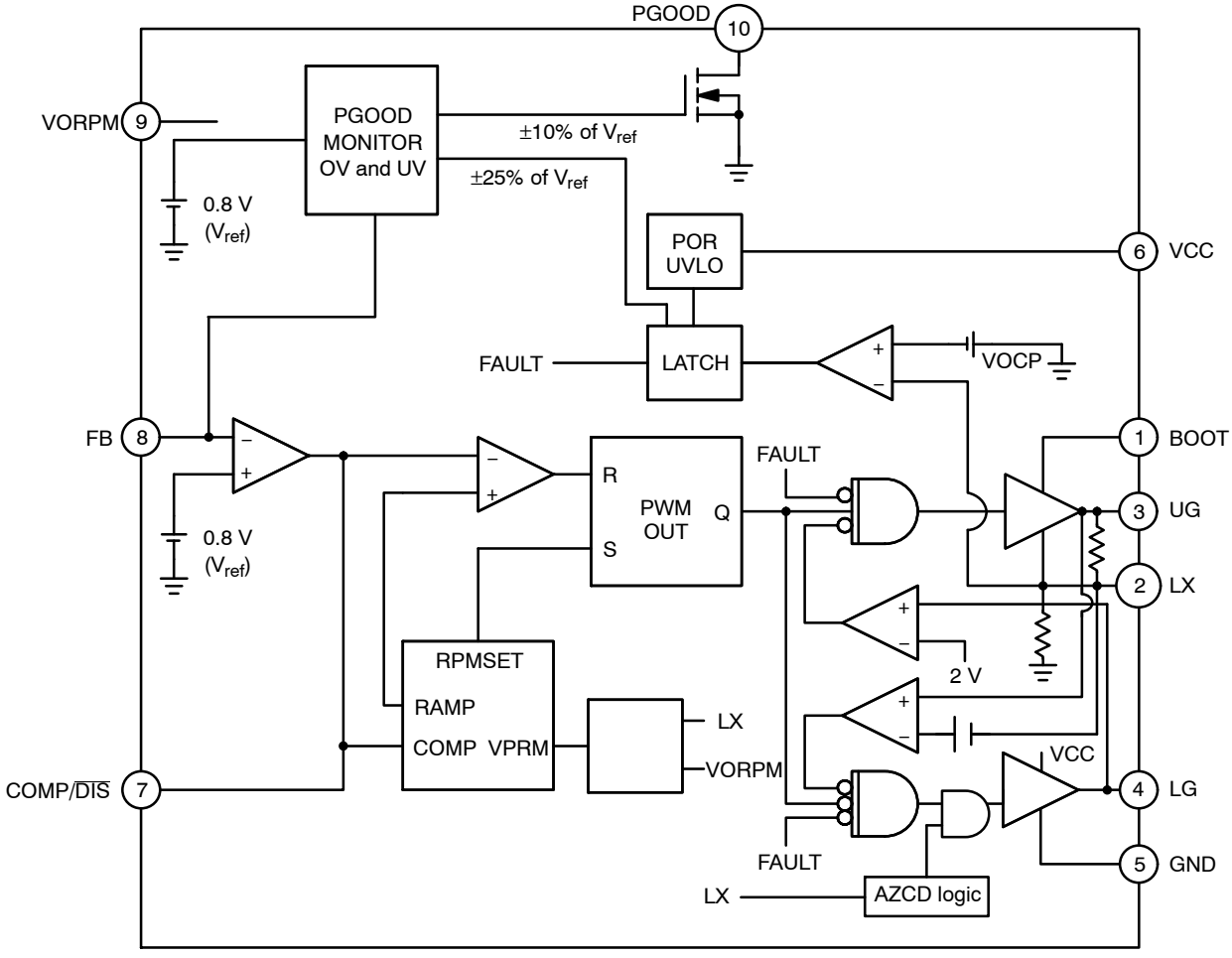


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BOOT	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BOOT pin). Connect a capacitor (C_{BOOT}) between this pin and the LX pin. Typical values for C_{BOOT} range from 0.1 μF to 1 μF. Ensure that C_{BOOT} is placed near the IC.
2	LX	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET. Also used for low side MOSFET $R_{DS(on)}$ current detection and diode emulation.
3	UG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−channel MOSFET.
4	LG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−channel MOSFET. Also used to set the overcurrent limit.
5	GND	IC ground reference. All control circuits are referenced to this pin. Connect to FLAG.
6	VCC	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC. Also low−side MOSFET drive voltage.
7	COMP/$\overline{DIS}$	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. Pull this pin low for disable.
8	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to V_{out}.
9	VORPM	Output voltage information for RPM threshold
10	PGOOD	Power Good output. Pulled Low if VFB is outside ±10% of 0.8 V V_{ref}.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	VCC	15 V	−0.3 V
Bootstrap Supply Voltage Input	BOOT	35 V wrt/GND 40 V < 100 ns 15 V wrt/LX	−0.3 V −0.3 V −0.3 V
Switching Node (Bootstrap Supply Return)	LX	35 V 40 V for < 100 ns	−5 V −10 V for < 200 ns
High−Side Driver Output (Top Gate)	UG	30 V wrt/GND 15 V wrt/LX 40 V for < 100 ns	−0.3 V wrt/LX −5 V for < 200 ns
Low−Side Driver Output (Bottom Gate)	LG	15 V	−0.3 V −5 V for < 200 ns
Feedback, VORPM	FB, VORPM	6.0 V	−0.3 V
COMP/$\overline{DIS}$	COMP/$\overline{DIS}$	5.5 V	−0.3 V
PGOOD	PGOOD	7 V	−0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	165	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Operating Junction Temperature Range	T_J	0 to 150	°C
Operating Ambient Temperature Range	T_A	0 to 95	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (0°C < T_A < 95°C; 4.5 V < [BOOT−LX] < 13.2 V, 4.5 V < BOOT < 30 V, 0 V < LX < 21 V, C_{TG} = C_{BG} = 1.0 nF, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
V_{CC} Input Voltage Range		4.5		13.2	V
BOOT Voltage Range	13.2 V wrt LX	4.5		30	V
dV/dt on V_{CC}		−10		10	V/μs
VREF AND ERROR AMPLIFIER					
Reference Voltage	Vref		0.8		V
Output Voltage Accuracy	Reference and Error Amplifier Excluding External Resistive Divider Tolerance	−1.0		1.0	%
SUPPLY CURRENT					
V_{CC} Quiescent Supply Current	No Switching, V_{CC} = 13.2 V		2.5	3.8	mA
BOOT Quiescent Current	No Switching	0.1		100	μA
UNDERVOLTAGE LOCKOUT					
V_{CC} UVLO Threshold	V_{CC} Rising		4.4		V
V_{CC} UVLO Threshold	V_{CC} Falling		4.0		V
V_{CC} UVLO Hysteresis	V_{CC} Rising or V_{CC} Falling		400		mV
SWITCHING REGULATOR					
Ramp Slope			0.5		V/μs
Ramp−Amplitude Voltage			1.50		V
Minimum Duty Cycle			0		%
Maximum Duty Cycle		70	83	92	%
LG Minimum on Time		200		350	ns
ERROR AMPLIFIER					
Open Loop DC Gain (Note 1)		80	120		dB
Output Source Current Output Sink Current	V_{fb} < 0.8 V V_{fb} > 0.8 V	2.0 2.0			mA
Unity Gain Bandwidth (Note 1)		15			MHz
Disable Threshold		0.7	0.8	0.9	V
Output Source Current During Disable			10	40	μA
GATE DRIVERS					
Upper Gate Source	BOOT − LX = 5 V	1.5			A
Upper Gate Sink	BOOT − LX = 5 V		1.8		Ω
Lower Gate Source	V_{CC} = 5 V	1.5			A
Lower Gate Sink	V_{CC} = 5 V		1.2		Ω
UG Falling to LG Rising Delay Tdead1 (Note 1)	V_{CC} = 12 V, UG−LX < 1.0 V, LG > 1.0 V Only Valid for CCM Operating Mode		20	30	ns
LG Falling to UG Rising Delay Tdead2 (Note 1)	V_{CC} = 12 V, LG < 1.0 V, UG > 1.0 V Only Valid for CCM Operating Mode		20	30	ns
UG Internal Resistor to LX	Unbiased, BOOT − LX = 0		45		kΩ
LX Internal Resistor to GND			45		kΩ
SOFT−START					
Soft−Start Time	V_{CC} > 4.5 V, COMP ≥ Disable Threshold		2.0	2.6	ms
Enable to Soft−Start Delay (Note 1)	V_{CC} > 4.5 V, COMP Rises and Crosses Disable Threshold			500	μs

1. Guaranteed by design but not tested in production.

ELECTRICAL CHARACTERISTICS (0°C < T_A < 95°C; 4.5 V < [BOOT−LX] < 13.2 V, 4.5 V < BOOT < 30 V, 0 V < LX < 21 V, C_{TG} = C_{BG} = 1.0 nF, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
POWER GOOD INCLUDING OVP AND UVP THRESHOLD					
Output Voltage	Logic Low, Sinking 4 mA			0.4	V
Overvoltage until PGOOD goes low			880	902	mV
Undervoltage until PGOOD goes low		698	720		mV
PGOOD High Upper Limit Hysteresis			16		mV
PGOOD High Lower Limit Hysteresis			16		mV
OVP Threshold to Part Disable		950	1000	1030	mV
UVP Threshold to Part Disable		570	600	630	mV
Power Good Delay (Note 1)				1.0	μs
ZERO CURRENT DETECTION (LX Pin)					
Zero Current Detection Blank Timer after TG < 1.0 V	LX > 50 mV, LG on time	200	250	350	ns
Capture Time for LX Voltage (Note 1)	Time to Capture LX Voltage Once LG is < 1.0 V			40	ns
ZERO CURRENT V_{th} ADJUSTMENT DETECTION (LX Pin)					
Negative LX Detection Voltage	Vbdls	200	300	400	mV
Positive LX Detection Voltage	Vbdhs	0.2	0.5	1.0	V
Time for V_{th} Adjustment and Settling Time	300 kHz	3.0		3.7	μs
Zero Current Detection Blank Timer after LG < 1.0 V (Note 1)	Blanking Time After LG is < 1.0 V			40	ns
Initial Negative Current Detection Threshold Voltage Setpoint (Note 1)	LX−GND, Includes ±2 mV Offset Range	−5.0	−3.0	−1.0	mV
V_{th} Adjustable Range (Note 1)		−16	0	15	mV
OVERCURRENT PROTECTION					
OC Current Source	Sourced from LG pin, before SS	9.5	10	10.5	μA
OCP Programming Time	V_{CC} > 4.5 V, R_{oscset} = 60 kΩ	1.0		5.0	ms

1. Guaranteed by design but not tested in production.

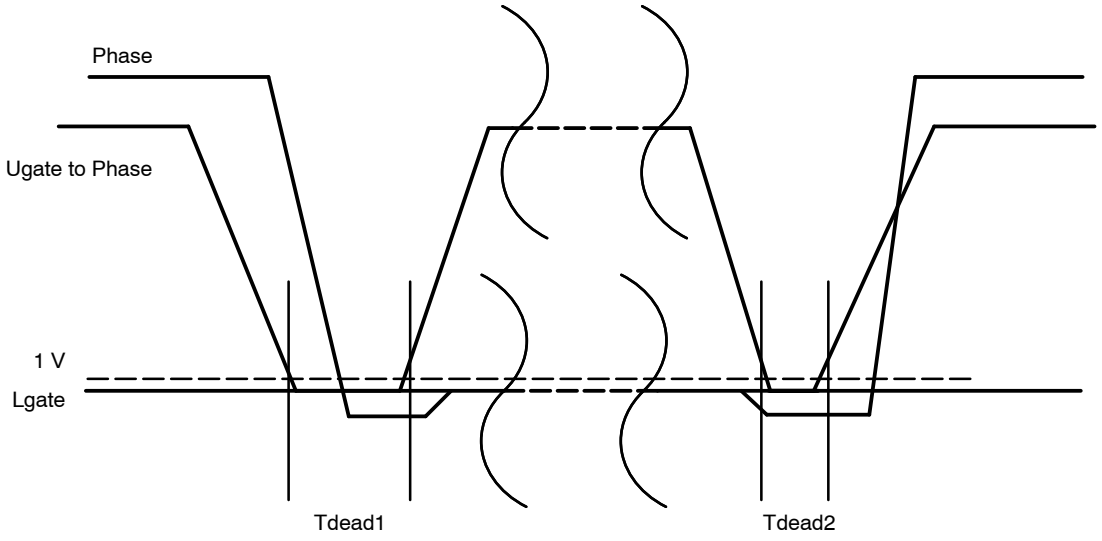


Figure 3. Dead Time Definition

APPLICATIONS INFORMATION

Overcurrent Protection (OCP)

The NCP1589L monitors the voltage across the low side MOSFET and used this information to determine if there is excessive output current. The voltage across the low side MOSFET is measured from the LX pin when it is conducted, and is referenced to ground. The overcurrent measurement is timed to occur at the end of the low side MOSFET conduction period.

If the voltage drop across the bottom MOSFET exceeds the overcurrent protection threshold, then an internal counter is triggered and incremented. If the voltage drop does not exceed the threshold for the next cycle, the internal counter will be reset. The NCP1589L will latch the over current protection fault condition after 4 consecutive cycles of overcurrent events.

When the NCP1589L latches an overcurrent protection fault, both the high side and low side MOSFETs are turned off. To reset the overcurrent protection fault, the power to the V_{CC} pin must be cycled.

The overcurrent threshold can be set externally, by varying the R_{OCSET} resistor shunted from low side gate pin to ground. During power on reset, after the V_{CC} and BOOT pins both pass the undervoltage lockout threshold, the NCP1589L will source a 10 μA current from LG pin through the R_{OCSET} resistor and produce a voltage. This voltage will be sampled and locked by the device as the overcurrent protection threshold. For example, if R_{OCSET} is set to 10 kΩ, the 10 μA of current will yield a 100 mV threshold, and if the voltage across the low side MOSFET exceeds 100 mV at the end of the its conduction period, an overcurrent event will be detected. The OCP threshold is only associated with power on reset, and won't be wiped out by pulling COMP pin down (disabling the part).

If the R_{OCSET} resistor is not present, the overcurrent protection threshold will max out at 640 mV. The recommended range for R_{OCSET} is 5 kΩ to 60 kΩ which yields a threshold voltage range of 50 mV to 600 mV.

Internal Soft−Start

To prevent excess inrush current during startup, the NCP1589L uses a calibrated current source with an internal soft−start capacitor to ramp the reference voltage from 0 V to 800 mV over a period of around 4 ms. The soft−start ramp generator will reset if the input power supply voltages reach the undervoltage lockout threshold, or if the NCP1589L is disabled by having the COMP pin pulled low.

Startup into a Precharged Load

During a startup, the NCP1589L will detect the residual charge on the output capacitors. Instead of fully discharging the capacitors, the soft−start will begin from the precharged output voltage level. For example, if the NCP1589L is configured to provide a regulated output voltage of 2.5 V, the normal soft−start sequence will ramp the output voltage from 0 to 2.5 V in 4.2 ms; however if the output capacitors already has 1.2 V voltage, the NCP1589L will not discharge the capacitors, instead the soft−start sequence will begin at 1.2 V and then ramp the output up to 2.5 V.

Power Good

The PGOOD pin is an open drain connection, with an active high output to signal the condition of the converter. PGOOD is pulled low during soft−start cycle, and if there is overvoltage or undervoltage fault. If the voltage on the FB pin is within ±10% of V_{ref} (800 mV) then the PGOOD pin will not be pulled low. The PGOOD pin does not have an internal pull-up resistor.

Overvoltage Protection (OVP)

If the voltage on the FB pin exceeds the overvoltage threshold (1000 mV, 125% of V_{ref}), the NCP1589L will latch an overvoltage fault. During an overvoltage fault event the UG pin will be pulled low, and the LG pin will stay high until the voltage on the FB pin goes below $V_{ref}/2$ (400 mV). If the overvoltage fault condition stays, the NCP1589L will continue drive the LG pin, LG will go high if FB exceeds 1000 mV, then go low when FB is below 400 mV. The power of the NCP1589L needs to be cycled up to clear the overvoltage fault.

Undervoltage Protection (UVP)

If the voltage on the FB pin falls below the undervoltage threshold after the soft−start cycle completes, then the NCP1589L will latch an undervoltage fault. During an undervoltage fault, both the UG and LG pins will be pulled low. Toggling power or COMP pin will reset the undervoltage protection unit.

VORPM (RPM threshold)

The NCP1589L runs in RPM mode, its switching frequency is controlled by COMP ripple voltage and RPM threshold. The VORPM pin is connected to the output voltage through an external divider. This voltage value is proportional to the output voltage and sets the RPM threshold voltage internally with input voltage information obtained through the switch node. The internal RPM threshold voltage (DTH) is a function of both V_{out} and V_{in}.

$$DTH = \frac{V_{out} \times \frac{R9}{R10+R9}}{V_{in}} \times V_{ramp} + V_{offset} \qquad \text{(eq. 1)}$$

Where R9/R10 (Figure 1) is the input voltage divider of VORPM pin V_{ramp} is the internal ramp amplitude, V_{offset} is the offset voltage of the threshold.

Each time when COMP voltage exceeds RPM threshold voltage, an internal ramp signal is started and UG is driven high. When the internal ramp intercepts with COMP voltage, the UG pin is reset low. The NCP1589L system operates at pseudo-fixed frequency in continuous current

conduction mode. The output frequency can be determined by the following equation:

$$F_{SW} = \frac{k1 \times Ramp\_slope}{\left(\frac{V_{out} \times \frac{R9}{R10+R9}}{V_{in}} \times V_{ramp} + V_{offset}\right)} \times \frac{1}{1 + k2} \times \frac{V_{out}}{V_{in}} \quad \text{(eq. 2)}$$

Where k1, k2 is an internal trimmed value; by default, k1 = 1, k2 = 0, Ramp_slope = 0.5 V/μs, V_{ramp} = 1.5 V, V_{offset} = 20 mV.

Light Load Operation

In continuous current conduction mode, the operating frequency of the NCP1589L is almost constant. In light load, it runs in a discontinuous current mode with a scaled-down frequency as a function of the load current. Internal zero current detection threshold will change adaptively to ensure the minimum amount of diode conduction period to further reduce the converter power consumption in the light load condition.

Feedback Voltage

The NCP1589L allows the output voltage to be adjusted from 0.8 V to 5 V via an external resistor divider network (R1, R4 in Figure 1). The controller will try to maintain 0.8 V at the FB pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{out}, the controller will regulate the output voltage in proportion to the resistor divider ratio in order to maintain 0.8 V at the FB pin. The relation between the resistor divider network and the output voltage is show in the following equation:

$$R4 = R1 \times \left(\frac{V_{ref}}{V_{out} - V_{ref}}\right) = R1 \times \left(\frac{0.8\ V}{V_{out} - 0.8\ V}\right) \quad \text{(eq. 3)}$$

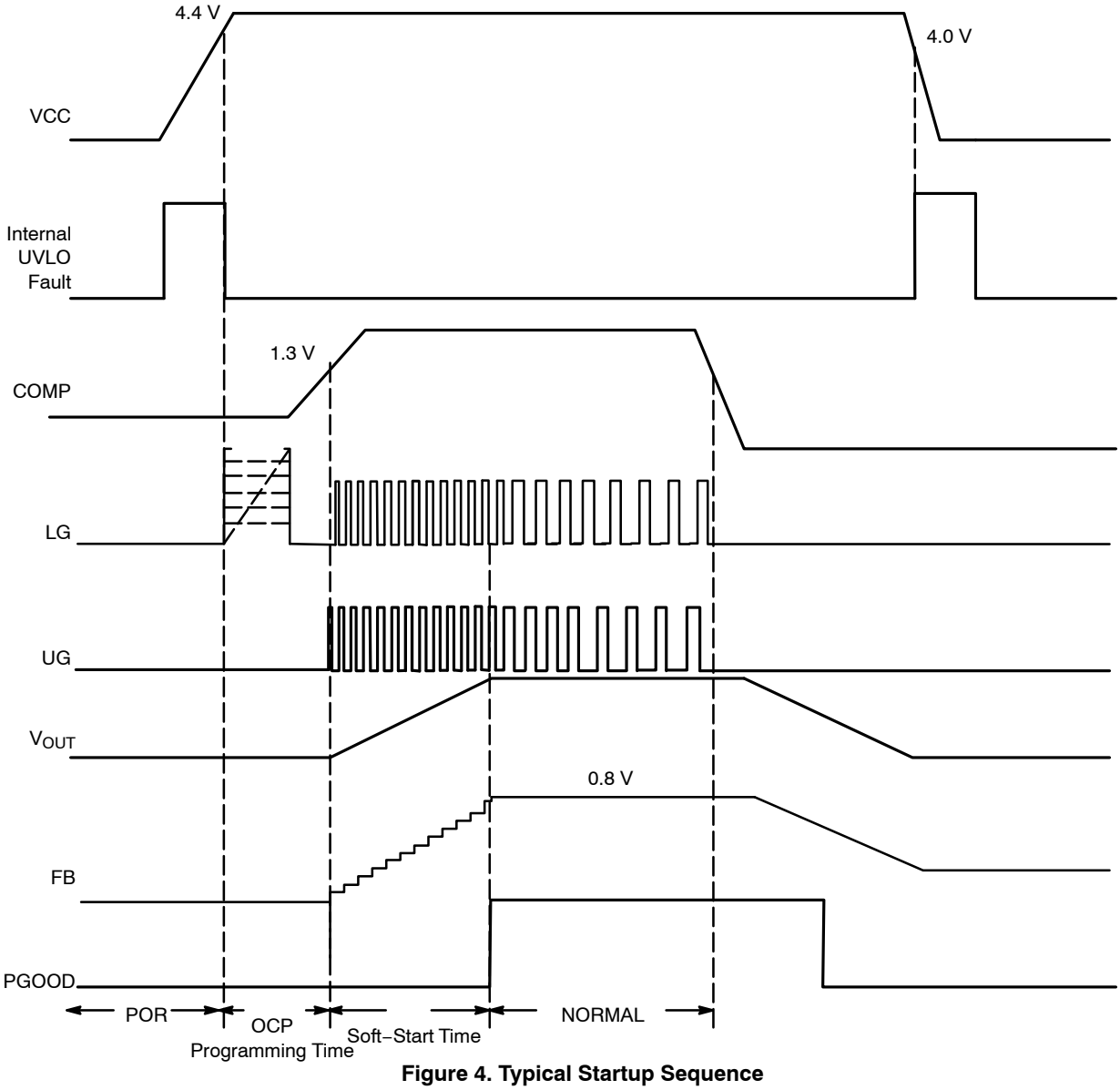
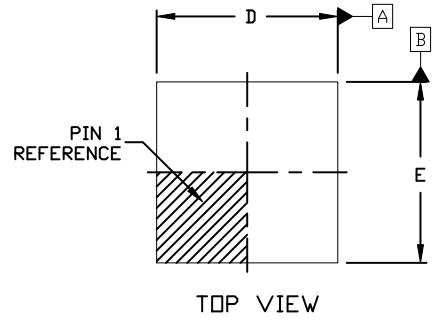


Figure 4. Typical Startup Sequence

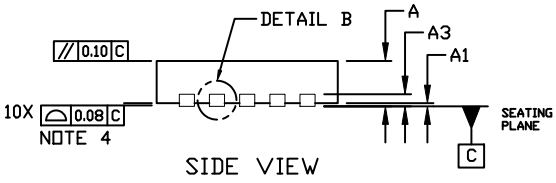
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

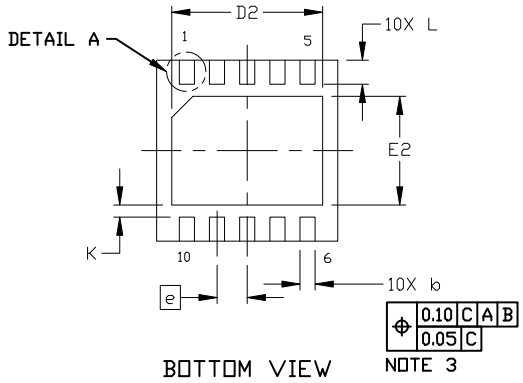
SCALE 2:1



TOP VIEW

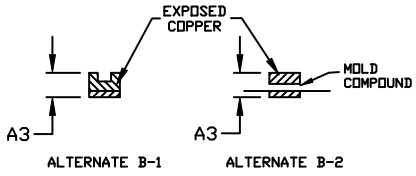


SIDE VIEW

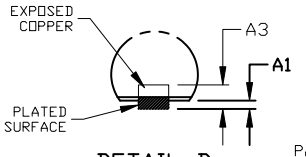


BOTTOM VIEW

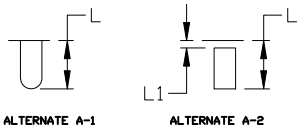
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

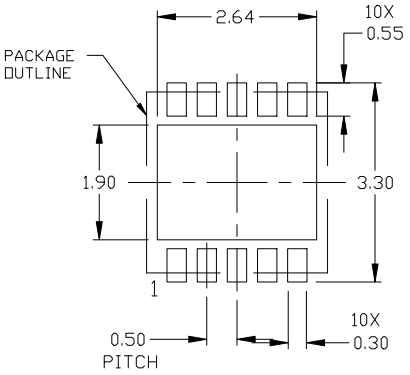


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

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