26V, 4-Channel Voltage Bus and 4-Channel High-Side Current Shunt Monitor

NCP45491

The NCP45491 is a high−performance monolithic IC which can be used to monitor bus voltage and current on four high−voltage power supplies simultaneously. The HV bus voltages and currents are translated to a low−voltage power domain and multiplexed onto a single differential output for measurement externally by common ADCs. The device is configurable to operate either standalone or as a pair, permitting up to eight separate HV power supplies to be monitored and measured.

Features

- Translates and Scales Shunt and Bus Voltages up to 26 V
- Single Device Monitors Four Supplies
- May Be Paired for Monitoring Up To Eight Supplies
- Very Low Powerdown Current
- All Channels Individually Gain Programmable by External Resistor Selection
- Fast Settling Time
- Real−Time Indication of All Bus Voltages Valid
- Adjustable Output Common−Mode Voltage Adapts to Most External ADCs
- Lead−Free Device

Applications

- Computers/Notebooks
- Graphical Cards
- Power Management/Power Control Loops
- Battery Chargers

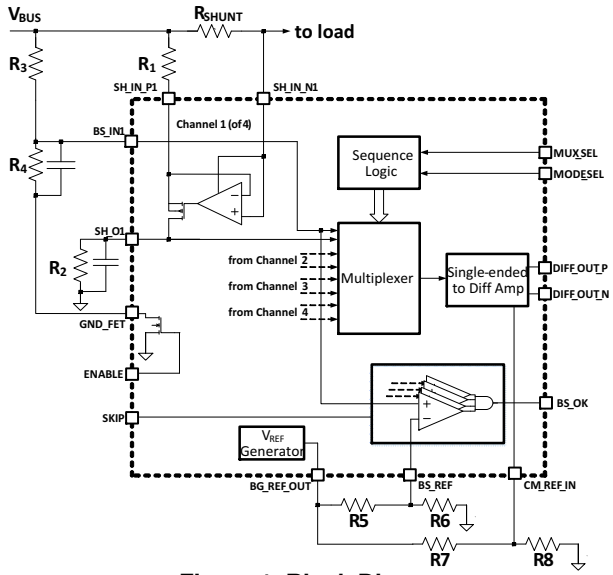
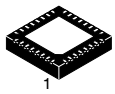


Figure 1. Block Diagram

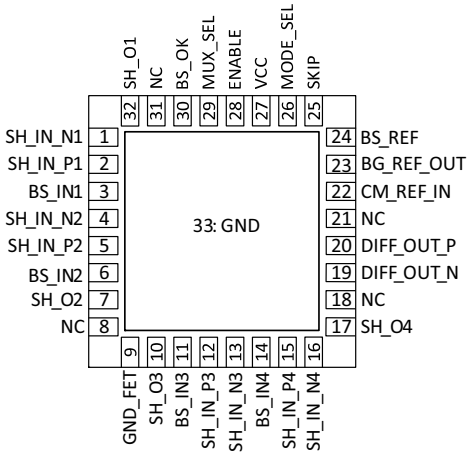


QFN32 4x4
CASE 485CD

MARKING DIAGRAM

45491 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
CCCCC = Country of Assembly

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP45491XMNTWG	QFN32 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Table 1. PIN DESCRIPTION

Pin	Name	I/O	Function
2, 5, 12, 15	SH_IN_Px	AI	Shunt Resistor Sense +, High Voltage
1, 4, 13, 16	SH_IN_Nx	AI	Shunt Resistor Sense –, High Voltage
32, 7, 10, 17	SH_Ox	AO	Shunt Voltage Gain Set / Filter, Current Output
3, 6, 11, 14	BS_INx	AI	Bus Voltage Sense, High Impedance Input
20	DIFF_OUT_P	AO	Differential Output, Positive
19	DIFF_OUT_N	AO	Differential Output, Negative
22	CM_REF_IN	AI	Common–Mode Reference for Differential Output
29	MUX_SEL	DI	Multiplexer Select Input
24	BS_REF	AI	Bus OK Reference Input
30	BS_OK	DO	Bus OK output (open–drain; high impedance = BUS OK)
28	ENABLE	DI	Device Enable. When high, places device in low–power state
23	BG_REF_OUT	AO	Buffered Bandgap Voltage Output
9	GND_FET	AO	Low–side GND ref for resistor dividers (open drain type)
25	SKIP	DI	Skip Function control (see description)
26	MODE_SEL	AI	Multi–level Input for single–device, device A, or device B modes
8, 18, 21,31	NC		Pins must be floated
27	VCC	PWR	Device Power
PAD	GND	GND	Device Ground

Table 2. MAXIMUM RATINGS

Rating	Pins	Condition	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	GND = 0 V	V_{CC}	–0.3 to 5.5	V
Shunt Input Voltage Range	SH_IN_Px, SH_IN_Nx	GND = 0 V	$V_{SH_IN_X}$	–0.3 to 30	V
Bus Input Voltage Range	BS_INx	GND = 0 V	V_{BS_IN}	–0.3 to 30	V
Grounding FET Range	GND_FET	GND = 0 V	V_{GND_FET}	–0.3 to 30	V
Shunt Output Voltage Range	SH_Ox	GND = 0 V	V_{SH_Ox}	–0.3 to 5.5	V
Digital Input Voltage Range	MUX_SEL, ENABLE, SKIP, MODE_SEL	GND = 0 V	V_{EN}	–0.3 to 5.5	V
Low Voltage I/O Range	BS_REF, CM_REF_IN, MODE_SEL, DIFF_OUT_P, DIFF_OUT_N, BS_OK, BG_REF_OUT	GND = 0 V	V_{LV}	–0.3 to 5.5	V
Thermal Resistance, Junction–to–Air			$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction–to–Case (V_{IN} Paddle)			$R_{\theta JC}$	5	°C/W
Operating Temperature Range			T_{A1}	–40 to 105	°C
Functional Temperature Range			T_{A2}	–40 to 125	°C
Maximum Junction Temperature			T_J	125	°C
Storage Temperature Range			T_{STG}	–40 to 150	°C
Lead Temperature, Soldering (10 sec.)			T_{SLD}	260	°C
Moisture Sensitivity Level			MSL	1	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. ESD RATINGS

Rating	Symbol	Value	Unit
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	>2.0	kV
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	>0.5	kV
Latch−up Immunity (Note 1)	I_{LU}	100	mA

1. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model per JESD22−C101.
   Latch−up testing per JEDEC78E.

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage Range	V_{CC}	2.8	3.8	V
Shunt Input Voltage Range	$V_{SH_IN_X}$	5	26	V
Shunt Output Voltage Range (operating)	V_{SH_Ox}	0	0.5	V
Shunt Output Voltage Range (floating)	V_{SH_Ox}	2.8	3.8	V
Bus Input Pin Voltage Range (Standby Mode)	V_{BS_INX}	0	26	V
Bus Input Pin Voltage Range (Full Function or Limited Function Mode)	V_{BS_INX}	0	0.5	V
Grounding FET Range	V_{GND_FET}	0	26	V
Low Voltage I/O Range	V_{LV}	0	3.8	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. AC CHARACTERISTICS ($V_{SH_IN_X}$ = 15 V, V_{EN} = 0 V, V_{CC} = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Multiplexer Settling Time (to 9.375 mV)	T_{STAB1}			100	ns
Multiplexer Settling Time (to 3.125 mV)	T_{STAB2}			300	ns
MUX_SEL Period (normal operation)	T_{MSP}	0.185		11	μs
MUX_SEL Reset Period	T_{RP}	35			μs
Power−up Time (STANDBY or Limited Function to Full Function)	T_{PWR_UP}			40	μs
Differential Amplifier Capacitive Load Capability (Note 2)	C_{DIFF}			82	pF

2. Differential Output C_{LOAD} (i.e.: DIFF_OUT_x to GND) appears as a series RC with lumped equivalent R (0.86−8.6 Ω) and C (8.2−82 pF).

Table 6. DC CHARACTERISTICS ($V_{SH_IN_X}$ = 15 V, V_{EN} = 0 V, V_{CC} = 3.3 V, unless indicated otherwise. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +105°C unless noted otherwise and are guaranteed by test, design, characterization, or statistical correlation. Typical values are referenced to T_J = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
MUX_SEL, SKIP, MODE_SEL, ENABLE Logic High	V_{IH}	1.4			V
MUX_SEL, SKIP, MODE_SEL, ENABLE Logic Low	V_{IL}			0.4	V
Input Impedance (MODE_SEL, ENABLE pins)	R_{FLOAT}	100k			Ω
SH_O Pin Current Source Capability	$I_{SH_O_MAX}$			5	mA
Fixed Current for Detection of SH_Ox Open	I_{SH_LEAK}			1	μA
GND_FET ON Resistance (measured @ 1 mA)	R_{GND_FET}			10	Ω
BG_REF_OUT Voltage	V_{BG}	1.274	1.3	1.326	V
BG_REF_OUT Load	IV_{BG_OUT}			100	μA
BS_OK Logic Low Impedance	R_{BS_OK}			300	Ω
VCC range for BS_OK low impedance	V_{LI}	1		3.8	V
VCC Threshold Reference for BS_OK Input (POR) (Note 3)	V_{BS_TH}	2.6		2.8	V
Shunt Monitor Offset Voltage (Note 4)	V_{SM_OV}			±150	μV
Shunt Monitor Offset Voltage Drift (Note 4)	SM_VD			2	μV/°C
Shunt Monitor CMRR ($V_{SH_IN_Px}$ in valid range, see above) (Note 5)	SM_CMRR	80			dB
Valid SH_O resistance	R_{SH_O}			2000	Ω
Differential Amp Input Offset Voltage, room temperature (Note 6)	V_{D_OVRT}			±2	mV
Differential Amp Input Offset Voltage Drift, −40°C to +105°C (Note 6)	V_{D_OVT}			±6	mV
Differential Amp PSRR (V_{CC} = 2.8 V to 3.8 V)	DA_PSRR	60			dB
Differential Amp Common−Mode Voltage	V_{CM}	565		885	mV
Differential Amp Closed Loop Gain	G_{DA}		2		V/V
Differential Full Scale Output	V_{FSO}			800	mV_{pp}
I_VCC (Fully Functional, V_{EN} = 0, V_{CC} must be 2.8 V − 3.8 V)	I_{VCC_F}			1.5	mA
I_VCC (Limited Function, V_{EN} = Tri−state, V_{CC} must be 2.8 V − 3.8 V)	I_{VCC_L}			400	μA
I_VCC (STANDBY) (Note 7)	I_{VCC_S}			180	μA
I_SHO (STANDBY, non−floated SH_Ox pin) (Note 7)	I_{SHO_S}			100	μA
I_SH_IN_N (VBUS current in Full Function) (Note 8)	I_{VBUS}			300	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Vcc detection for BS_OK must trip in this range. Device can be either operational or not operational in this range.
4. Shunt Monitor Offset Voltage and Offset Voltage Drift are referred to the SH_IN_Px and SH_IN_Nx pins.
5. Input Offset voltage at T_J = 25°C.
6. Differential Amplifier Offset Voltage and Offset Voltage Drift are referred to the multiplexer input pins (e.g. BS_INx or SH_Ox).
7. V_{EN} = V_{CC}; Total V_{CC} standby current is I_{VCC_S} plus an additional I_{SHO_S} for every SH_Ox channel that is not floating.
8. Specifications for V_{BUS} current draw are only applicable when V_{CC} = 2.8 V to 3.8 V.

APPLICATIONS INFORMATION

Differential Output Amplifier

A differential output amplifier provides a scaled representation of multiple bus voltages and currents to an external device on the DIFF_OUT_P and DIFF_OUT_N pins. These voltages and currents are presented *sequentially* (under control of the Sequence Logic block) via the Multiplexer. The common−mode voltage of the differential output amplifier is established by the voltage on the CM_REF_IN pin.

Current Shunt Monitor (one of four identical instances)

The differential voltage across an external shunt resistor (R_{SHUNT}) is converted to a current by a transconductor stage implemented by an op−amp and external resistor R1. This current is supplied to the SH_Ox pin where it is converted back to a ground−referenced voltage by external resistor R2. The conversion gain from differential voltage across the shunt resistor to that ground−referred voltage on SH_Ox may then be set directly as the ratio of R_{SHUNT} to R1. A capacitor may be connected across R2 in order to provide noise filtering if required in the application. Note that bias current for the op−amp is taken from the "load" side of the shunt resistor so that it is included in the load current measurement.

Current Shunt Resistors

The external resistors labeled R_{SHUNT}, R1, and R2 in Figure 1 are used to define the full dynamic range of the shunt current monitoring and are user application dependent. Resistors R_{SHUNT} and R1 are chosen based on the maximum load current (I_{LOAD}) to define the SH_Ox current (I_{SH_Ox}) using the equation;

$$I_{SH_Ox} = \frac{R_{SHUNT}}{R_1} I_{LOAD} \qquad \text{(eq. 1)}$$

I_{SH_Ox} is also user defined and is not to exceed $I_{SH_O_MAX}$. Ideally, the SH_Ox current is around 2 mA. The resistance of R2 is found with the relationship;

$$R_2 = \frac{V_{SH_Ox}}{I_{SH_Ox}} \qquad \text{(eq. 2)}$$

Regardless of the values of I_{LOAD} or I_{SH_Ox}, the maximum voltage of the SH_Ox pin shall not exceed V_{SH_Ox}, indicated in the operating range table.

Bus Voltage Monitor (one of four identical instances)

An external voltage divider is used to scale the voltage on the BS_INx pin to an appropriate full−scale range for the differential output amplifier. Resistors R3 and R4 form a resistor divider to define the full dynamic range of the bus voltage monitor with;

$$\frac{R_4}{R_3 + R_4} \times V_{BUS} = V_{BS_INx} \qquad \text{(eq. 3)}$$

Multiplexer Select

The multiplier selection is controlled by a single digital input (MUX_SEL pin). The device will monitor this pin and cycle through the different measured parameters in a fixed sequence. The sequence will repeat cycle as shown in the tables until either a timeout condition is detected or the device is disabled. The MUX_SEL pin needs to be pulsed at least once before normal MUX_SEL cycles begin. The delay between the falling edge of the last initial MUX_SEL pulse and the first rising edge of the normal MUX_SEL cycle needs to be 14.75 μs > Td > 24.25 μs.

Operating Modes

There are two operating modes – stand−alone (one to four channels) and paired operation (up to eight channels). In paired operation, MODE_SEL is used to designate a "Device A" and "Device B" of a pair. When paired, the differential output amplifiers of the two devices are expected to be "wire−or'ed" together, and the table logic insures that only one device will actively drive DIFF_OUT_P and DIFF_OUT_N at any given time. See description in the Auxiliary Functions section for details. Additionally, devices can be configured to operate with a reduced channel count. See description in the Auxiliary Functions section for details.

Power−up Sequence

V_{BUS} voltages must be applied before V_{CC}. V_{CC} must be applied (2.8 V − 3.8 V) for expected operation and current consumption. The enable signal must be held low while the V_{CC} supply comes up. After both V_{BUS} and V_{CC} supplies are present, EN can then be pulled high or floated if standby mode or limited function mode is desired. Refer to auxiliary functions section for more information.

Four−Channel Stand−Alone Operation	
MUX_SEL Cycle	**Differential Amp Output**
Standby	Hi−Z
1	Channel 1 Bus Voltage
2	Channel 1 Shunt Current
3	Channel 2 Bus Voltage
4	Channel 2 Shunt Current
5	Channel 3 Bus Voltage
6	Channel 3 Shunt Current
7	Channel 4 Bus Voltage
8	Channel 4 Shunt Current
9→1	Channel 1 Bus Voltage
10→2	Channel 1 Shunt Current
….	Repeat cycle until reset or timeout

Six−Channel Paired Operation		
MUX_SEL Cycle	**Differential Amp Output (Device A)**	**Differential Amp Output (Device B)**
Standby	Hi−Z	Hi−Z
1	Ch 1 Bus Voltage	Hi−Z
2	Ch 1 Shunt Current	Hi−Z
3	Ch 2 Bus Voltage	Hi−Z
4	Ch 2 Shunt Current	Hi−Z
5	Ch 3 Bus Voltage	Hi−Z
6	Ch 3 Shunt Current	Hi−Z
7	Hi−Z	Ch 1 Bus Voltage
8	Hi−Z	Ch 1 Shunt Current
9	Hi−Z	Ch 2 Bus Voltage
10	Hi−Z	Ch 2 Shunt Current
11	Hi−Z	Ch 3 Bus Voltage
12	Hi−Z	Ch 3 Shunt Current
13→1	Ch 1 Bus Voltage	Hi−Z
14→2	Ch 1 Shunt Current	Hi−Z
….	Repeat cycle until reset or timeout	Repeat cycle until reset or timeout

APPLICATIONS DIAGRAMS

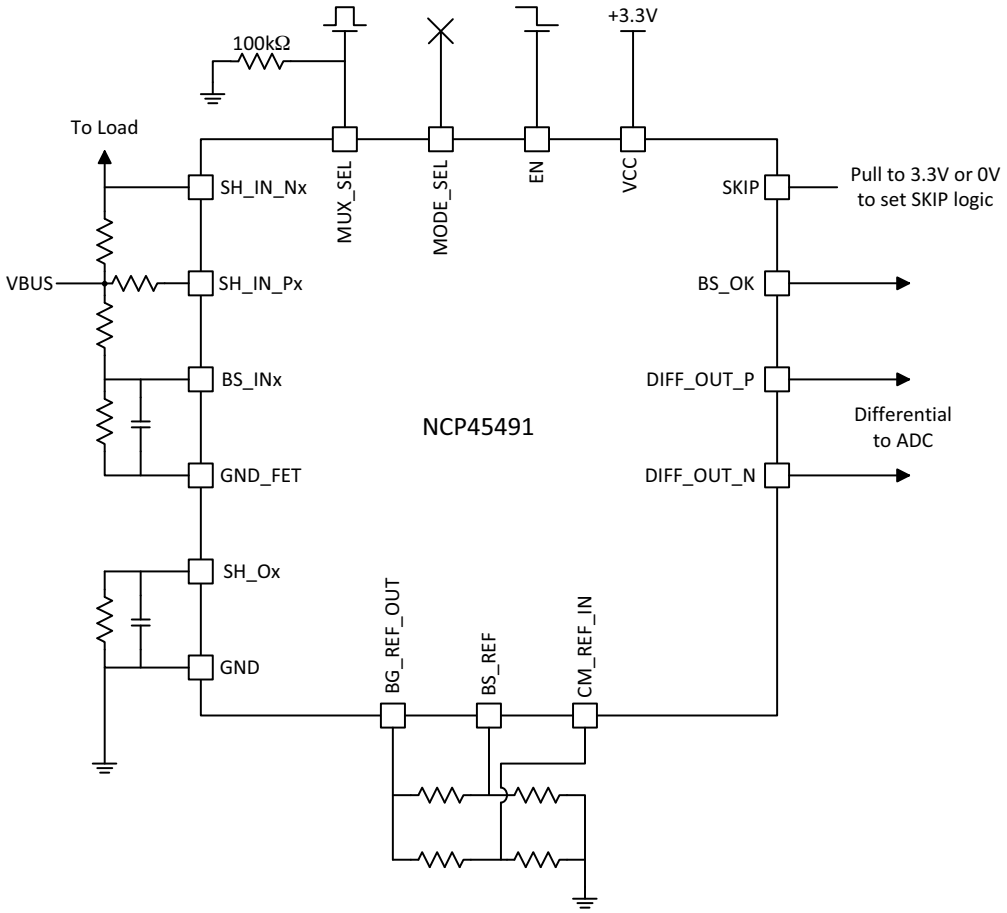


Figure 2. Stand Alone Device Operation

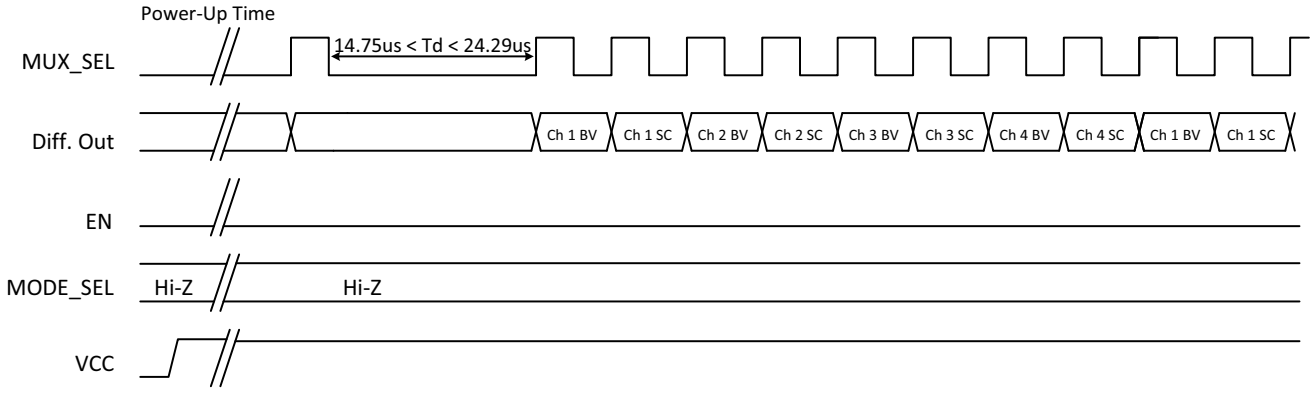


Figure 3. Stand Alone Timing Characteristics

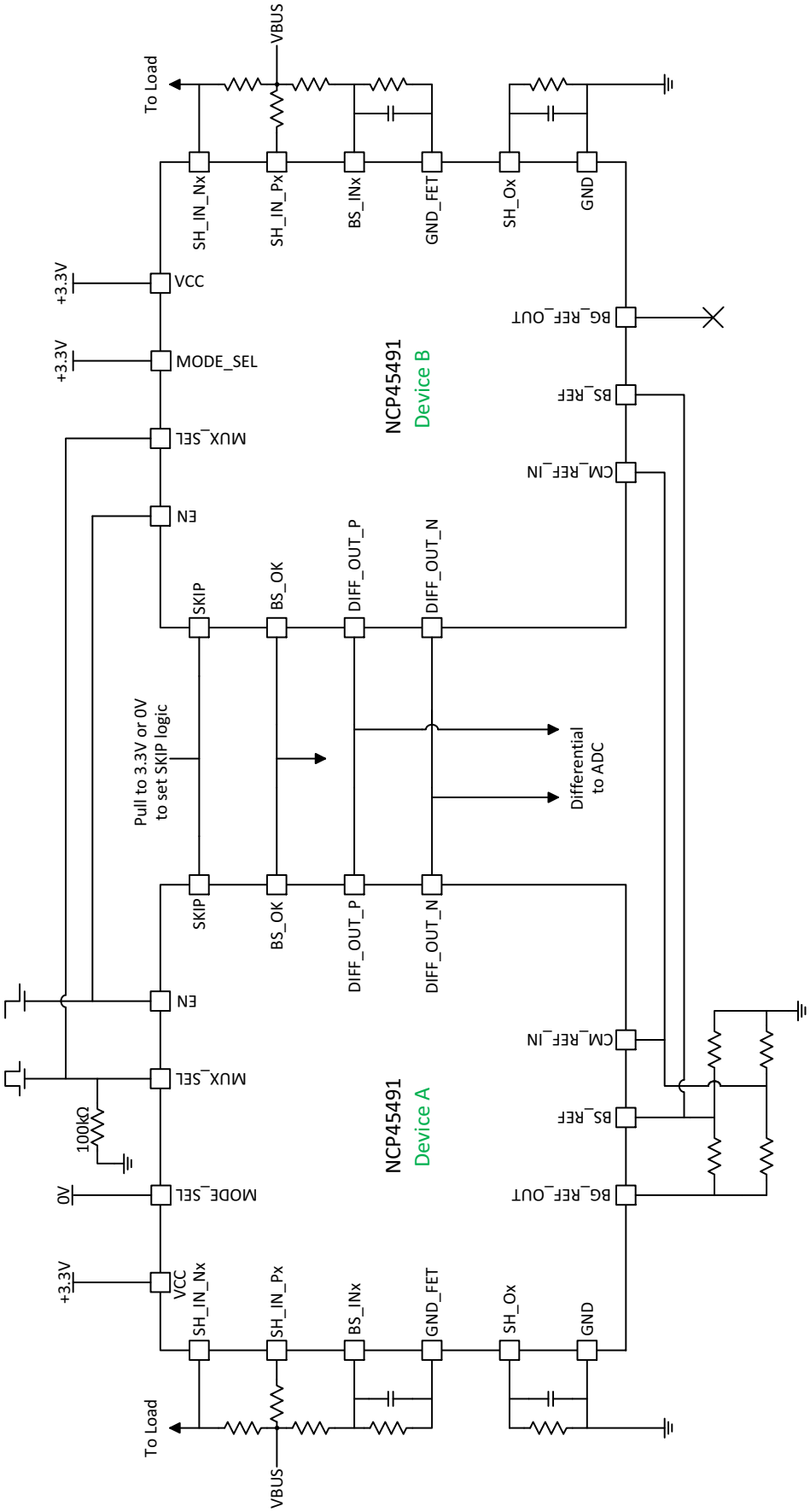


Figure 4. Six−Channel Paired Device Operation

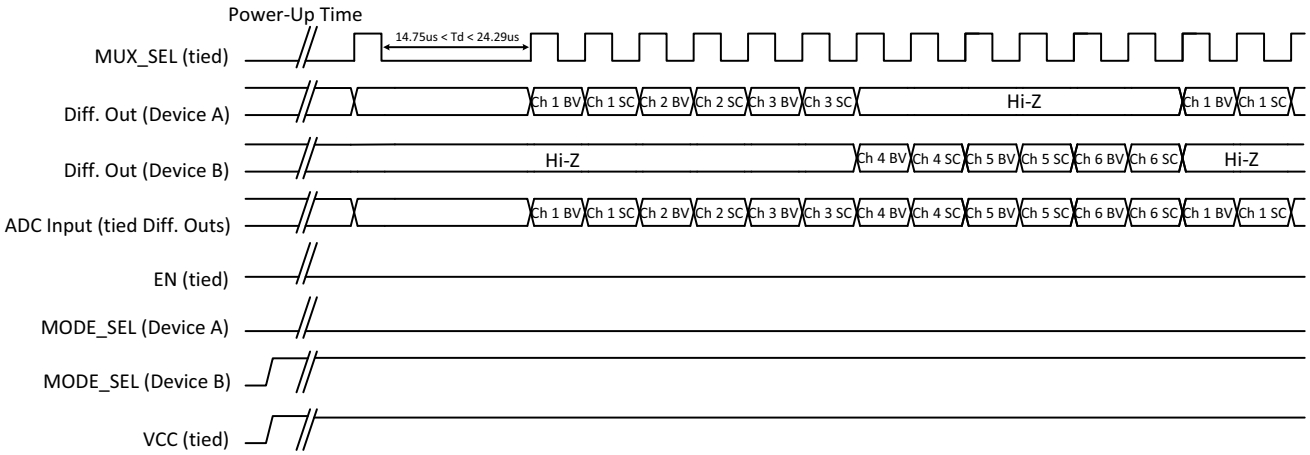


Figure 5. Six−Channel Paired Device Timing Characteristics

AUXILIARY FUNCTIONS

Bus Comparator (BS_OK)

A real−time indication that V_{CC} and all bus voltages (as measured on the BS_INx pins) are valid is provided on the BS_OK pin. BS_OK remains low until all used BS_INx pins are above a user−defined threshold voltage. The threshold voltage for the valid condition of BS_INx pins is set by the voltage provided to the BS_REF pin and must be less than 0.2 V. This can be done via an external resistor divider and the bandgap reference. If desired, the user can use the SKIP pin to modify the logic as shown in the corresponding table (H=high, L=low, Z=tristate, X=don't care). The SKIP pin can also be used to hold BS_OK = L in the absence of VCC.

Reset/Timeout

Normal operation can be interrupted and device returned to standby mode by holding the MUX_SEL pin HIGH or LOW longer than the reset period T_{RP}.

Bandgap Reference

The BG_REF_OUT pin provides a high−accuracy voltage from which BS_REF and CM_REF_IN voltages can be supplied via external voltage dividers.

Ground FET

The GND_FET pin is a switch that connects the bus voltage dividers to ground. In order that these voltage dividers not consume current when not needed (as in device shutdown), a low−impedance open−drain FET disconnects the low−side of these resistor dividers when the EN pin is at a logic HIGH level.

Enable Function

The EN pin controls device operation according to the corresponding table.

Mode Select Function

The MODE_SEL pin controls multiplexer operation according to the corresponding table. Note that MODE_SEL is left floating in stand−alone operation.

Reduced Channel Count

If an application requires less than 4 channels, then pins for unused channels must be connected in the following manner for correct operation of the BS_OK output.

PINS for Unused Channels	Connection
BS_INx	Connect to BS_IN pin of previous channel
SH_Ox	Float
SH_IN_Px	Connect to VCC voltage or higher
SH_IN_Nx	Connect to VCC voltage or higher

Note: "x" refers to the unused channel number

Connecting the SH_IN_Px and SH_IN_Nx pins for unused channels to the respective SH_IN_Px and SH_IN_Nx of previous active channels is an acceptable way to provide the bias voltages needed. If the SH_Ox pin is left floating, then that channel and all subsequent channels will be skipped in the DIFF_OUT readout. For example, if SH_O3 is left floating, SH_O3 and SH_O4 will be bypassed. If devices are in paired mode, the number of unused channels on both devices must be matched. However, bus voltage on those unused channels (as measured on the BS_INx pins) will still be compared to the BS_REF voltage and included in the BS_OK output logic. If SKIP = 0 V, then the BS_INx voltages are ignored. In this case the unused BS_INx pins can be tied to any voltage less than VCC.

SKIP Logic				
EN	VCC	BS_INx	SKIP	BS_OK
X	Z(unpowered)	X	H	L
X	L (POR)	X	X	L
H	X	X	X	L
Z/L	H	L	H	L
Z/L	H	H	H	H (open drain)
Z/L	H	X	L	H (open drain)

EN Logic	
Level	Device Operation
LOW	Fully Functional
Tri−state (floating)	Limited Function: BG_REF_OUT is valid, GND_FET is turned ON, BS_OK comparators and output are functional. All other functions to be disabled. DIFF_OUT to be Hi−Z and multiplexer select logic is held in reset.
HIGH	Standby: As described in Limited Function above with GND_FET turned OFF

MODE_SEL Logic	
Level	Multiplexer Operation
LOW	Device A
Tri−state (floating)	Stand−Alone
HIGH	Device B

LAYOUT GUIDELINES

Electrical Layout Considerations

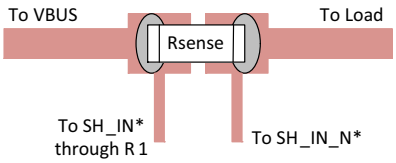
Correct physical layout is important for proper low noise accurate operation of the NCP45491.

Power Paths: Use wide and short traces for bus voltage source to load path to reduce parasitic resistance and loss of power through the primary current path. The load current (traveling from source to load through Rshunt) does not pass through the NCP45491, but careful consideration of this path is critical.

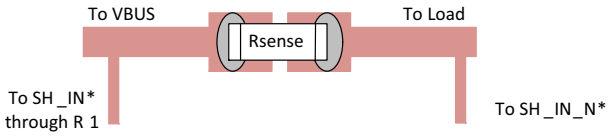
Power Supply Decoupling: A decoupling capacitor of 0.1 μF from VCC to ground is recommended. Keep capacitor as close to the NCP45491 VCC pin as possible, with a direct connection to the GND pad.

Rshunt layout: A correct 4−wire Kelvin connection to the Rshunt resistor (also commonly known as the Rsense resistor) is critical to achieving accurate bus current and voltage measurements. The Rshunt resistor should have a low tolerance specification with adequate power ratings depending on the application. Any shared traces between the force and sense connections to the Rshunt resistor will result in additional un−accounted for resistance in the mΩ that will add error to the bus current and voltage measurements. The figure below demonstrates correct Rshunt connection.

Correct layout:



Incorrect layout:



Ground: A solid connection to the back ground pad of the NCP45491 to a ground plane will help to reduce noise, in addition to the decoupling capacitor. Using the ground plane to shield sensitive analog signals is good practice.

Differential Output: To achieve a low noise result, the DIFF_OUT_P and the DIFF_OUT_N should be routed close together with matched lengths. Shielding these lines with GND will provide additional protection from noise. Minimizing the distance traveled by the differential output pair to get to the digitizing ADC is also a good way to avoid additional noise. The DIFF_OUT_x signals should not be routed in close proximity to other digital signals in the system application.

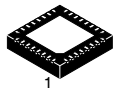
Routing of Digital Signals: MUX_SEL, MODE_SEL, SKIP, and ENABLE should be routed to avoid direct coupling with any of the analog input and output signals of the NCP45491. In most applications, these digital signals are static and are of lesser concern.

References: Connections to BS_REF, BG_REF_OUT, and CM_REF_IN should be kept close to the NCP45491 for best noise performance.

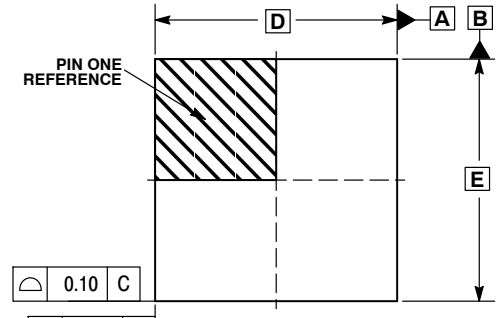
Thermal Layout Considerations: As the load current does not flow through the NCP45491, thermal dissipation is of minimal concern. Connecting the GND pad on the back of the part to a ground plane is ample. Selection of R1, R2, R3, R4, and Rshunt may require higher power ratings above the 0.1W standard for small SMD passives.

QFN32 4x4, 0.4P
CASE 485CD
ISSUE A

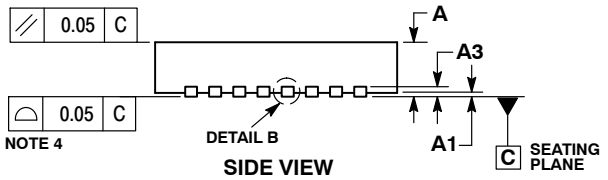
DATE 09 OCT 2012



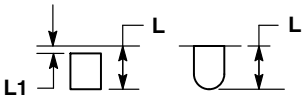
SCALE 2:1



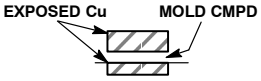
TOP VIEW



SIDE VIEW



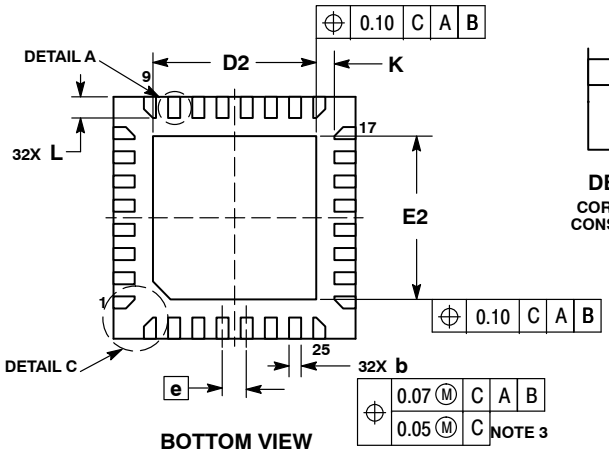
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



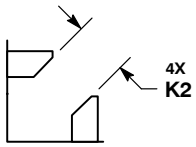
DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	4.00 BSC	
D2	2.60	2.80
E	4.00 BSC	
E2	2.60	2.80
e	0.40 BSC	
K	0.30 REF	
K2	0.45 REF	
L	0.25	0.45
L1	---	0.15



BOTTOM VIEW



DETAIL C
CORNER LEAD CONSTRUCTION

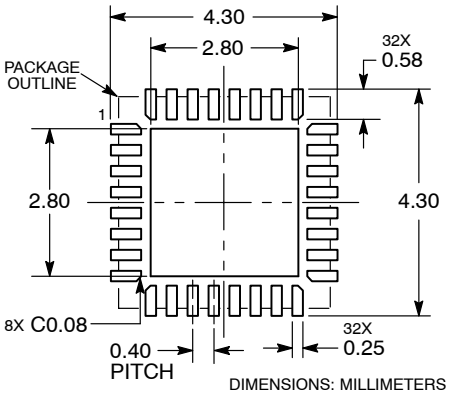
GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	QFN32 4X4, 0.4P	PAGE 1 OF 1

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