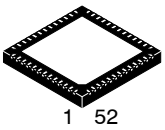
Dual Output 3 & 2 Phase Controller with Single Intel Proprietary Interface for Desktop and Notebook CPU Applications

NCP81243



QFN52
MN SUFFIX
CASE 485BE

The NCP81243 dual output three plus two phase buck solutions are optimized for Intel®'s IMVP8 CPUs. The NCP81243 offer five PWM drive signals that can be configured in multiple setups. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for both desktop and notebook applications.

The control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing an ultra fast initial response to dynamic load events and reduced system cost. The NCP81243 provides the mechanism to shed phases during light load operation and can auto frequency scale in light load conditions while maintaining excellent transient performance.

Dual high performance operational error amplifiers are provided to simplify compensation of the complete system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.

Features

- Meets Intel's IMVP8 Specification
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- DAC with Droop Feed−forward Injection
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- "Lossless" DCR Current Sensing for Current Balancing
- Summed Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 300 kHz – 1.4 MHz
- Startup into Pre−Charged Loads while Avoiding False OVP
- Pin Programmable Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Desktop & Notebook Processors
- Gaming

MARKING DIAGRAM

NCP81243 = Specific Device Code
F = Wafer Fab
A = Assembly Site
WL = Lot ID
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81243MNTXG	QFN52 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

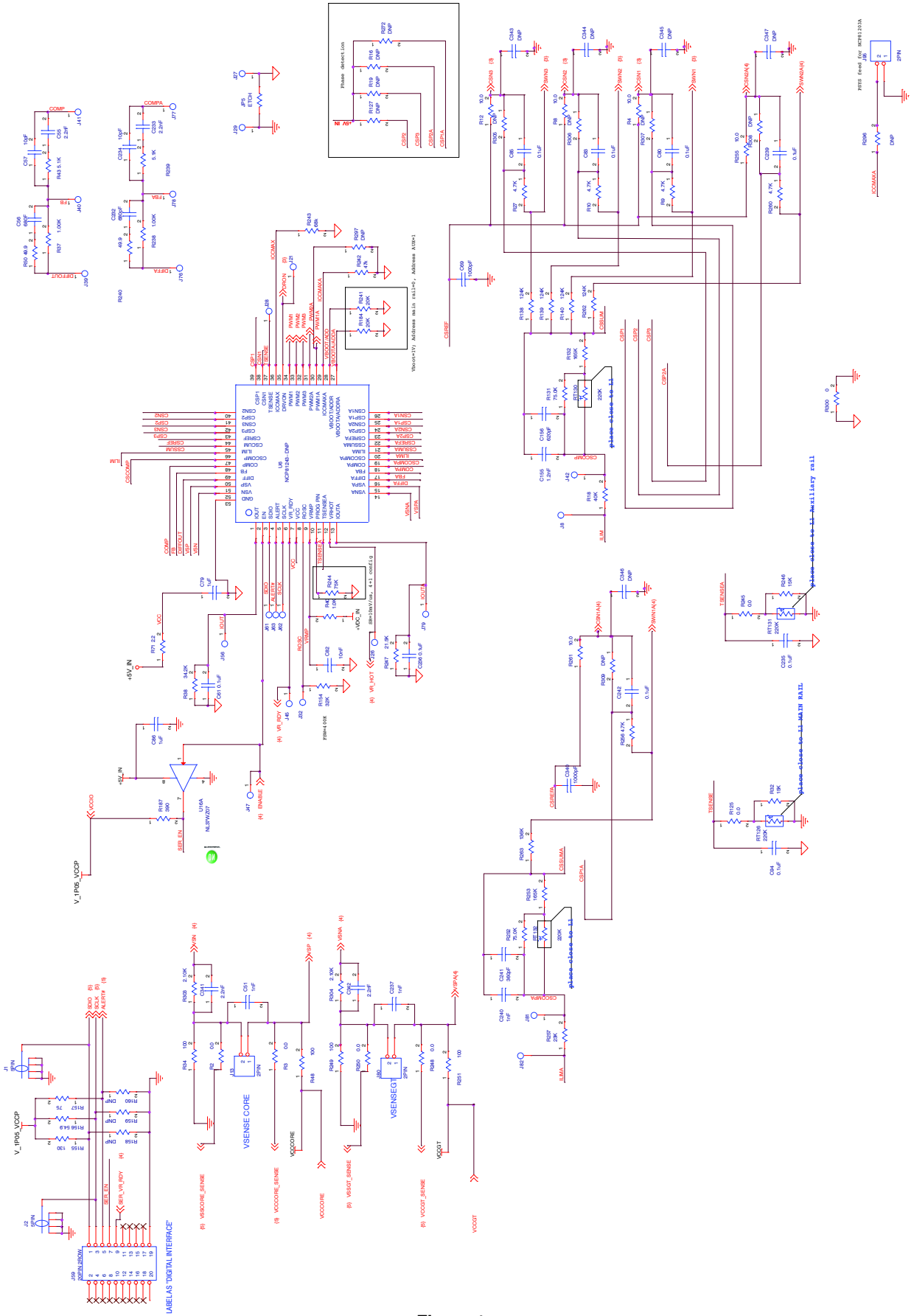


Figure 1.

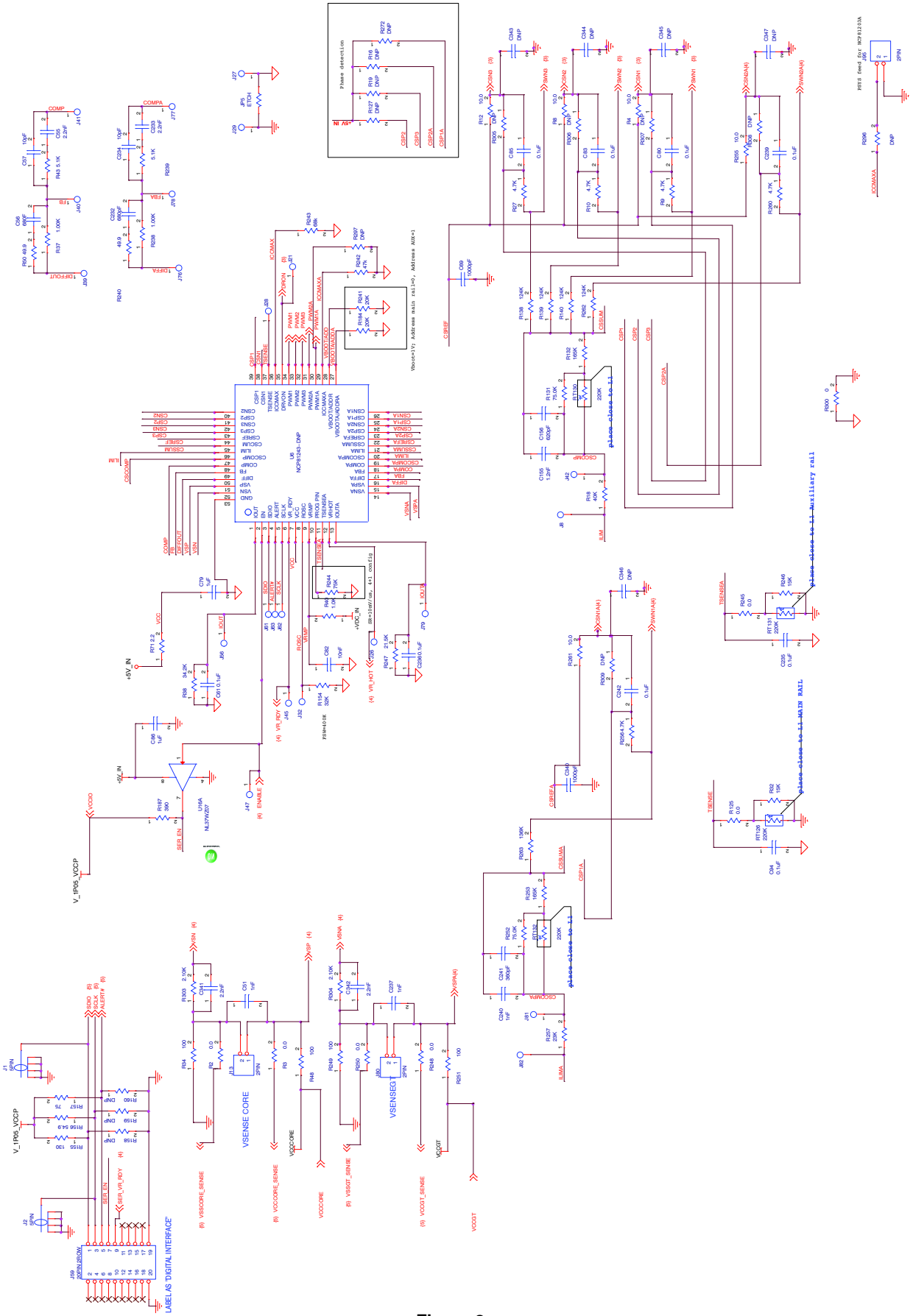


Figure 2.

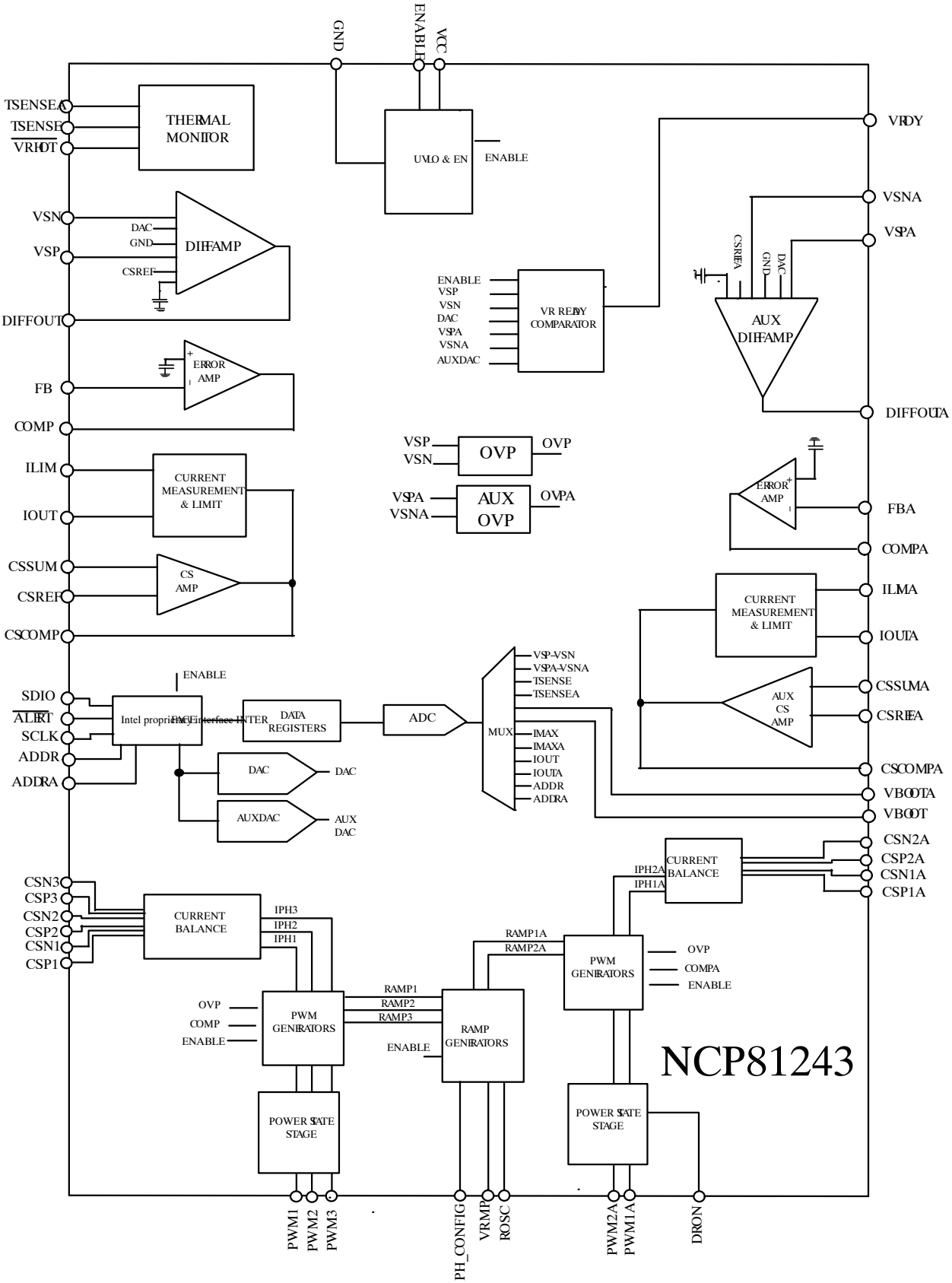


Figure 3. 3 + 2 Block Diagram

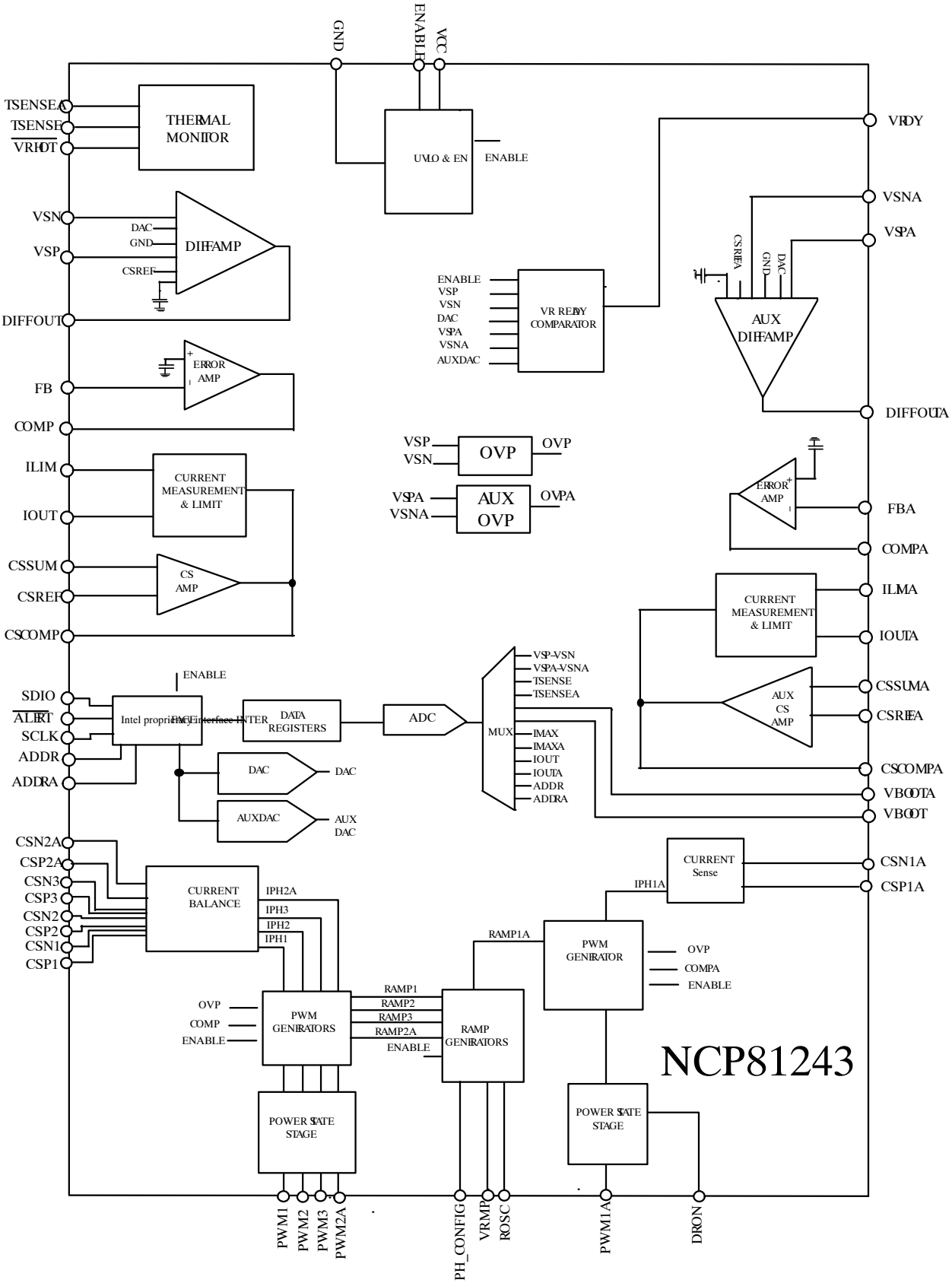


Figure 4. 4 + 1 Block Diagram

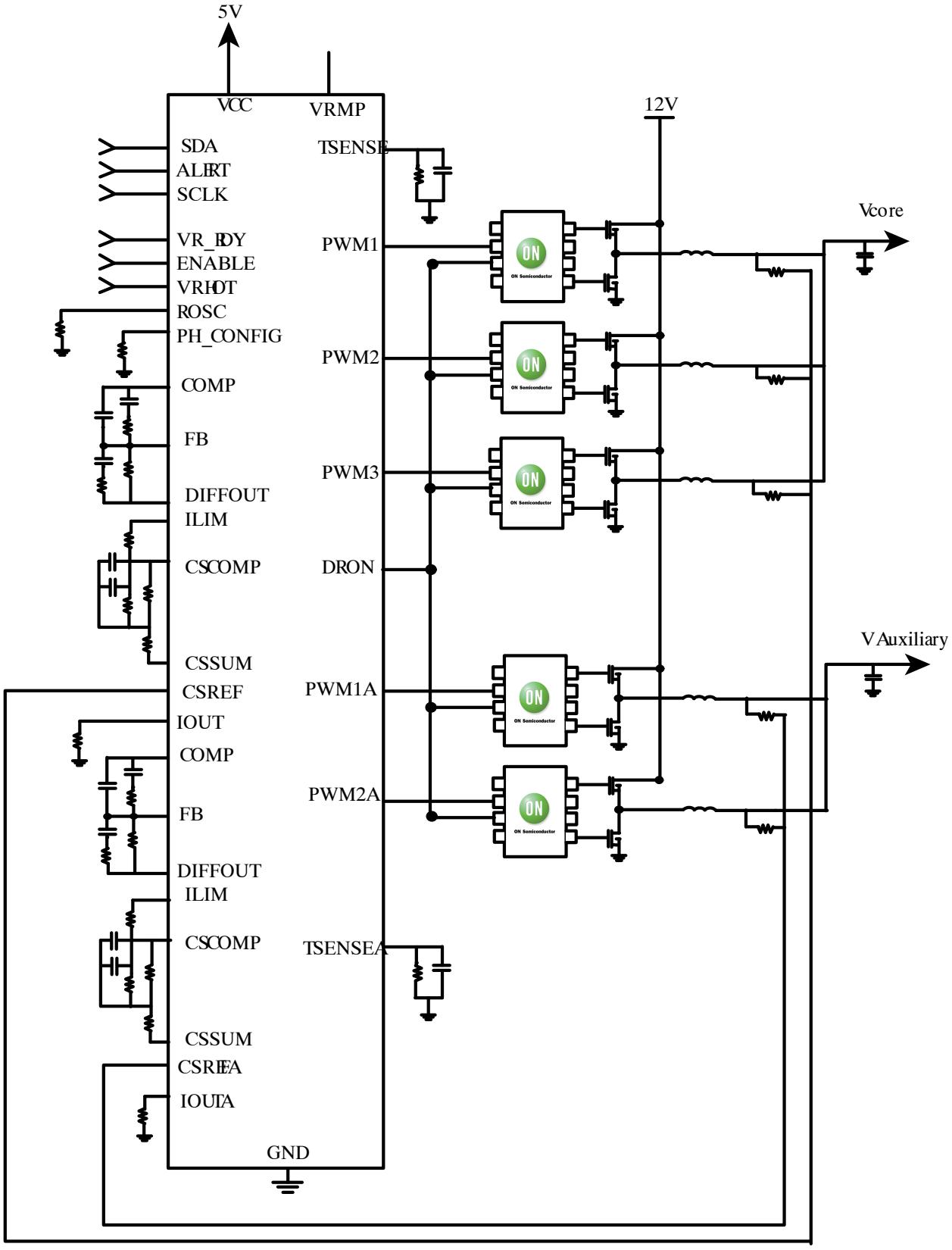


Figure 5. Pinout

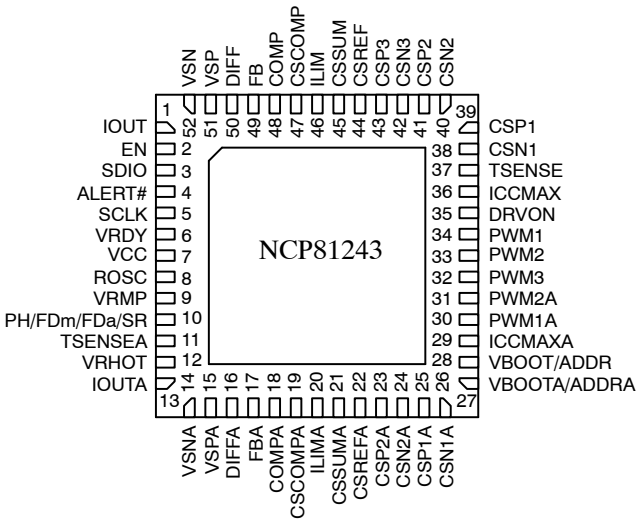


Figure 6.

Table 1. QFN52 PIN LIST DESCRIPTION

Symbol	Pin No.	Description
IOUT	1	Total output current for Main Rail.
EN	2	Logic input. Logic high enables both rail output and logic low disables both rail output.
SDIO	3	Serial VID data interface
ALERT#	4	Serial VID ALERT#.
SCLK	5	Serial VID clock
VRDY	6	Open drain output. High output on this pin indicates that the Main Rail output is regulating.
VCC	7	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground.
ROSC	8	A resistor to ground on this pin will set the oscillator frequency
VRMP	9	Feed−forward input of Vin for the ramp slope compensation. The current fed into this pin is used to control of the ramp of PWM slope
PH/FDm/FDa/SR	10	A resistor to ground on startup is used to set the phase configuration per rail of the NCP81243 as well as the Fast slew rate
TSenseA	11	Temp Sense input for Auxiliary rail
VR_HOT	12	Open drain output. Signals an over temperature event has occurred
IOUTA	13	Total output current for the Auxiliary rail.
VSNA	14	Differential Output Voltage Sense Negative for auxiliary rail
VSPA	15	Differential Output Voltage Sense Positive for auxiliary rail
DIFFA	16	Output of the auxiliary rail differential remote sense amplifier.
FBA	17	Error amplifier voltage feedback for auxiliary rail output
COMPA	18	Output of the error amplifier and the inverting inputs of the PWM comparators for the auxiliary rail output.
CSCOMPA	19	Output of total current sense amplifier for auxiliary rail output.
ILIMA	20	Over current shutdown threshold setting for auxiliary rail I output. Resistor to CSCOMP to set threshold.
CSSUMA	21	Inverting input of total current sense amplifier for auxiliary rail output.
CSREFA	22	Total output current sense amplifier reference voltage input for auxiliary rail
CSP2A	23	Non−inverting input to current balance sense amplifier for phase 2 A
CSN2A	24	Inverting input to current balance sense amplifier for phase 2 A
CSP1A	25	Non−inverting input to current balance sense amplifier for phase 1 A
CSN1A	26	Inverting input to current balance sense amplifier for phase 1 A

Table 1. QFN52 PIN LIST DESCRIPTION

Symbol	Pin No.	Description
VBOOTA/ADDRA	27	VBOOT and Address AUX rail Input Pin. A resistor to ground on startup is used to VBOOT and address of the auxiliary rail
VBOOT/ADDR	28	VBOOT and Address main rail Input Pin. A resistor to ground on startup is used to VBOOT and address of the main rail
ICCMAXA	29	ICCMAX Input for auxiliary rail Pin. During start up it is used to program configuration of Internal register with a resistor to ground
PWM1A	30	PWM 1 Auxiliary rail output.
PWM1A	30	PWM 1 Auxiliary rail output. ICCMAX Input for auxiliary rail Pin.
PWM2A	31	PWM 2 Auxiliary rail output.
PWM3	32	PWM 3 Main rail output.
PWM2	33	PWM 2 Main rail output.
PWM1	34	PWM 1 Main output.
DRVON	35	Bidirectional gate driver enable for external drivers for both Main and Auxiliary Rails. It should be left floating if unused.
ICCMAX	36	ICCMAX Main rail Input Pin. During start up it is used to program configuration of Internal register with a resistor to ground
Tsense	37	Temp Sense input for main rail
CSN1	38	Non−inverting input to current balance sense amplifier for Main Rail phase 1
CSP1	39	Non−inverting input to current balance sense amplifier for Main Rail phase 1
CSN2	40	Non−inverting input to current balance sense amplifier for Main rail phase 2
CSP2	41	Non−inverting input to current balance sense amplifier for Main Rail phase 2
CSN3	42	Non−inverting input to current balance sense amplifier for Main Rail phase 2
CSP3	43	Non−inverting input to current balance sense amplifier for Main Rail phase 2
CSREF	44	Total output current sense amplifier reference voltage input for Main Rail
CSSUM	45	Inverting input of total current sense amplifier for Main Rail output
ILIM	46	Over current shutdown threshold setting for Main Rail output. Resistor to CSCOMP to set threshold.
CSCOMP	47	Output of total current sense amplifier for Main Rail output
COMP	48	Output of the Main Rail error amplifier and the inverting input of the PWM comparator for Main Rail output
FB	49	Error amplifier voltage feedback for Main Rail output
DIFF	50	Output of the Main Rail differential remote sense amplifier.
VSP	51	Differential Output Voltage Sense Positive for mail rail
VSN	52	Differential Output Voltage Sense Negative for main rail
AGND	53	

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP,COMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP, CSCOMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
DIFF, DIFFA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWM1, PWM2, PWM3, PWM1A, PWM2A	VCC + 0.3 V	−0.3 V		
VSN, VSNA	GND + 300 mV	GND−300 mV	1 mA	1 mA
VRDY	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VCC	6.5 V	−0.3 V		
VRMP	+25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to GND unless noted otherwise.

Symbol	Description	Value	Unit
R_{JA}	Thermal Characteristic QFN Package (Note 1)	68	°C/W
T_J	Operating Junction Temperature Range (Note 2)	−40 to +125	°C
	Operating Ambient Temperature Range	−40 to +100	°C
T_{STG}	Maximum Storage Temperature Range	−40 to +150	°C
MSL	Moisture Sensitivity Level QFN Package	1	

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 3. NCP81243 (3+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current		−400		400	nA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 0.75 V − 1.52 V, CL = 20 pF to GND, DC Load = 10 k to GND		20		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	–	–	V
Minimum Output Voltage	I_{SINK} = 0.5 mA	–	–	1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−400	–	400	nA
VSP Input Voltage Range		−0.3	–	3.0	V
VSN Input Voltage Range		−0.3	–	0.3	V
−3 dB Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		12		MHz
Closed Loop DC gain VS to DIFF	VS+ to VS− = 0.5 to 1.3 V		1.0		V/V
Droop Accuracy	CSREF−DROOP = 80 mV DAC = 0.8 V to 1.2 V	−82		−78	mV
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.0	–	–	V
Minimum Output Voltage	I_{SINK} = 0.5 mA	–	–	0.5	V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		−500		500	μV
Input Bias Current	CSSUM = CSREF = 1 V	−7.5		7.5	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 KΩ to GND		10		MHz
Maximum CSCOMP (A) Output Voltage	Isource = 2 mA	3.5	–	–	V
Minimum CSCOMP(A) Output Voltage	Isink = 500 μA	–	–	0.1	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSPX = CSNX = 1.2 V	−50	–	50	nA
Common Mode Input Voltage Range	CSPx = CSNx	0	–	2.0	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−100	–	100	mV
Closed loop Input Offset Voltage Matching	CSPx = 1.2 V, Measured from the average	−2	–	2	mV
Current Sense Amplifier Gain	0 V < CSPx < 0.1 V	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSNX = CSPX = 10 mV to 30 mV	−4.5		4.5	%
−3 dB Bandwidth	Guaranteed by simulation		8		MHz
BIAS SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	PS0			50	mA
VCC Quiescent Current	PS1			50	mA

Table 3. NCP81243 (3+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Quiescent Current	PS2			50	mA
VCC Quiescent Current	PS3		20		mA
VCC Quiescent Current	PS4 (25°C only)		230		μA
VCC Quiescent Current	Enable low			45	μA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			
VCC UVLO Hysteresis			200		mV
VRMP					
Supply Range		4.5		20	V
UVLO Threshold	VRMP rising			4.2	V
	VRMP falling	3			
VCC UVLO Hysteresis			700		mV
DAC SLEW RATE					
Soft Start Slew Rate			1/2 SR Fast		mv/μs
Slew Rate Slow			1/2 SR Fast		mv/μs
Slew Rate Fast			>10		mv/μs
AUX Soft Start Slew Rate			1/2 SR Fast		mv/μs
AUX Slew Rate Slow			1/2 SR Fast		mv/μs
AUX Slew Rate Fast			>10		mv/μs
ENABLE INPUT					
Enable High Input Leakage Current	Enable = 0	−1	0	1.0	μA
Upper Threshold	V_{UPPER}	0.8			V
Lower Threshold	V_{LOWER}			0.3	V
Enable Delay Time	Measure time from Enable transitioning HI, VBOOT is not 0 V			2.5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0	–	–	V
Output Low Voltage	Sinking 500 μA	–	–	0.1	V
Pull Up Resistances			2.0		kΩ
Rise/Fall Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%	–	160		ns
Internal Pull Down Resistance	VCC = 0 V		70		kΩ
IOUT /IOUTA OUTPUT					
Input Referred Offset Voltage	I_{limit} to CSREF	−3		+3	mV
Output current max	Ilimit sink current 80 μA	–	–	800	μA
Current Gain	(Iout current)/(Ilimit Current) Rlim = 20 K, Riout = 5 K DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	
OSCILLATOR					
Switching Frequency Range		300	–	1400	KHz
Switching Frequency Accuracy	300 KHz < Fsw < 1.4 MHz	−10	–	10	%
3 Phase Operation		350	390	430	kHz
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start			2.5		V

Table 3. NCP81243 (3+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold Above DAC	VSS rising	375	400	425	mV
Over Voltage Delay	VSS rising to PWMx low		50		ns
Under Voltage Threshold Below DAC−DROOP	VSS falling	275	300	325	mV
Under−voltage Hysteresis	VSS rising		25		mV
Under−Voltage Delay			5		μS
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shutdown after 50 us delay)	Main Rail, Rlim = 20 kΩ	8.0	10	12	μA
ILIM Threshold Current (immediate OCP shutdown)	Main Rail, Rlim = 20 k	13	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	Main Rail, RLIM = 20 K (N = number of phases in PS0 mode)		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	Main Rail, RLIM = 20 K (N= number of phases in PS0 mode)		15/N		μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	Auxiliary Rail, Rlim = 20 k	8.0	10	11	μA
ILIM Threshold Current (immediate OCP shutdown)	Auxiliary Rail, Rlim = 20 k	13	15	16.5	μA
ILIM Threshold Current (OCP shutdown after 50 μs delay)	Auxiliary Rail RLIM = 20 K		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	Auxiliary Rail, RLIM = 20 K		15/N		μA
MODULATORS (PWM COMPARATORS) FOR MAIN RAIL & AUXILIARY RAIL					
Minimum Pulse Width	Fsw = 350 KHz		60		ns
0% Duty Cycle	COMP voltage when the PWM outputs remain LO		1.3	–	V
100% Duty Cycle	COMP voltage when the PWM outputs remain HI VRMP = 12.0 V	–	2.5	–	V
PWM Ramp Duty Cycle Matching	COMP = 2 V, PWM Ton matching		1		%
PWM Phase Angle Error	Between adjacent phases		±5		deg
Ramp Feed−forward Voltage range		4.5		20	V
TSENSE/TSENSEA					
VRHOT Assert Threshold			440		mV
VRHOT Rising Threshold			460		mV
Alert Rising Threshold			480		mV
Alert Assertion Threshold			460		mV
TSENSE Bias Current		−57.5	−60	−62.5	μA
VRHOT					
Output Low Voltage				0.3	V
Output Leakage Current	High Impedance State	−1.0	–	1.0	μA
ADC					
Voltage Range		0		2	V
Total Unadjusted Error (TUE)		−1.25		+1.25	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			±1		%
Conversion Time			30		μs

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Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC					
Round Robin			90		μs
VRDY OUTPUT					
Output Low Saturation Voltage	$I_{VDD(A)\_VRDY}$ = 4 mA	–	–	0.3	V
Rise Time	External pull−up of 1KΩ to 3.3V, C_{TOT} = 45 pF, ΔVo = 10% to 90%			150	ns
Fall Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%			150	ns
Output Voltage at Power−up	VRDY pulled up to 5 V via 2 KΩ enable low	–	–	0.1	V
Output Leakage Current When High	VRDY = 5.0 V	−1.0	–	1.0	μA
VRDY Delay (falling)	From OCP	–	50	–	μs
	From OVP		300		ns
PWM (A), OUTPUTS					
Output High Voltage	Sourcing 500 μA	VCC − 0.2V	–	–	V
Output Mid Voltage	No load	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo =10% to 90% of VCC	–	10		ns
Tri−State Output Leakage	Gx = 2.0V, x = 1−2, EN=Low	−1.0	–	1.0	μA
PHASE DETECTION					
CSP2, CSP3, CSP1A, CSP2A Pin Threshold Voltage		4.7			V
Phase Detect Timer			100		μs

3. Guaranteed by design or characterization. Not in production testing

Table 4. STATE TRUTH TABLE

STATE	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	DRON PIN	Method of Reset
POR 0<VCC<UVLO	N/A	N/A	N/A	Resistive pull down	
Disabled EN < threshold UVLO >threshold	Low	Low	Disabled	Low	
Start up Delay & Calibration EN> threshold UVLO>threshold	Low	Low	Disabled	Low	
DRON Fault EN> threshold UVLO>threshold DRON<threshold	Low	Low	Disabled	Resistive pull up	Driver must release DRON to high
Soft Start EN > threshold UVLO >threshold DRON > High	Low	Operational	Active / No latch	High	
Normal Operation EN > threshold UVLO >threshold DRON > High	High	Operational	Active / Latching	High	N/A
Over Voltage	Low	N/A	DAC+OVP	High	
Over Current	Low	Operational	Last DAC Code	Low	
V_{OUT} = 0 V	Low: if Reg34h:bit0=0; High:if Reg34h:bit0=1;	Clamped at 0.9 V	Disabled	High, PWM outputs in low state	

General

The NCP81243 is a dual rail three plus two phase dual edge modulated multiphase PWM controller, with a single serial Intel proprietary interface control interface.

Ultrasonic Mode:

The Switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible frequency range.

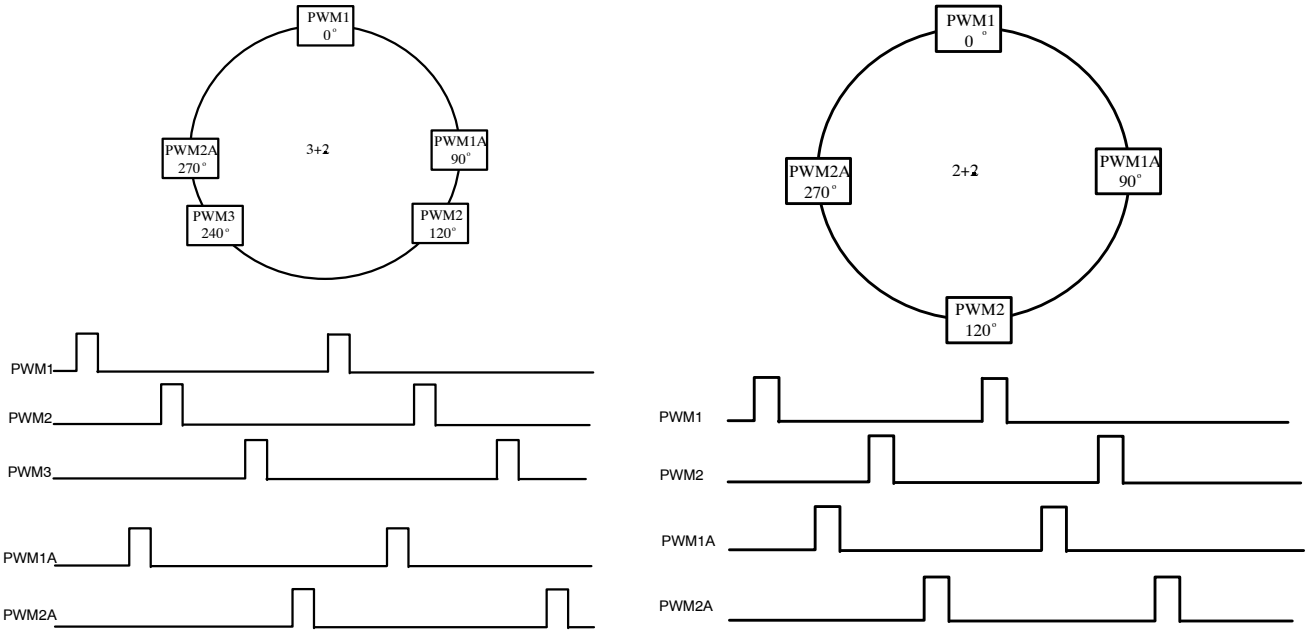
Phase Configuration:

The NCP81243 has 5 external PWM signals which can be configured across the two rail. A resistor to ground on pin10, is used to configure Phase configuration, Frequency double on main/Auxiliary rail and SR. Available configuration options from pin10 are shown below:

Table 5. PHASE CONFIGURATION SELECTION

Resistor	LEVEL	PH_config	BOOST Main Rail	BOOST AUX Rail	SR
10000	1	3+2	NO	NO	10
13000	2	3+2	NO	NO	30
16000	3	3+2	NO	NO	10
19200	4	3+2	NO	NO	30
22500	5	3+2	NO	YES(*2)	10
26000	6	3+2	NO	YES(*2)	30
29600	7	3+2	NO	YES(*2)	10
33500	8	3+2	NO	YES(*2)	30
37400	9	3+2	YES(*2)	NO	10
41500	10	3+2	YES(*2)	NO	30
45800	11	3+2	YES(*2)	NO	10
50200	12	3+2	YES(*2)	NO	30
54800	13	3+2	YES(*2)	YES(*2)	10
59500	14	3+2	YES(*2)	YES(*2)	30
64500	15	3+2	YES(*2)	YES(*2)	10
69600	16	3+2	YES(*2)	YES(*2)	30
75000	17	4+1	NO	NO	10
80600	18	4+1	NO	NO	30
86500	19	4+1	NO	NO	10
92600	20	4+1	NO	NO	30
99000	21	4+1	NO	YES(*2)	10
105500	22	4+1	NO	YES(*2)	30
112500	23	4+1	NO	YES(*2)	10
119600	24	4+1	NO	YES(*2)	30
127000	25	4+1	YES (*1.5)	NO	10
134800	26	4+1	YES(*1.5)	NO	30
143000	27	4+1	YES(*1.5)	NO	10
151400	28	4+1	YES(*1.5)	NO	30
160300	29	4+1	YES(*1.5)	YES(*2)	10
169500	30	4+1	YES(*1.5)	YES(*2)	30
180000	31	4+1	YES(*1.5)	YES(*2)	10
210000	32	4+1	YES(*1.5)	YES(*2)	30

PHASE INTERLEAVING



Serial VID Interface (Intel proprietary interface)

Information regarding Intel proprietary interface can be obtained from Intel.

VBOOT and Intel proprietary interface Address Programming

The NCP81243 has a VBOOT voltage register that can be externally programmed for both core and Auxiliary boot−up output voltages. The VBOOT voltage for main and auxiliary rails can be programmed with a resistor from VBOOT and VBOOTA pin to GND. In addition to VBOOT level, pin 28 and pin 29 also support Intel proprietary interface bus address programming. The NCP81243 support multiple Intel proprietary interface Device Addresses per rail. Pin 28 (VBOOT/ADDR) is used to set the address for the main rail, pin 29 (VBOOTA/ADDRA) is used to address the Auxiliary rail. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. Table 6 shows the resistor values that should be used and the corresponding Intel proprietary interface and VBOOT options for each rail.

Pin 28 (VBOOT/ADDR) Resistor	LEVEL	VBOOT	Address	Auto Phase Shedding Disabling
10000	1	0	**0**	No
15000	2	0	**0**	Yes
21000	3	1.2	**0**	no
26700	4	0.9	**0**	No
33200	5	0	**1**	No
41200	6	0	**1**	Yes
49900	7	1.2	**1**	No
60400	8	0.9	**1**	No
71500	9	0	**2**	No
84500	10	0	**2**	Yes
97600	11	1.2	**2**	No
115000	12	1.5	**2**	No
133000	13	0	**4**	No
154000	14	0	**4**	Yes
178000	15	1.2	**4**	No
210000	16	1.5	**4**	No

Table 6. VBOOT, ADDRESS PROGRAMMABILITY MAIN AND AUX RAILS

Pin 27 (VBOOTA/ADDRA) Resistor	LEVEL	VBOOT AUX	Address AUX
10000	1	0	**1**
13000	2	1.05	**1**
15800	3	1.2	**1**
20000	4	0.9	**1**
23700	5	0	**0**
28000	6	1.05	**0**
33200	7	1.2	**0**
38300	8	0.9	**0**
45000	9	0	**2**
52300	10	1.05	**2**
60400	11	1.2	**2**
69800	12	1.5	**2**
80600	13	0	**3**
93100	14	1.05	**3**
107000	15	1.2	**3**
121000	16	1.5	**3**
137000	17	0.8	**2**
158000	18	0.95	**2**
180000	19	0.8	**3**
210000	20	0.95	**3**

Remote Sense Amplifier

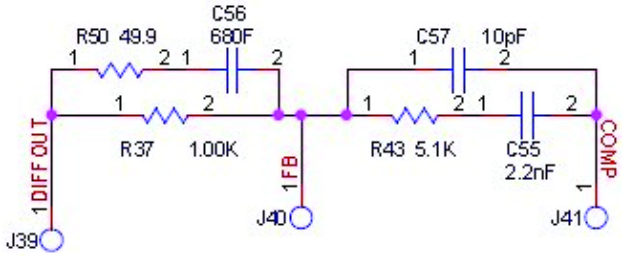
A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to V_{DIFOUT} =

$$\left(V_{VSP} - V_{VSN}\right) + \left(1.3\ V - V_{DAC}\right) + \left(V_{DROOP} - V_{CSREF}\right)$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

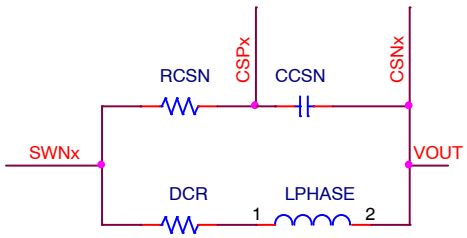
High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type III compensation circuit is normally used to compensate the system.



Differential Current Feedback Amplifiers

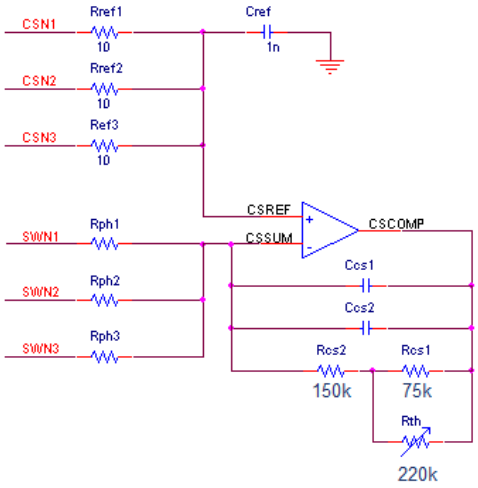
Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5 kΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \cdot DCR}$$

Total Current Sense Amplifier

The NCP81243 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.



The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{Total} \cdot DCR\right)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 220k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2 \cdot PI \cdot L_{Phase}}$$

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP−CSREF voltage as shown below.

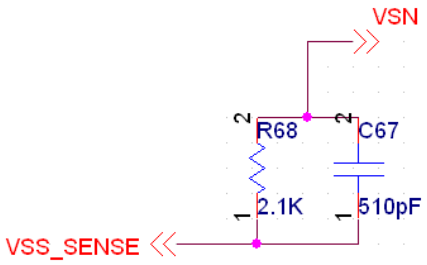
$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{LIMIT} \cdot DCR\right) \over 10\ \mu$$

or

$$R_{LIMIT} = \frac{V_{CSCOMP-CSREF\ @\ ILIMIT}}{10\ \mu}$$

Programming DAC Feed−Forward Filter

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.



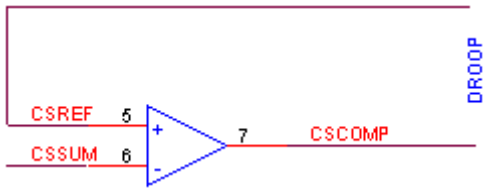
$$Rvsn = Cout \cdot Rout \cdot 453.6 \cdot 10^6$$

$$Cvsn = \frac{Rout \cdot Cout}{Rvsn}$$

Programming DROOP

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to the load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transient faster than those to which the regulation loop can respond. With the NCP81243 and projects the loadline is produced by adding a signal proportional to output load current (Vdroop) to the output voltage feedback signal− thereby satisfying the voltage regulator at an output voltage reduced proportional to load current.

The loadline is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



Droop = DCR * (R_{CS} / R_{ph})

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0\ V \cdot R_{LIMIT}}{10 \cdot \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{ICC\_MAX} \cdot DCR\right)}$$

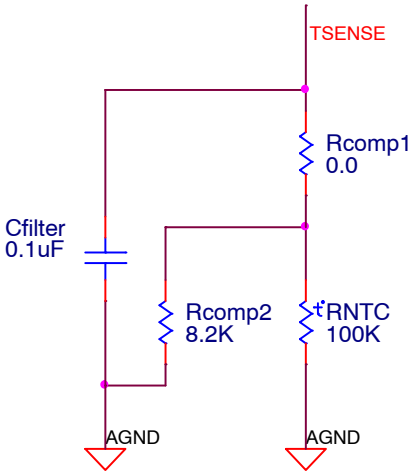
Programming ICC_MAX

A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 uA is sourced from these pins to generate a voltage on the program resistor.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 255\ A}{2\ V}$$

Programming TSENSE

A temperature sense input per rail is provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense inputs are sampled by the internal A/D converter. A 100 k NTC similar to the VISHAY ERT−J1VS104JA should be used. Rcomp1 is optional to the user, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.



Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 300 KHz/phase to 1.4 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. The oscillator frequency is approximately proportional to the current flowing in the ROSC resistor.

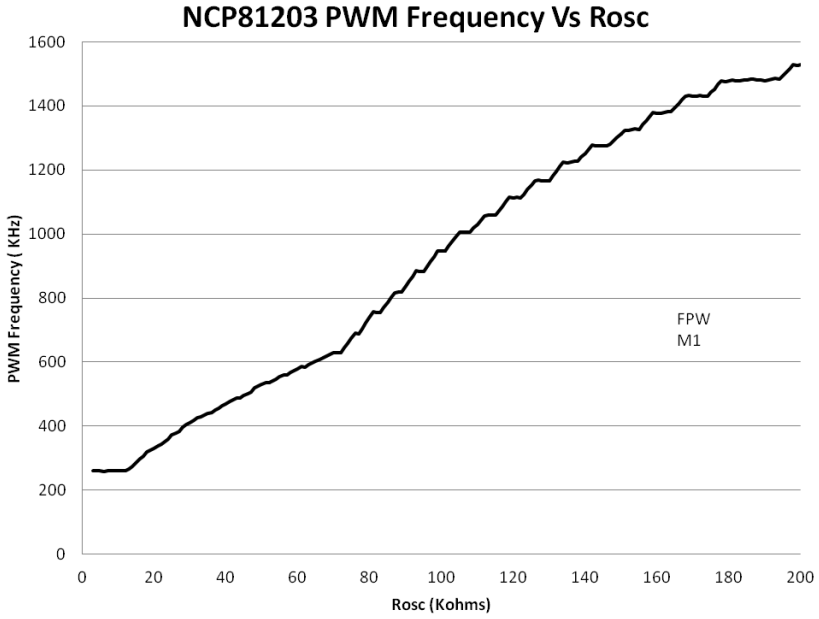


Figure 7. NCP81243 Operating Frequency vs. Rosc

The oscillator generates triangle ramps that are 1.3~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

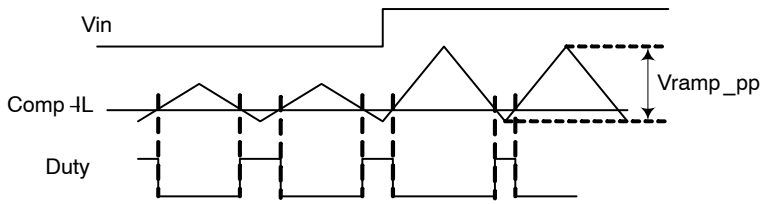
For use with **onsemi** phase doubler the NCP81243 offers the user the ability to double the frequency of each rail independently or simultaneously. This will allow the rail that is being doubled to maintain a higher system switching frequency.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following,

$$V_{RAMPpk=pk_{PP}} = 0.1 \cdot V_{VRMP}$$



PWM Comparators

The noninverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (I_L*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

Phase Detection Sequence

Normally, NCP81243 operates as a 3−phase VCORE/ 2−phase Auxiliary PWM controller however the NCP81243 can also be configures as a 4+1−phase controller. During start−up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the CSP outputs.

Configuration	Phase Configuration	Programming Pin Phase Config (30 mv/us slew rate)	Programming Pin CSPx	Unused Pins
1	4+1	80k6	All CSP pins connected normally	
2	4+0	80k6	Connect CSP1A to VCC through a 2 k resistor. All other CSP pins connected normally	Float:PWM1A, ILIMA, DIFFOUTA,COMPA,CSCOMPA Ground: IOUTA, FBA, CSSUMA, CSREFA,VSPA, TsenseA
3	3+2	13k	All CSP pins connected normally	No unused pins
4	3+1	13k	Connect CSP2A to VCC through a 2k resistor. All other CSP pins connected normally	Float: PWM2A
5	3+0	13k	Connect CSP2A and CSP1A to VCC through a 2k resistor. All other CSP pins connected normally	Float: PWM2A, PWM1A, ILIMA, DIFFOUTA, COMPA, CSCOMPA Ground: IOUTA, FBA, CSSUMA, CSREFA, VSPA, TsenseA
6	2+2	13k	Connect CSP3 to VCC through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: PWM3
7	2+1	13k	Connect CSP2A to VCC through a 2k resistor. All other CSP pins connected normally	Float PWM3, PWM2A
8	2+0	13K	Connect CSP3, CSP2A and CSP1A to VCC through a 2k resistor. All other CSP pins connected normally	Float PWM3, PWM1A, PWM2A, PWM3ILIMA, DIFFOUTA, COMPA, CSCOMPA Ground: IOUTA, FBA, CSSUMA, CSREFA, VSPA, TsenseA
9	1+2	13K	Connect CSP3 and CSP2 through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: PWM2 and PWM3
10	1+1	13K	Connect CSP3, CSP2 and CSP2A through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: PWM2, PWM3, PWM2A
11	1+0	13K	Connect CSP3, CSP2, CSP2A and CSP1A through a 2k resistor pulled to VCC. All other CSP pins connected normally	Float: PWM2, PWM3, PWM1A, PWM2A, ILIMA, DIFFOUTA, COMPA, CSCOMPA Ground: IOUTA, FBA, CSSUMA, CSREFA, VSPA, VSNA

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the NCP81151 and NCP81161. As each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one PWM output can be on at the same time to allow overlapping phases.

PROTECTION FEATURES

Under Voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81243 monitors the 5 V VCC supply. The gate driver monitors both the gate driver VCC and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off it's startup sequence. In this case the PWM is set to the MID state to begin soft start.

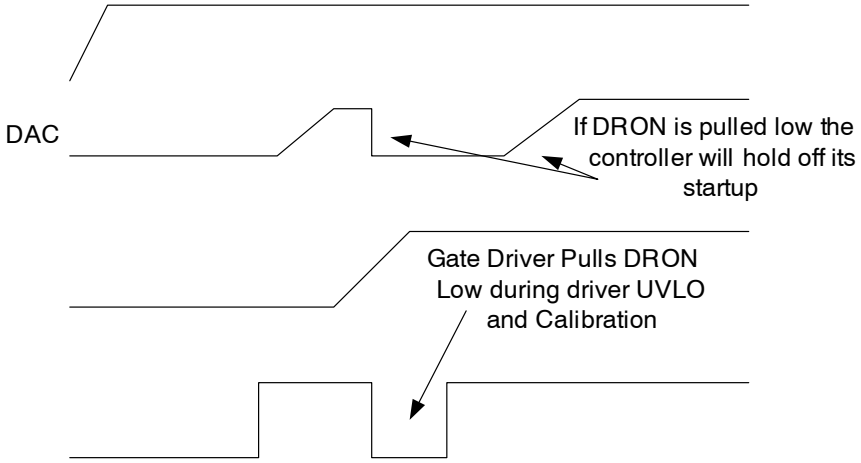


Figure 8. Gate Driver UVLO Restart

Start Up Sequence

Following the rise of Vcc and VRMP above the UVLO thresholds, externally programmed data is collected. After the configuration data is collected, the PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. When the device is enabled DRON will then be asserted high to activate the gates, please note that there is only one Enable pin, once this enable is pulled high both the main and Auxiliary rail is enabled at this time. A digital counter steps the DAC up from Zero to the target voltage level based on the soft start slew rate selected. As the DAC ramps the PWM outputs for each rail will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state. When the controller is disabled, the PWM signals will return to Mid – level.

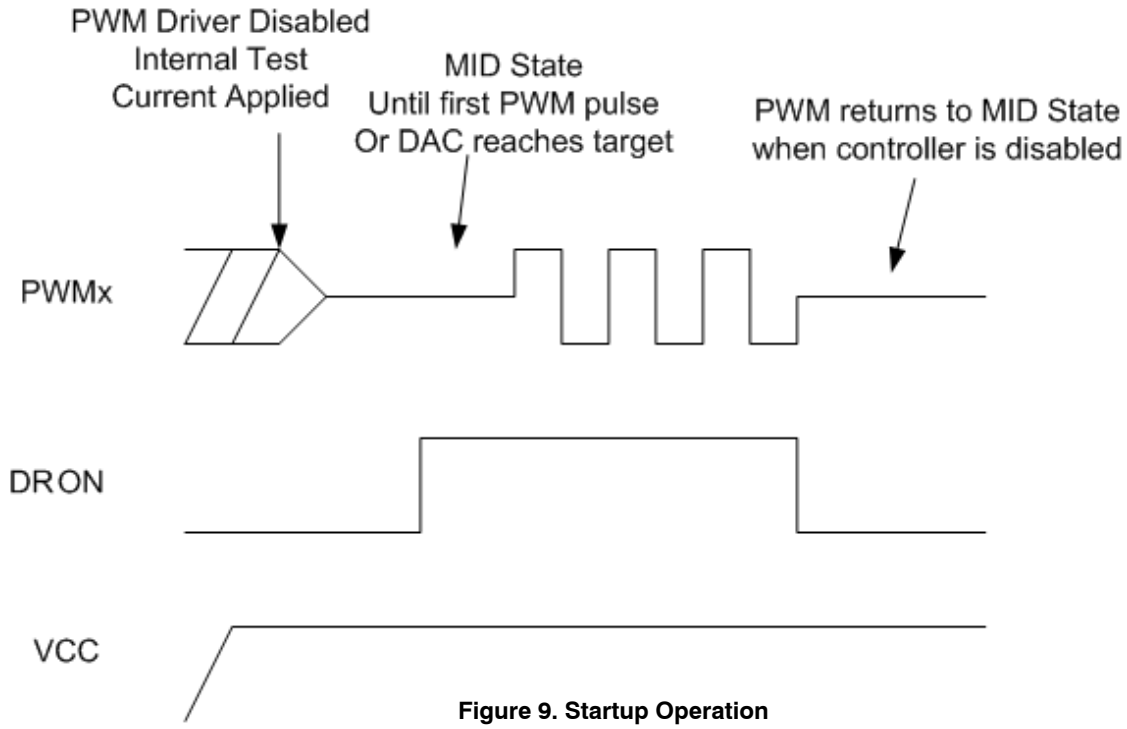


Figure 9. Startup Operation

Over Current Latch−Off Protection

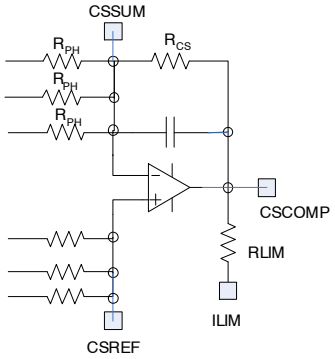
The NCP81243 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs (shut down immediately for 150% load current) after which the outputs will remain disabled until the Vcc voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations.

Equation related to the NCP81243:

$$R_{ILIM} = \frac{I_{LIM} \cdot DCR \cdot \frac{R_{CS}}{R_{PH}}}{I_{CL}}$$

Where I_{CL} = 10 μA



Input Under−Voltage Lockouts

NCP81243 monitors the 5 V VCC supply as well as the VRMP pin. Hysteresis is incorporated within these comparators. If either the Vcc or the VRMP UVLO requirements are not met the VR will fail to startup and the Intel proprietary interface interface will be unresponsive to all commands.

Under Voltage Monitor

The output voltage is monitored at the output of each differential amplifier for UVLO. If the output falls more than 300 mV below the DAC−DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low.

Over Voltage Protection

The output voltage for each rail is also monitored for OVP at the output of the differential amplifier and also at the CSREF pin. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V, the ramp to 0 V is controlled to avoid producing negative output voltage. At the same time, the PWMs of the OVP rail are sent low. The PWM outputs will pulse to mid level during the DAC ramp down period if the output decreases below the DAC+OVP threshold as DAC decreases. When the DAC reaches 0 V, the PWMs will be held low, the high side gate drivers are all turned off and the low side gate drivers are all turned on. The part will stay in this mode until the Vcc voltage or EN is toggled.

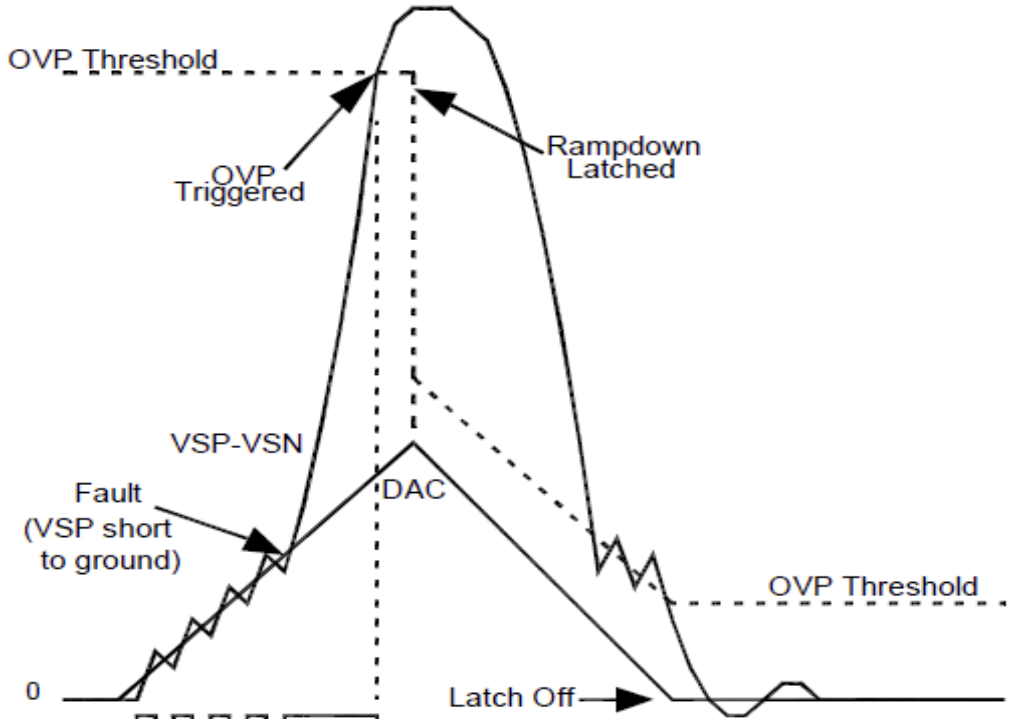


Figure 10. OVP Behavior at Startup

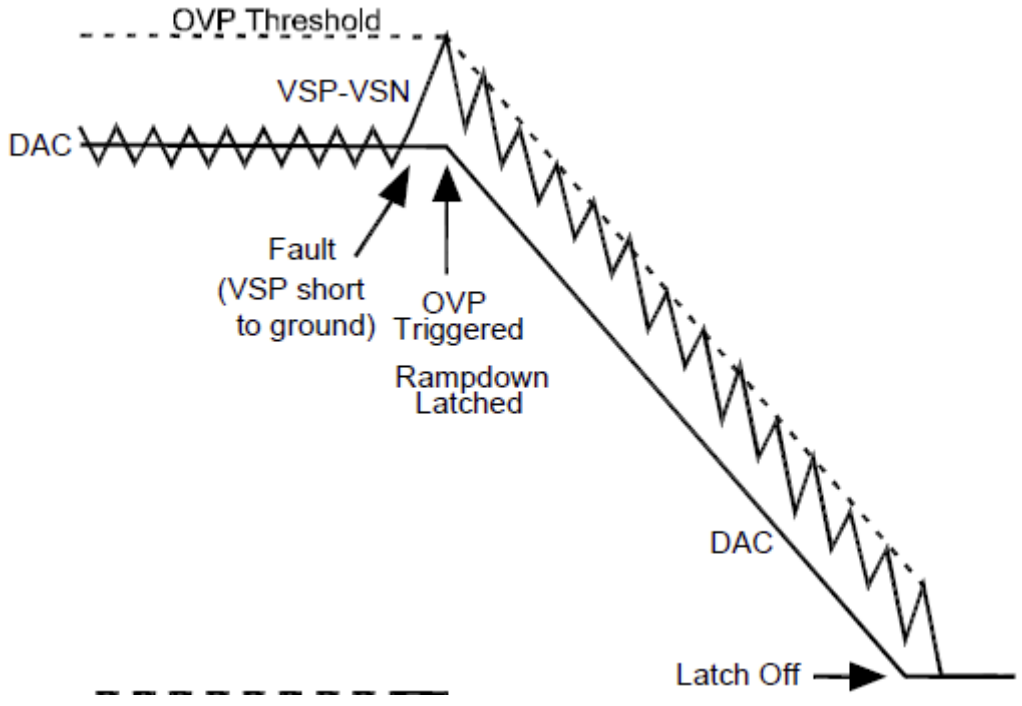
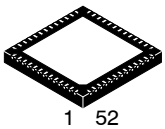


Figure 11. OVP During Normal Operation Mode

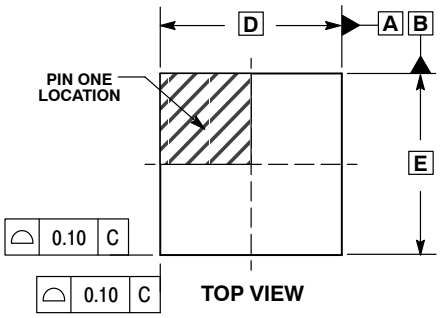
During start up, the OVP threshold is set to 2.5 V. This allows the controller to start up without false triggering the OVP

QFN52 6x6, 0.4P
CASE 485BE
ISSUE B

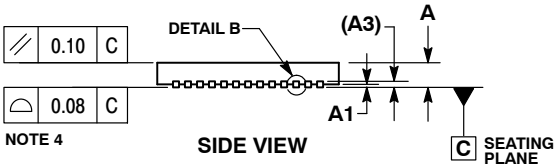
DATE 23 JUN 2010



SCALE 2:1

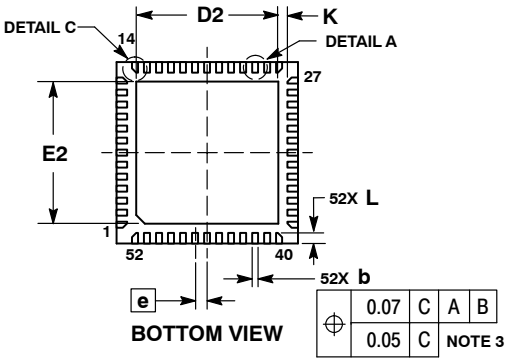


TOP VIEW



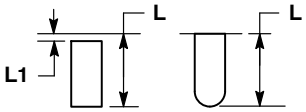
NOTE 4

SIDE VIEW

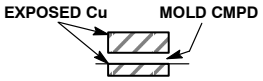


NOTE 3

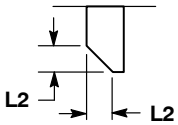
BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



DETAIL C
8 PLACES

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

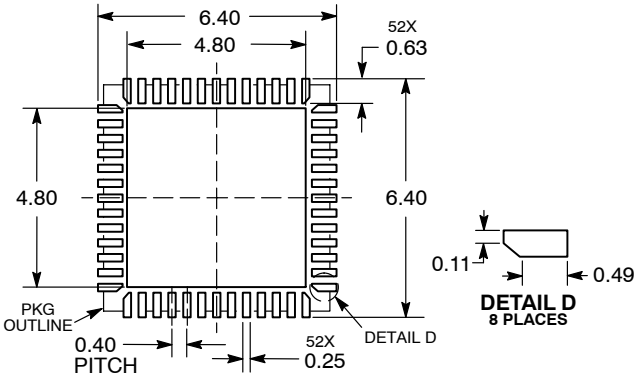
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DETAIL D
8 PLACES

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON47515E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN52, 6x6, 0.4MM PITCH**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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