

Single Unbuffered Inverter

NLV74VHC1GU04

The NLV74VHC1GU04 is an advanced high speed CMOS unbuffered inverter in tiny footprint packages.

This device consists of a single unbuffered inverter. In combination with others, or in the NLV74VHCU04 Hex Unbuffered Inverter, these devices are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the NLV74VHC1G04 or the NLV74VHC04 are recommended.

The input structures provide protection when voltages up to 5.5 V are applied, regardless of the supply voltage. This allows the device to be used to interface 5 V circuits to 3 V circuits.

Features

- Designed for 2.0 V to 5.5 V V_{CC} Operation
- 2.5 ns t_{PD} at 5 V (typ)
- Inputs Over-Voltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection on Input
- Source/Sink 8 mA at 3.0 V
- Available in SC-88A and TSOP-5 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

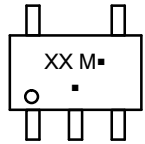


Figure 1. Logic Symbol

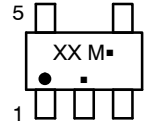


SC-88A
DF SUFFIX
CASE 419A

MARKING DIAGRAMS



TSOP-5
DT SUFFIX
CASE 483



XX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

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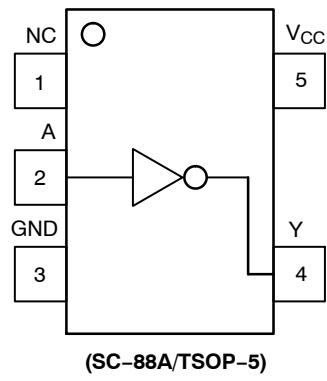


Figure 2. Pinout (Top View)

PIN ASSIGNMENT (SC-88A/TSOP-5)

Pin	Function
1	NC
2	A
3	GND
4	Y
5	V _{CC}

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

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MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-20	mA
I _{OK}	DC Output Diode Current	±20	mA
I _{OUT}	DC Output Source/Sink Current	±25	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SC-88A TSOP-5 377 320	°C/W
P _D	Power Dissipation in Still Air	SC-88A TSOP-5 332 390	mW
MSL	Moisture Sensitivity	Level 1	-
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model 2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
3. HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0	1.7	-	-	1.7	-	1.7	-	V
			3.0	2.4	-	-	2.4	-	2.4	-	
			4.5	3.6	-	-	3.6	-	3.6	-	
			5.5	4.4	-	-	4.4	-	4.4	-	
V _{IL}	Low-Level Input Voltage		2.0	-	-	0.3	-	0.3	-	0.3	V
			3.0	-	-	0.6	-	0.6	-	0.6	
			4.5	-	-	0.9	-	0.9	-	0.9	
			5.5	-	-	1.1	-	1.1	-	1.1	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	2.0	1.9	2.0	-	1.9	-	1.9	-	V
			3.0	2.9	3.0	-	2.9	-	2.9	-	
			4.5	4.4	4.5	-	4.4	-	4.4	-	
		V _{IN} = GND I _{OH} = -4 mA I _{OH} = -8 mA	3.0	2.58	-	-	2.48	-	2.34	-	
			4.5	3.94	-	-	3.80	-	3.66	-	
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	2.0	-	0.0	0.1	-	0.1	-	0.1	V
			3.0	-	0.0	0.1	-	0.1	-	0.1	
			4.5	-	0.0	0.1	-	0.1	-	0.1	
		V _{IN} = V _{CC} I _{OL} = 4 mA I _{OL} = 8 mA	3.0	-	-	0.36	-	0.44	-	0.52	
			4.5	-	-	0.36	-	0.44	-	0.52	
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	2.0 to 5.5	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V	0	-	-	1.0	-	10	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	1.0	-	20	-	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

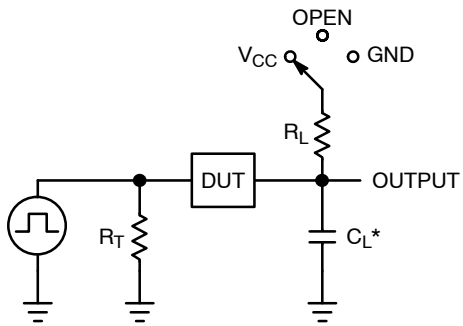
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, A to Y (Figures 3 and 4)	C _L = 15 pF	3.0 to 3.6	-	3.5	8.9	-	10.5	-	12.0	ns
				-	4.8	11.4	-	13.0	-	15.5	
		C _L = 50 pF	4.5 to 5.5	-	2.5	5.5	-	6.5	-	8.0	
				-	3.8	7.0	-	8.0	-	9.5	
C _{IN}	Input Capacitance			-	4.0	10	-	10	-	10	pF

C _{PD}	Power Dissipation Capacitance (Note 5)	Typical @ 25°C, V _{CC} = 5.0 V	
		22.0	
		pF	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Figure 3. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X = Don't Care

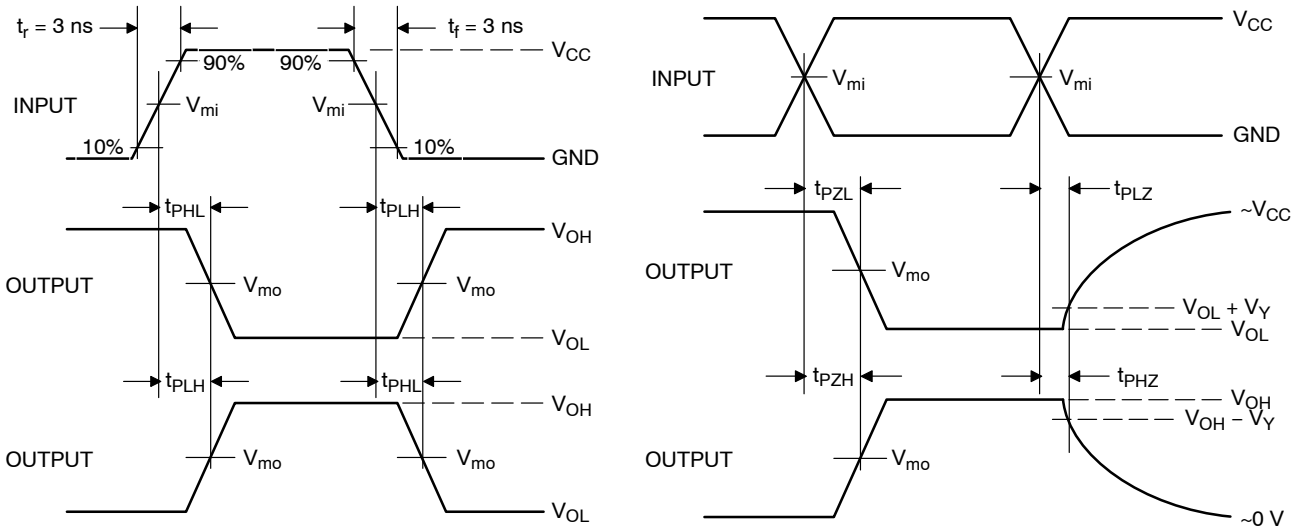


Figure 4. Switching Waveforms

V_{CC} , V	V_{mi} , V	V_{mo} , V		V_Y , V
		t_{PLH} , t_{PHL}	t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}	
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

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ORDERING INFORMATION

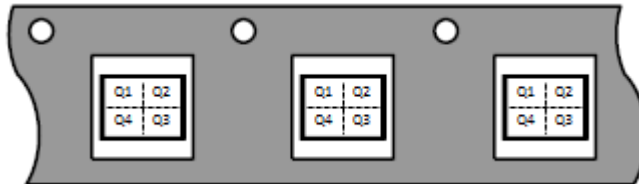
Device	Package	Specific Device Code	Pin 1 Orientation (See below)	Shipping†
MC74VHC1GU04DF1G-L22038	SC-88A	V6	Q2	3000 / Tape & Reel
M74VHC1GU04DFT1G-L22038	SC-88A	V6	Q2	3000 / Tape & Reel
NLVVHC1GU04DFT2G*	SC-88A	V6	Q4	3000 / Tape & Reel
M74VHC1GU04DTT1G	TSOP-5	M0	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel

Direction of Feed



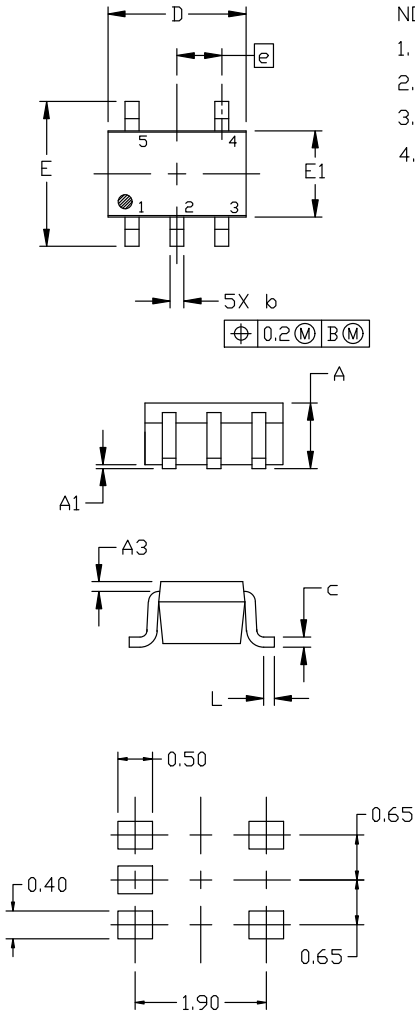
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PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE M

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30

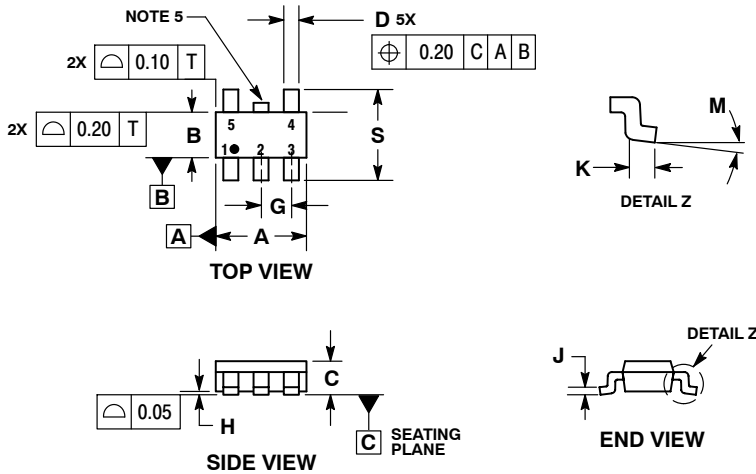
RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE N

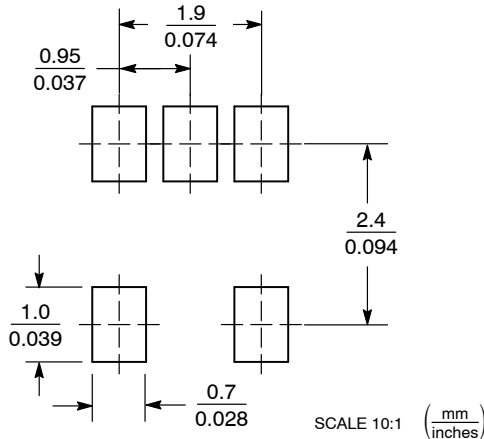


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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