

NTD110N02R, STD110N02R

MOSFET – Power, N-Channel, DPAK

24 V, 110 A

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	24	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	V
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.35	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	110	W
Drain Current	I_D	110	A
– Continuous @ $T_C = 25^\circ\text{C}$, Chip	I_D	110	A
– Continuous @ $T_C = 25^\circ\text{C}$	I_D	110	A
Limited by Package	I_D	32	A
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	32	A
Limited by Wires	I_D	110	A
– Single Pulse ($t_p = 10 \mu\text{s}$)	I_D	110	A
Thermal Resistance	$R_{\theta JA}$	52	$^\circ\text{C/W}$
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.88	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	17.5	A
Thermal Resistance	$R_{\theta JA}$	100	$^\circ\text{C/W}$
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.5	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	I_D	12.5	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_L = 15.5 \text{ Apk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	120	mJ
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

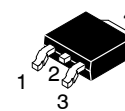
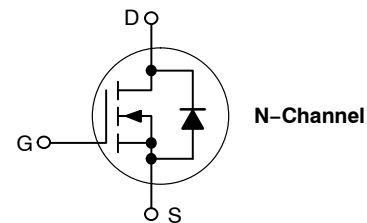
1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.



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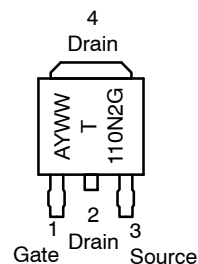
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	4.1 m Ω @ 10 V	110 A



DPAK
CASE 369AA
(Surface Mount)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
T110N2 = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NTD110N02R, STD110N02R

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$)	$V_{(BR)DSS}$	24	28		V
Positive Temperature Coefficient			15		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{DSS}			1.5 10	μA
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$)	$V_{GS(th)}$	1.0	1.5 5.0	2.0	V mV/ $^\circ\text{C}$
Negative Threshold Temperature Coefficient					
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10\text{ V}$, $I_D = 110\text{ A}$) ($V_{GS} = 4.5\text{ V}$, $I_D = 55\text{ A}$) ($V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$) ($V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$)	$R_{DS(on)}$		4.1 5.5 3.9 5.5	4.6 6.2	m Ω
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$) (Note 3)	g_{FS}		44		Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz})$	C_{iss}		2710 3440	pF
Output Capacitance		C_{oss}		1105 1670	
Transfer Capacitance		C_{rss}		450 640	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{GS} = 10\text{ V}, V_{DD} = 10\text{ V}, I_D = 40\text{ A}, R_G = 3.0\ \Omega)$	$t_{d(on)}$		11 22	ns
Rise Time		t_r		39 80	
Turn-Off Delay Time		$t_{d(off)}$		27 40	
Fall Time		t_f		21 40	
Gate Charge	$(V_{GS} = 4.5\text{ V}, I_D = 40\text{ A}, V_{DS} = 10\text{ V})$ (Note 3)	Q_T		23.6 28	nC
		Q_{GS}		5.1	
		Q_{GD}		11	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 20\text{ A}, V_{GS} = 0\text{ V})$ (Note 3) $(I_S = 55\text{ A}, V_{GS} = 0\text{ V})$ $(I_S = 20\text{ A}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C})$	V_{SD}		0.82 0.99 0.65	1.2	V
Reverse Recovery Time	$(I_S = 30\text{ A}, V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s})$ (Note 3)	t_{rr}		36.5		ns
		t_a		30		
		t_b		25		
Reverse Recovery Stored Charge		Q_{rr}		0.048		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NTD110N02R, STD110N02R

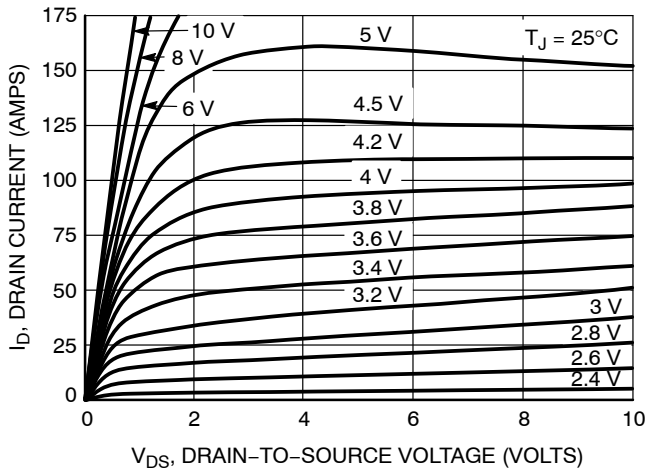


Figure 1. On-Region Characteristics

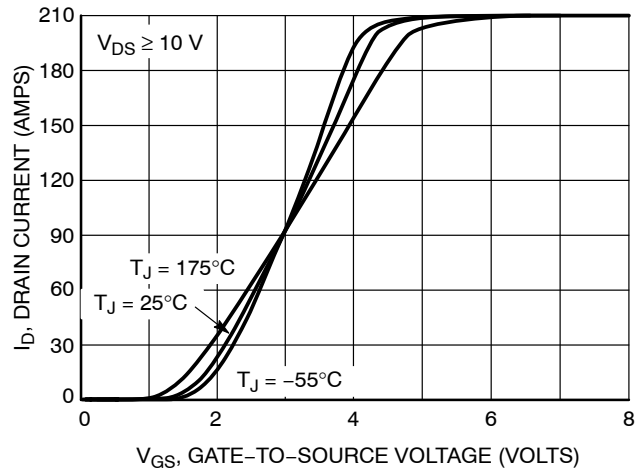


Figure 2. Transfer Characteristics

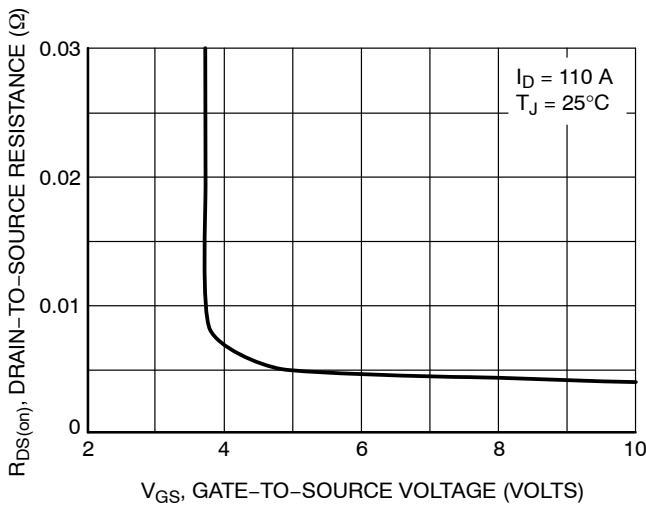


Figure 3. On-Resistance versus Gate-to-Source Voltage

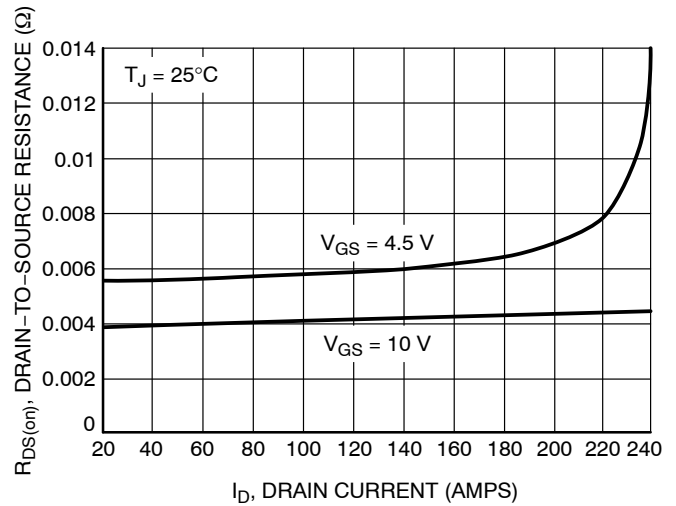


Figure 4. On-Resistance versus Drain Current and Gate Voltage

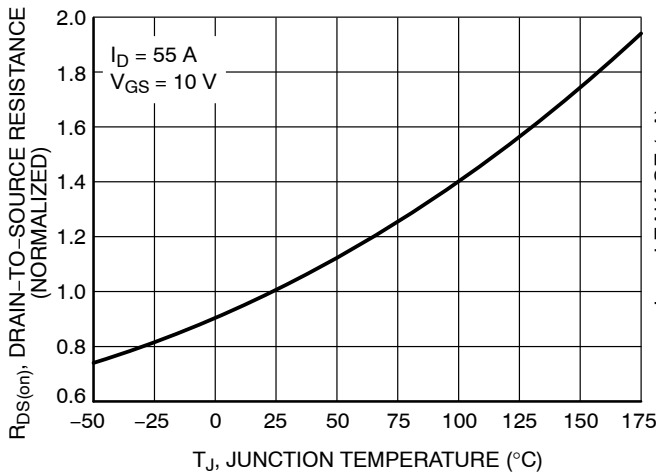


Figure 5. On-Resistance Variation with Temperature

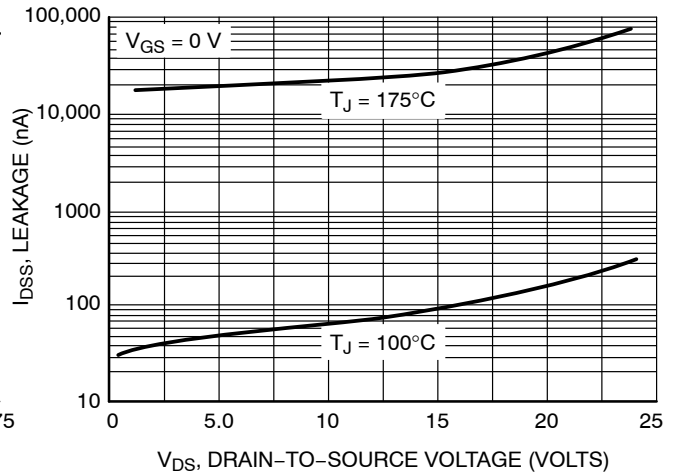


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD110N02R, STD110N02R

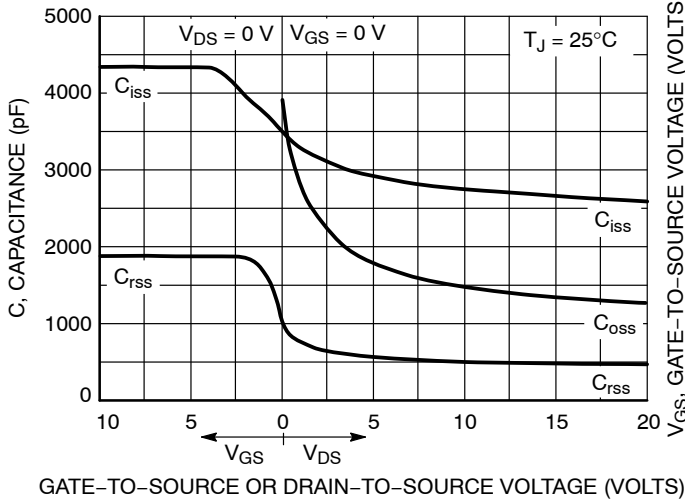


Figure 7. Capacitance Variation

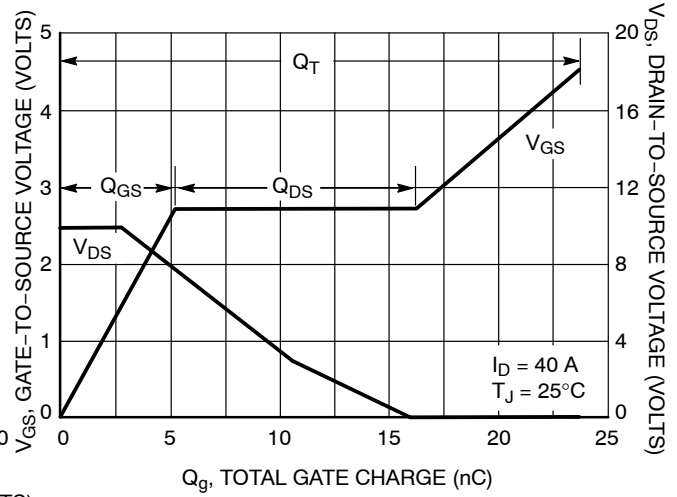


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

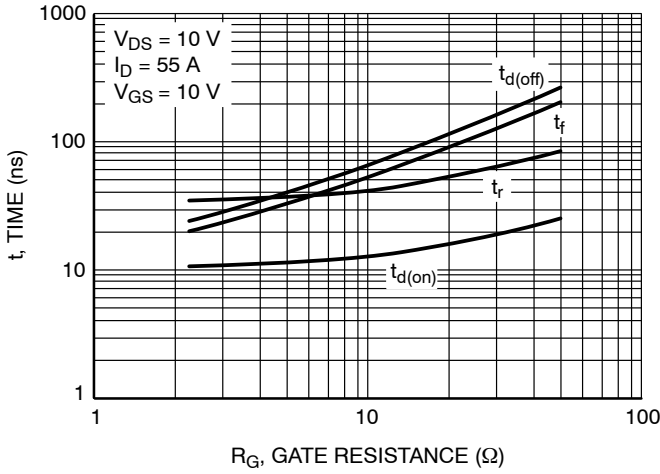


Figure 9. Resistive Switching Time Variation versus Gate Resistance

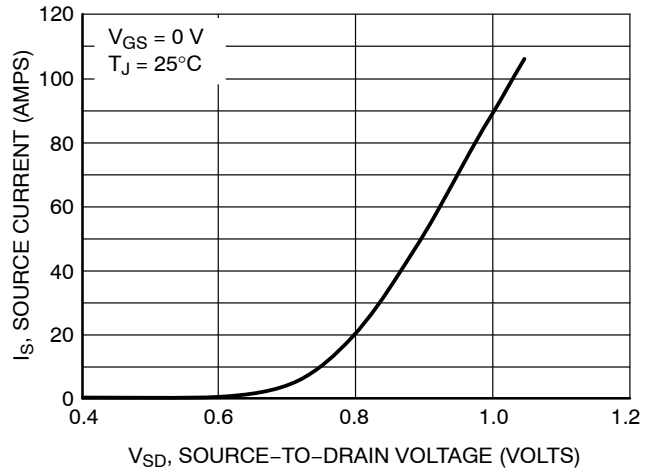


Figure 10. Diode Forward Voltage versus Current

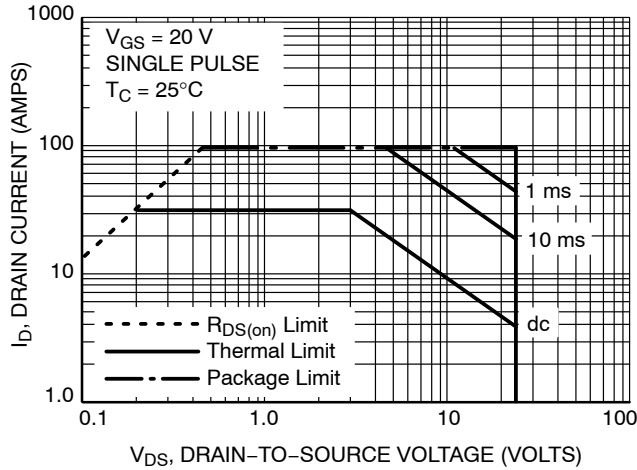


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD110N02R, STD110N02R

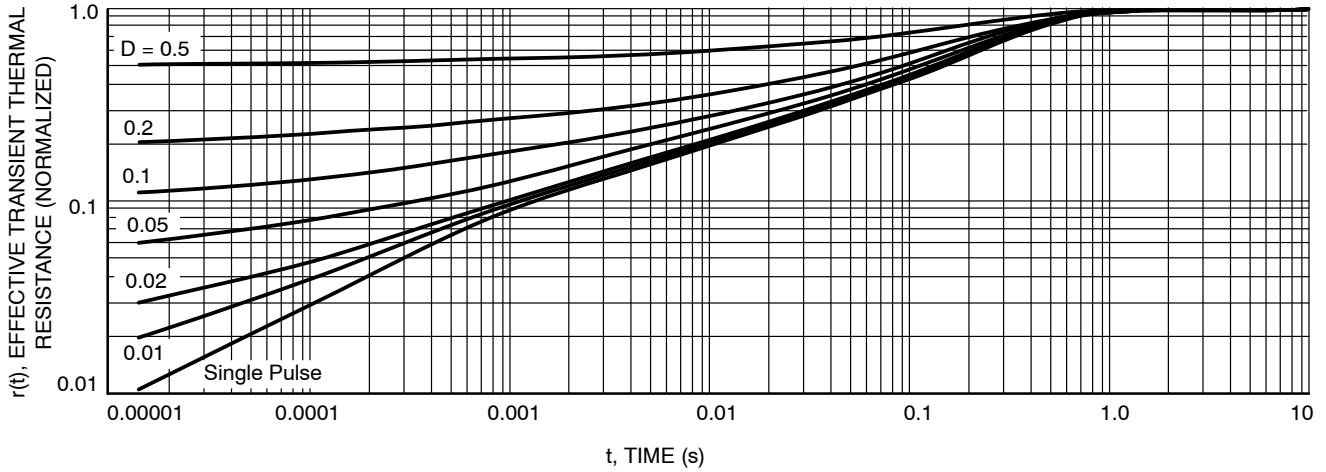


Figure 12. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD110N02RT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD110N02RT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

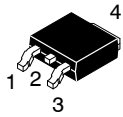
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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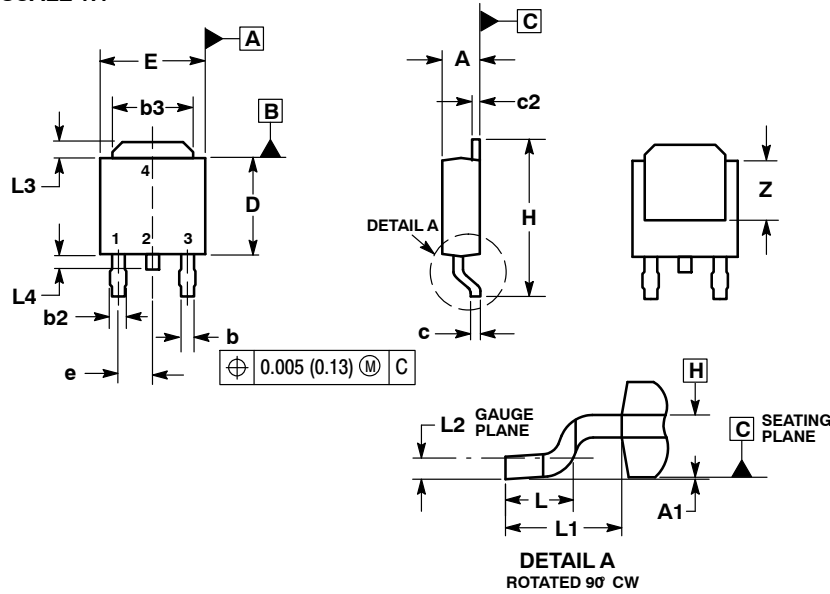
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



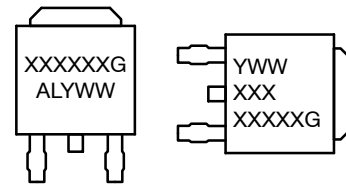
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- | | | | |
|--|---|--|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> |
| <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> | <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | |

GENERIC MARKING DIAGRAM*



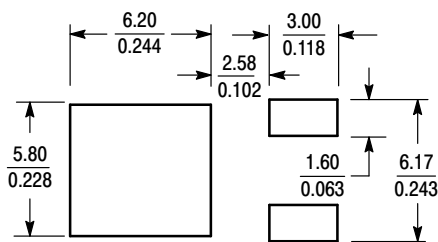
IC

Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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