

# NTD6415AN, NVD6415AN

## MOSFET – Power, N-Channel

**100 V, 23 A, 55 mΩ**

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	100	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$	$I_D$	$T_C = 25^\circ\text{C}$	23
		$T_C = 100^\circ\text{C}$	16
Power Dissipation $R_{\theta JC}$	Steady State $T_C = 25^\circ\text{C}$	$P_D$	83
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	89
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	23	A
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 50 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_{L(pk)} = 23 \text{ A}$ , $L = 0.3 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	79	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	39	

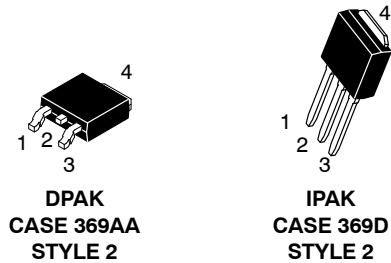
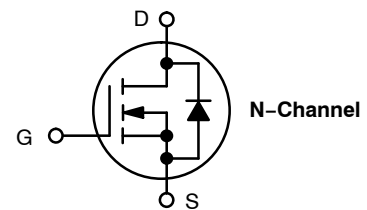
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



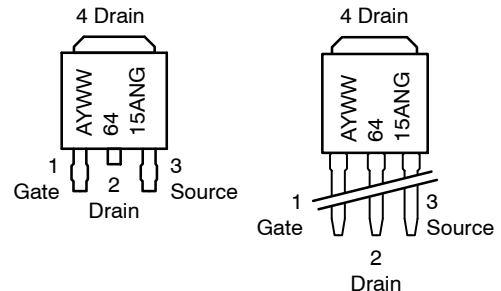
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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX (Note 1)
100 V	55 mΩ @ 10 V	23 A



### MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location\*  
 Y = Year  
 WW = Work Week  
 6415AN = Device Code  
 G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTD6415AN, NVD6415AN

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			113		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.0		4.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			7.6		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 23 A		47	55	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> = 5 V, I <sub>D</sub> = 10 A		13		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		700		pF	
Output Capacitance	C <sub>OSS</sub>			110			
Reverse Transfer Capacitance	C <sub>RSS</sub>			52			
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 80 V, I <sub>D</sub> = 23 A		29		nC	
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.2			
Gate-to-Source Charge	Q <sub>GS</sub>			5			
Gate-to-Drain Charge	Q <sub>GD</sub>			14.6			
Plateau Voltage	V <sub>GP</sub>			5.7			V
Gate Resistance	R <sub>G</sub>			2.3			Ω

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 80 V, I <sub>D</sub> = 23 A, R <sub>G</sub> = 6.1 Ω		10		ns
Rise Time	t <sub>r</sub>			37		
Turn-Off Delay Time	t <sub>d(off)</sub>			30		
Fall Time	t <sub>f</sub>			37		

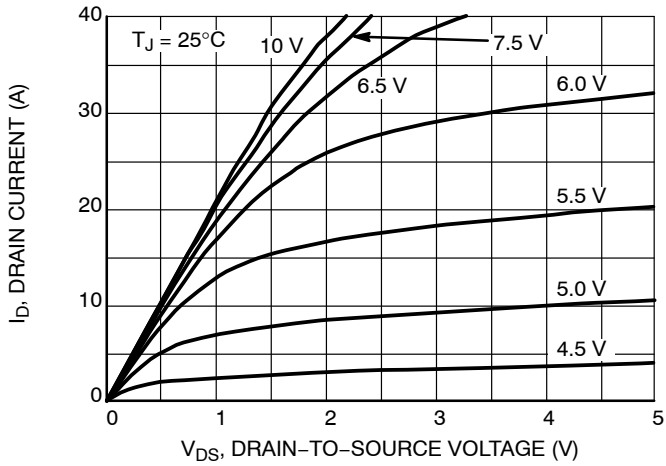
### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 23 A	T <sub>J</sub> = 25°C	0.83	1.2	V
			T <sub>J</sub> = 125°C	0.68		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 23 A		65		ns
Charge Time	T <sub>a</sub>			46		
Discharge Time	T <sub>b</sub>			19		
Reverse Recovery Charge	Q <sub>RR</sub>			176		

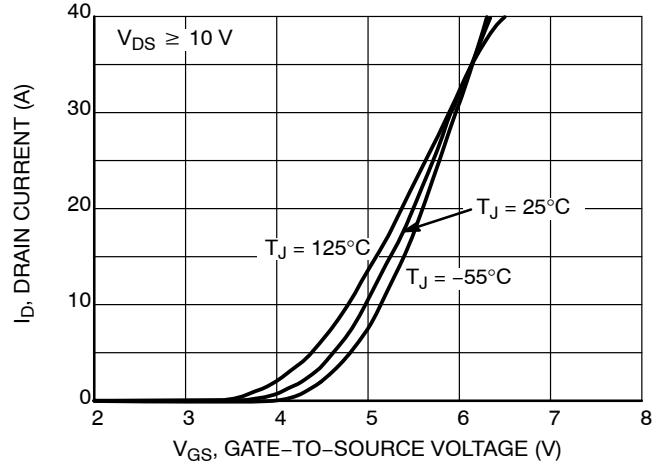
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

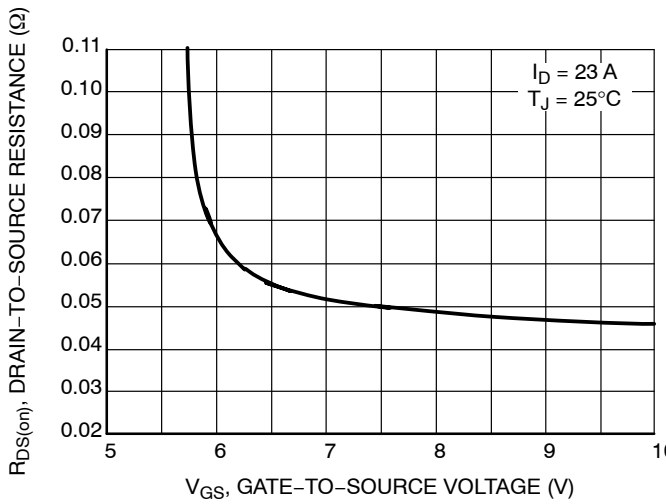
# NTD6415AN, NVD6415AN



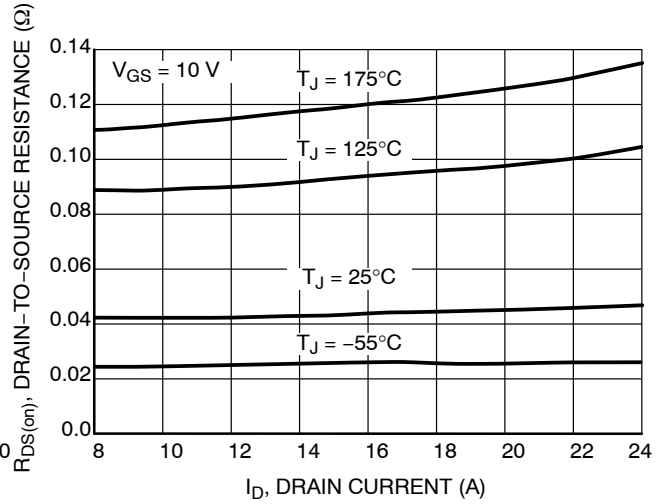
**Figure 1. On-Region Characteristics**



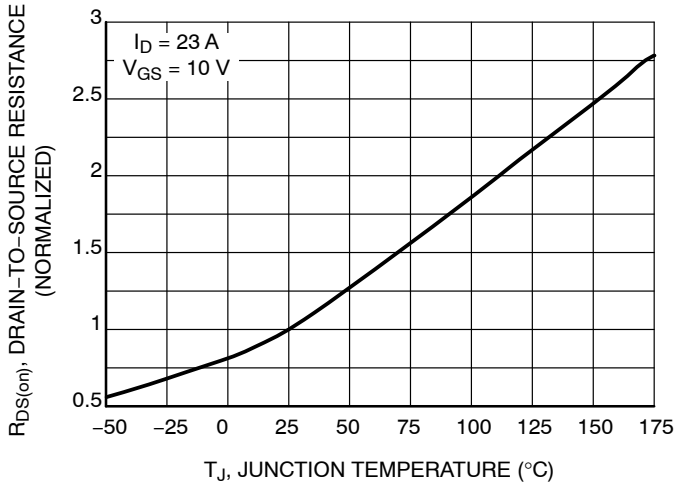
**Figure 2. Transfer Characteristics**



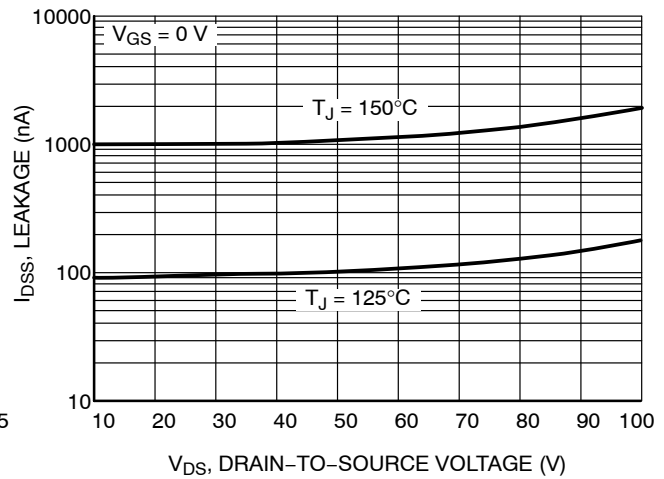
**Figure 3. On-Region versus Gate Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

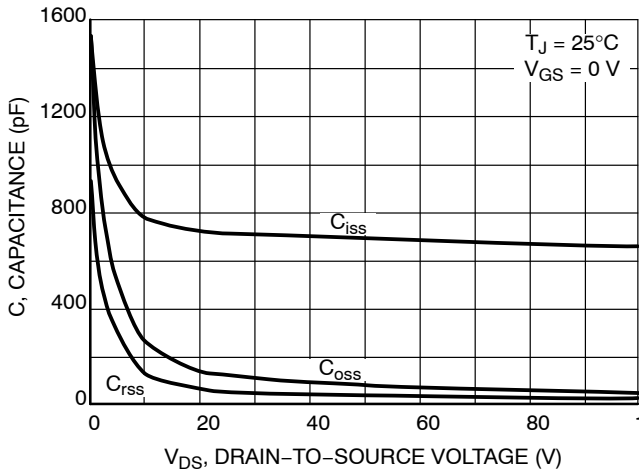


**Figure 5. On-Resistance Variation with Temperature**

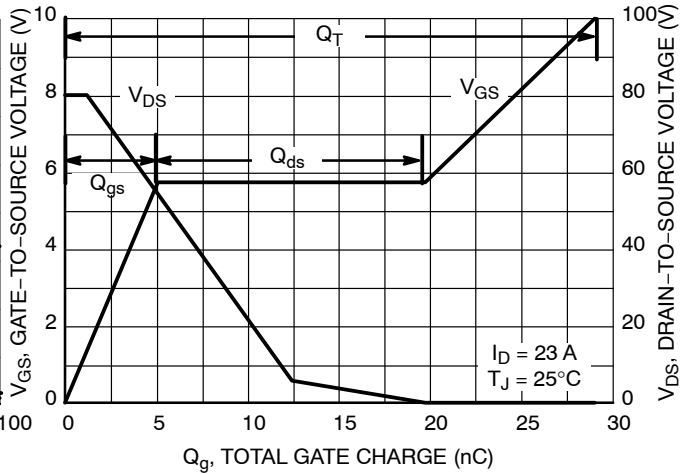


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

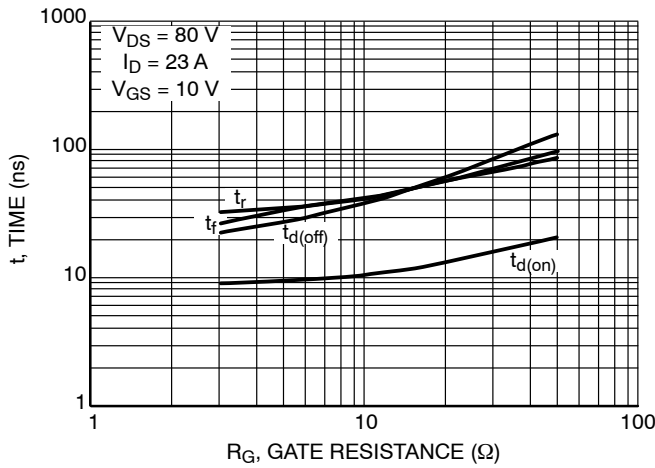
# NTD6415AN, NVD6415AN



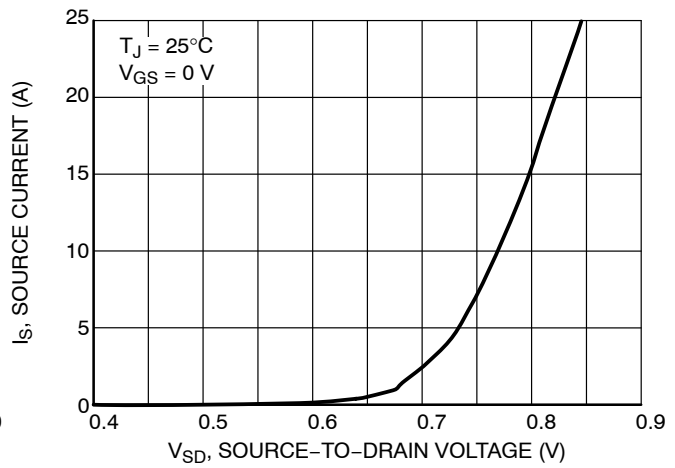
**Figure 7. Capacitance Variation**



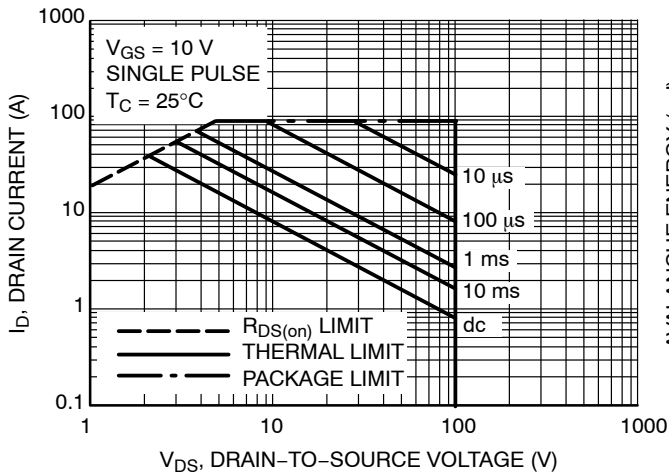
**Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge**



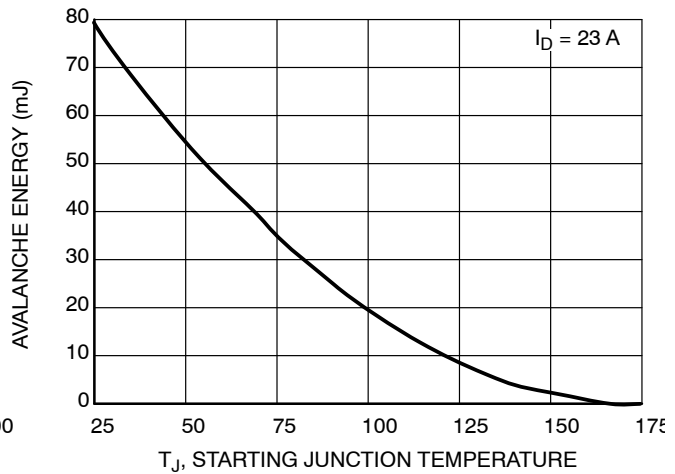
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**

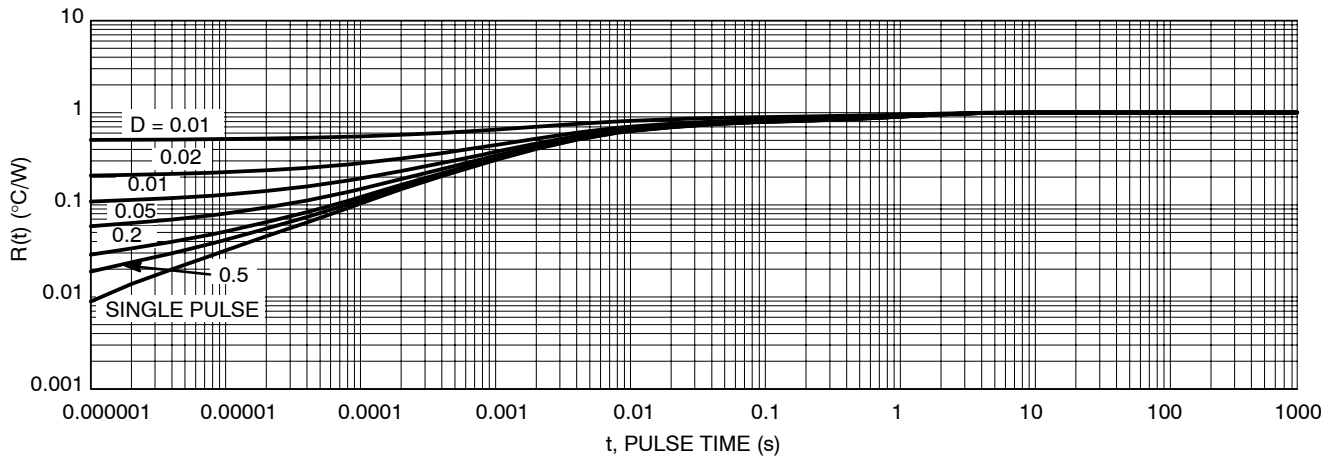


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

# NTD6415AN, NVD6415AN



**Figure 13. Thermal Response**

## ORDERING INFORMATION

Device	Package	Shipping†
NTD6415ANT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD6415AN-1G	IPAK (Pb-Free)	75 Units / Rail
NVD6415ANT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

\*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1



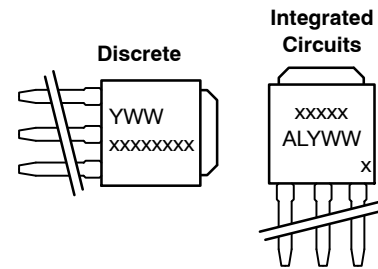
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

### MARKING DIAGRAMS

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR



- xxxxxxxx = Device Code
- A = Assembly Location
- IL = Wafer Lot
- Y = Year
- WW = Work Week

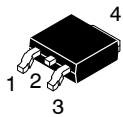
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<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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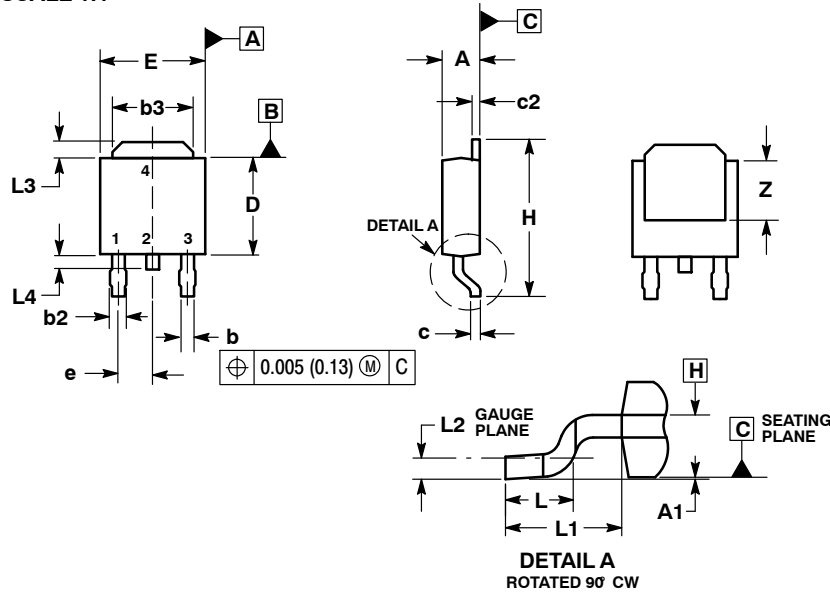
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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SCALE 1:1



### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010

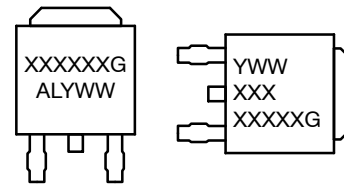
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### GENERIC MARKING DIAGRAM\*



IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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