

NTGD4161P

Power MOSFET

-30 V, -2.3 A, Dual P-Channel, TSOP-6

Features

- Fast Switching Speed
- Low Gate Charge
- Low $R_{DS(on)}$
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb-Free Device

Applications

- Load Switch
- Battery Protection
- Portable Devices Like PDAs, Cellular Phones and Hard Drives

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	-30	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-2.1	A
		$T_A = 85^\circ\text{C}$	-1.5	
		$t \leq 5 \text{ s}$, $T_A = 25^\circ\text{C}$	-2.3	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.1	W
		$t \leq 5 \text{ s}$	1.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	-1.5	A
		$T_A = 85^\circ\text{C}$	-1.1	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	0.6	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-10	A
Operating Junction and Storage Temperature	T_J , T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	-0.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	115	$^\circ\text{C/W}$
Junction-to-Ambient - Steady State (Note 2)		225	
Junction-to-Ambient - $t \leq 5 \text{ s}$ (Note 1)		95	
Junction-to-Case - Steady State (Note 1)	$R_{\theta JC}$	40	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.2 in² [1 oz] including traces)
2. When surface mounted to an FR4 board using minimum recommended pad size (Cu. area = 0.047 in²)

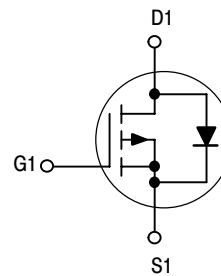


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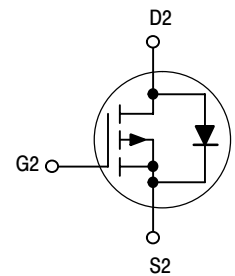
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$V_{(BR)DSS}$	$R_{DS(on)}$ Max
-30 V	160 m Ω @ -10 V
	280 m Ω @ -4.5 V

P-Channel (MOSFET1)



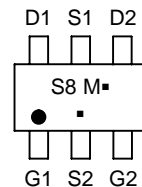
P-Channel (MOSFET2)



MARKING DIAGRAM



TSOP-6
CASE 318G
STYLE 13



- S8 = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTGD4161PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTGD4161P

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			22		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V	T _J = 25°C		-1.0	μA
			T _J = 125°C		-10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1.0	-1.9	-3.0	V
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-4.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -2.1 A		105	160	mΩ
		V _{GS} = -4.5 V, I _D = -1.6 A		190	280	
Forward Transconductance	g _{FS}	V _{DS} = -5.0 V, I _D = -2.1 A		2.7		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{DS} = -15 V, f = 1.0 MHz, V _{GS} = 0 V		281		pF
Output Capacitance	C _{OSS}			50		
Reverse Transfer Capacitance	C _{RSS}			28		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -5.0 V, I _D = -2.1 A		5.6	7.1	nC
Threshold Gate Charge	Q _{G(TH)}			0.65		
Gate-to-Source Charge	Q _{GS}			1.2		
Gate-to-Drain Charge	Q _{GD}			0.90		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -15 V, I _D = -1.0 A, R _G = 6.0 Ω		7.6	14	ns
Rise Time	t _r			9.2	23	
Turn-Off Delay Time	t _{d(off)}			12.5	20	
Fall Time	t _f			4.5	12	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -0.8 A	T _J = 25°C		-0.79	-1.2	V
			T _J = 125°C		-0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -0.8 A		8.0		ns	
Charge Time	t _a			5.7			
Discharge Time	t _b			2.3			
Reverse Recovery Charge	Q _{RR}			3			nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

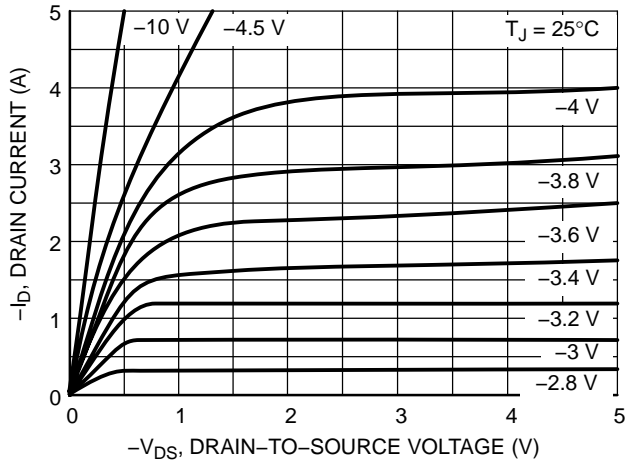


Figure 1. On-Region Characteristics

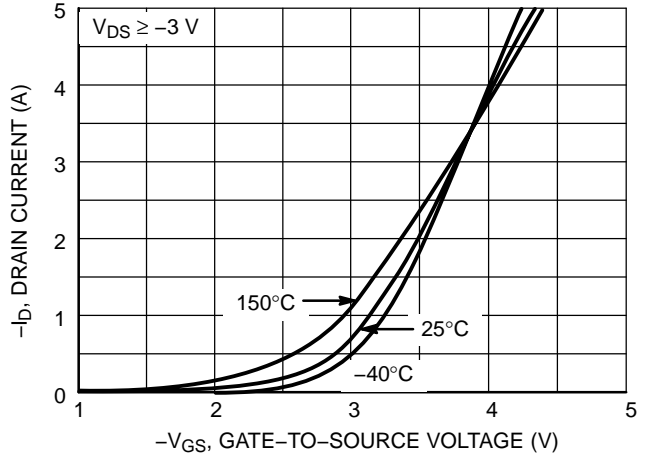


Figure 2. Transfer Characteristics

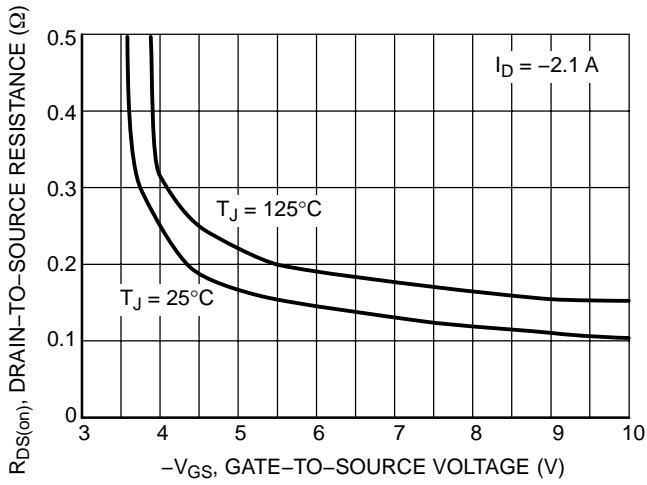


Figure 3. On-Resistance versus Gate-to-Source Voltage

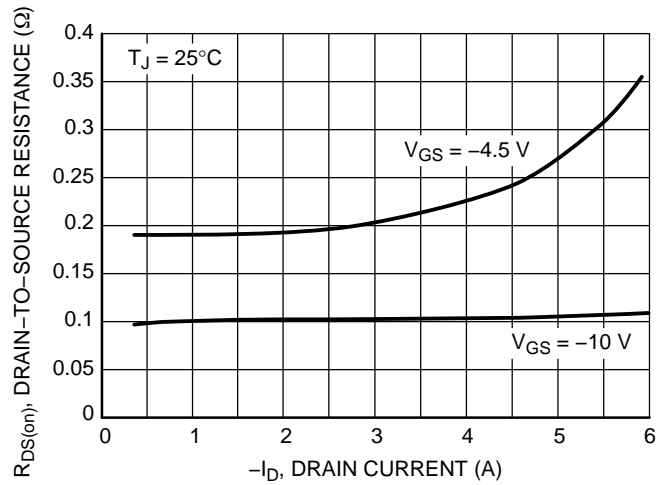


Figure 4. On-Resistance versus Drain Current and Temperature

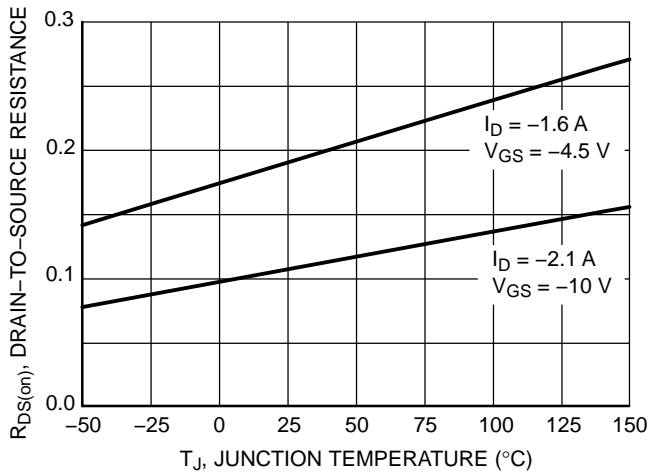


Figure 5. On-Resistance Variation with Temperature

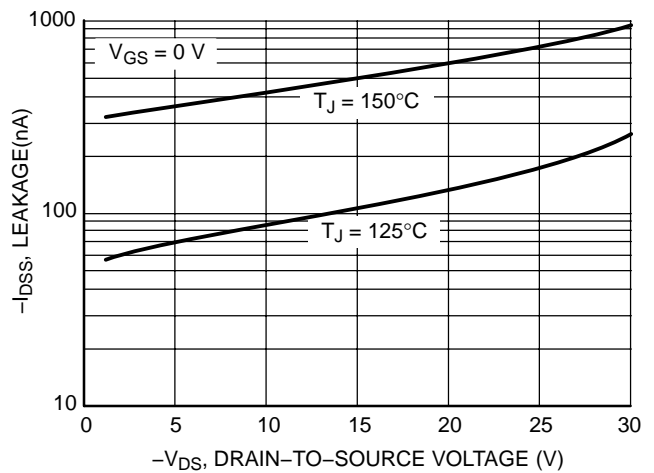


Figure 6. On-Resistance Variation with Temperature

NTGD4161P

TYPICAL PERFORMANCE CURVES

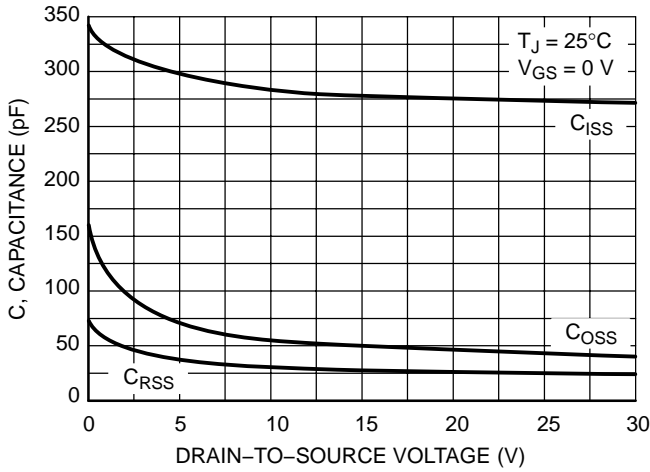


Figure 7. Capacitance Variation

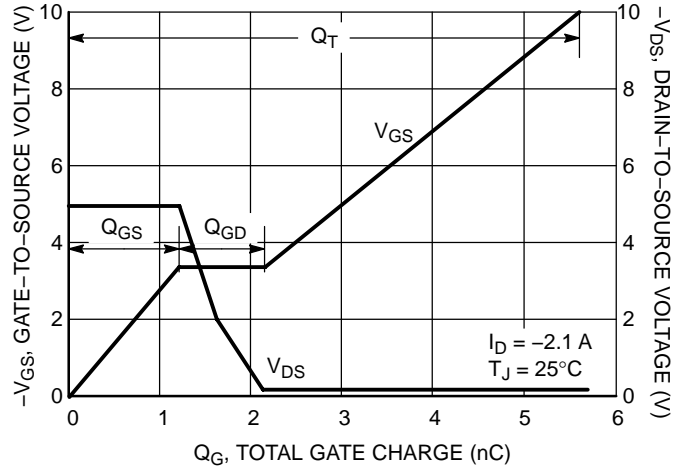


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

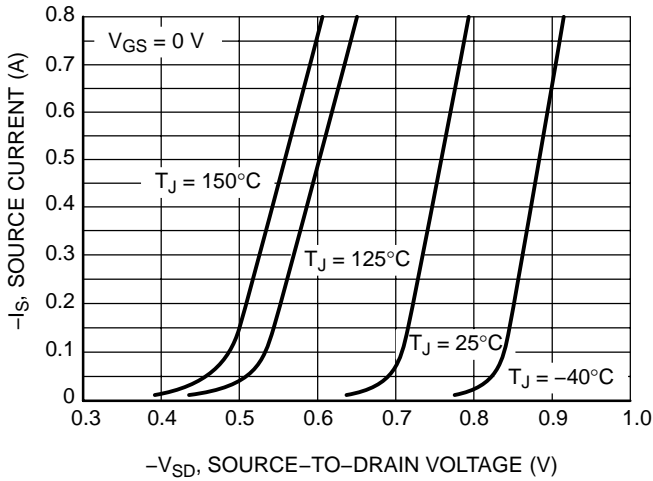


Figure 9. Diode Forward Voltage versus Current

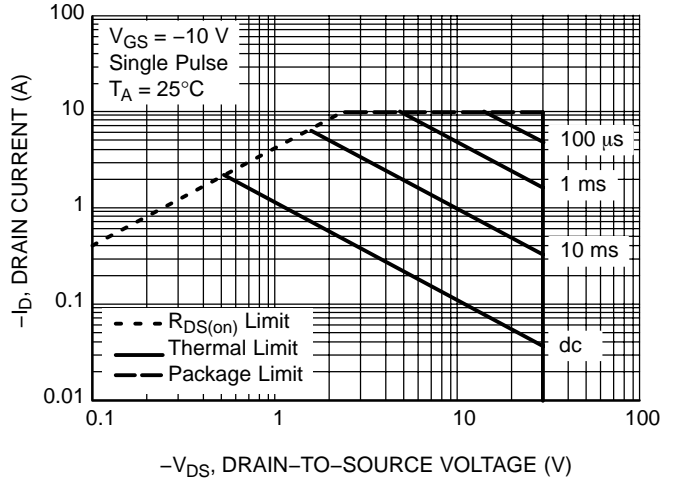


Figure 10. Maximum Rated Forward Biased Safe Operating Area

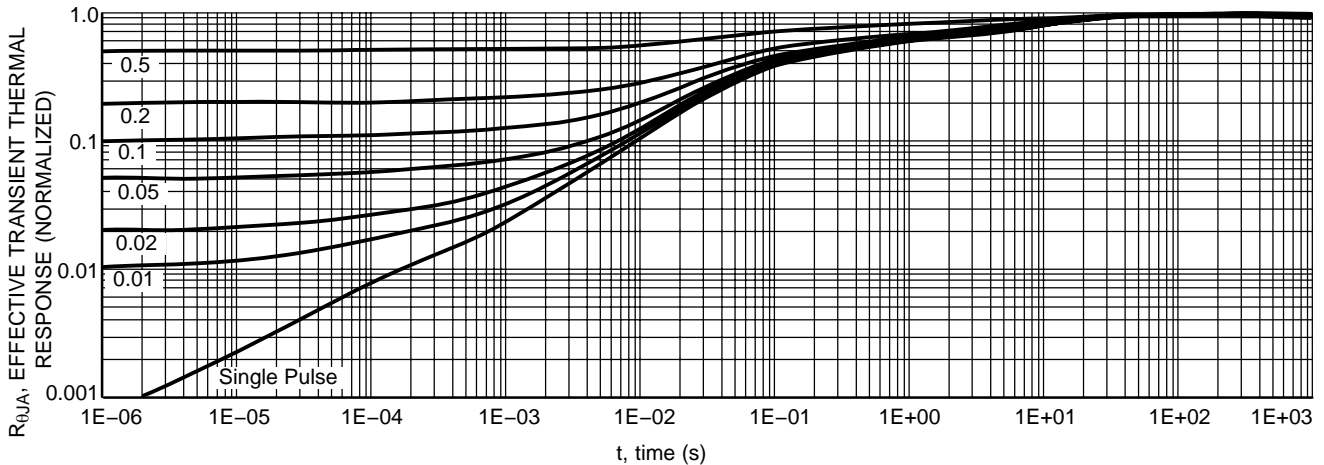
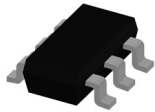


Figure 11. FET Thermal Response

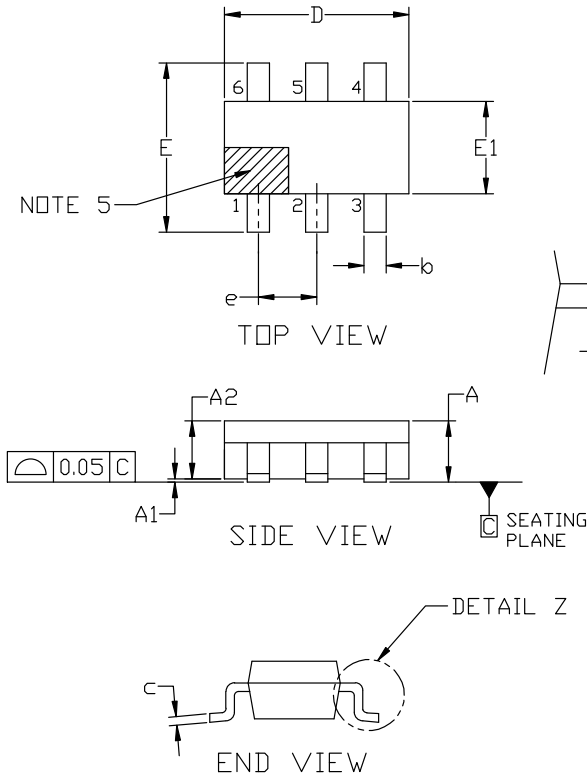
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

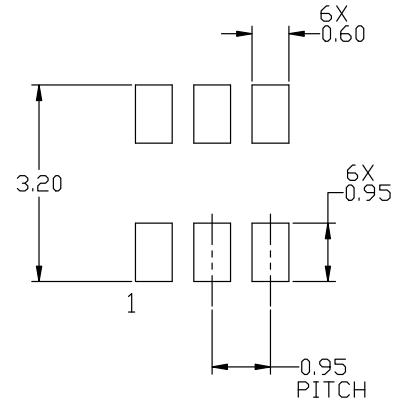
DATE 26 FEB 2024



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 1 OF 2

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MECHANICAL CASE OUTLINE

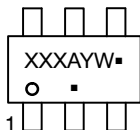
PACKAGE DIMENSIONS



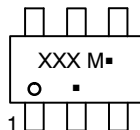
TSOP-6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- 2. BASE 1
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 2
- 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- 2. N/C
- 3. R BOOST
- 4. Vz
- 5. V in
- 6. V out

STYLE 4:

- PIN 1. N/C
- 2. V in
- 3. NOT USED
- 4. GROUND
- 5. ENABLE
- 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. N/C
- 5. COLLECTOR
- 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- 2. D(in)
- 3. D(in)+
- 4. D(out)+
- 5. D(out)
- 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN
- 5. DRAIN
- 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- 2. GND
- 3. D(OUT)-
- 4. D(IN)-
- 5. VBUS
- 6. D(IN)+

STYLE 11:

- PIN 1. SOURCE 1
- 2. DRAIN 2
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 1
- 6. DRAIN 1/GATE 2

STYLE 12:

- PIN 1. I/O
- 2. GROUND
- 3. I/O
- 4. I/O
- 5. VCC
- 6. I/O

STYLE 13:

- PIN 1. GATE 1
- 2. SOURCE 2
- 3. GATE 2
- 4. DRAIN 2
- 5. SOURCE 1
- 6. DRAIN 1

STYLE 14:

- PIN 1. ANODE
- 2. SOURCE
- 3. GATE
- 4. CATHODE/DRAIN
- 5. CATHODE/DRAIN
- 6. CATHODE/DRAIN

STYLE 15:

- PIN 1. ANODE
- 2. SOURCE
- 3. GATE
- 4. DRAIN
- 5. N/C
- 6. CATHODE

STYLE 16:

- PIN 1. ANODE/CATHODE
- 2. BASE
- 3. EMITTER
- 4. COLLECTOR
- 5. ANODE
- 6. CATHODE

STYLE 17:

- PIN 1. EMITTER
- 2. BASE
- 3. ANODE/CATHODE
- 4. ANODE
- 5. CATHODE
- 6. COLLECTOR

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