Electrical Rules Check Report

Class	Document	Message
		Successful Compile for Lidar_board.PrjPcb

Design Rules Verification Report

Filename : C:\Users\fg4ng\AppData\Local\TempReleases\Snapshot\1\design_files\Lidar_

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('IC_ON_TSOP6'))	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('IC_ON_SOT23_5_CASE527AH'))	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('IC_ON_Micro8_CASE846A_02'))	0
Clearance Constraint (Gap=5mil) (InNet('USB_D_*') Or	0
Clearance Constraint (Gap=15mil) (All),(All)	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('CON_WURTH_microUSB_B_629_105_136_821') And	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('IC_FTDI_QFN32_5x5'))	0
Clearance Constraint (Gap=5mil) (All),(IsPad And (HasFootprint('IC_ON_TSOP5_SOT23_5_MA05BC') Or	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('T_ON_SOT353'))	0
Clearance Constraint (Gap=5mil) (All),(IsPad And HasFootprint('IC_ON_WDFN8_CASE511_BN'))	0
Clearance Constraint (Gap=5mil) (InNet('NetQ4_3')),(InNet('GND') Or InNet('NetC25_2'))	0
Clearance Constraint (Gap=5mil) (InNet('NetQ4_7') Or InNet('NetQ4_1')),(InNet('P3V3') Or InNet('NetC25_2'))	0
Clearance Constraint (Gap=20mil) (InNamedPolygon('GND_plane_L4') Or InNamedPolygon('GND_plane_L1')),(All)	0
Clearance Constraint (Gap=0mil) (HasFootprint('CON_WE_Redcube_WP_SMRA_746_631_3') And	0
Clearance Constraint (Gap=5mil) (InNet('NetU7_15')),(InNet('NetC36_1'))	0
Clearance Constraint (Gap=5mil) (InNet('NetU7_14') Or InNet('GND')),(InNet('NetU7_15') Or InNet('P5V_USB'))	0
Clearance Constraint (Gap=5mil) (TouchesRoom('Under_FPGA') Or	0
Clearance Constraint (Gap=5mil) (InNet('P3V3_USB') Or InNet('GND')),(InNet('USB_UART_RXD'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (HasFootprint('CON_WE_Redcube_WP_SMRA_746_631_3') And	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=80mil) (Preferred=30mil) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: thru_middle, thru_small, viaInBGApad) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=130mil) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=2mil) (HasFootprint('IC_ON_SOT563')),(InPadClass('All Pads'))	0
Minimum Solder Mask Sliver (Gap=3mil) (HasFootprint('IC_FTDI_QFN32_5x5')),(InPadClass('All Pads'))	0
Minimum Solder Mask Sliver (Gap=4mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=4mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Room Under_FPGA (Bounding Region = (5854mil, 4536.685mil, 6480.473mil, 5102.457mil) (False)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (InComponent('A2')),(InComponent('H2')	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (InComponent('SL')),(InComponent('P1')	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil) (InComponent('A1')),(InComponent('H1')	0
Component Clearance Constraint (Horizontal Gap = 10mil, Vertical Gap = 10mil) (All),(All)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Component Clearance Constraint (Horizontal Gap = 0mil, Vertical Gap = 0mil)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (Disabled)(All)	0
Silk primitive without silk layer	0
Total	0