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AND8468/D

A 60 W ac-dc Demonstrator with NCP1250

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APPLICATION NOTE

Housed in a tiny TSOP6 package, the NCP1250 lends itself very well to the design of moderate to high output power converters. Some features such as Over Power Protection (OPP) and internal Over Voltage Protection (OVP) make the part a component of choice for applications where high performance and cost must be combined. This application note demonstrates the part capabilities in a 60 W ac−dc adapter, typical of what is needed for the high−volume net/notebook market.

A Comprehensive Feature Set

Rather than jumping directly to the board description, it is interesting to enumerate the various features we have packed in this part. Generally speaking, the component operates in peak current mode control and switches at a constant frequency when the converter delivers its nominal power (65 kHz or 100 kHz). When the power goes down and hits around 20% of the nominal value, the frequency is linearly reduced down to 26 kHz typically as the load gets lighter. When the frequency reduction is over, the part enters skip cycle. This function will satisfy the designers looking for efficiency performance, especially in moderate output loading conditions. Please note that we have introduced a low−frequency jitter that the part keeps even when operated in frequency foldback. It will naturally help to soften the EMI signature even when the converter does not deliver its full output power.

To cope with Continuous Conduction Mode (CCM) designs, the part includes adjustable slope compensation via the inclusion of a simple series resistance with the current sense signal. Unlike other 6−pin devices, the level can be nicely tweaked to adjust the compensation level to the right value, without over or under compensating the converter as it is often the case with fixed internal settings. Finally, a 4 ms soft−start ensures a smooth start−up sequence and prevents the output from overshooting.

If there is one parameter that plagues most of the adapter designs, this is the maximum authorized power that the converter can deliver in fault condition. Beyond the authorized value, the power supply must be stopped. When the fault detection capitalizes on the collapsing of the auxiliary V_{CC} (as it was the case in past times), the exercise quickly turns into a nightmare especially with a poor coupling between the power and the auxiliary windings. When the fault is detected by monitoring the feedback level, as in the NCP1250 case, the situation improves. However, the line compensation circuitry, the so−called OPP which compensates for various propagation delays at high line, often destroys the no−load performance as it permanently offsets the current sense information with a portion of the bulk (high) voltage. The NCP1250 offers a solution that will ravish power supply designers by sensing the line input level via the negative swing naturally present on the auxiliary winding. Requiring two resistors only, the process is fully non−dissipative and does not hamper the performance in no−load conditions. Combined with the naturally−low propagation delay of the NCP1250, the OPP performance is excellent as confirmed by the values collected on the prototype.

Adapters must also include some typical protections such as Over Voltage Protection and Over Temperature Protection (OTP). When one of these events occurs, the part must immediately latch off. This is the case with the NCP1250 where the latch input is easily accessible via pin 3. When activated, the device stays latched until someone resets the converter by un−plugging the power cord. Thanks to a simple arrangement made of one Zener diode and a Negative Temperature Coefficient (NTC) component, the demonstration board fully complies with the protection requirements for most of the ac−dc adapter designs.

Finally, if controller self−supply is often a problem for designers, this potential issue goes away with the NCP1250. The wide V_{CC} voltage range, from 9 to 28 V lets you think of a transformer without caring too much about the auxiliary and power windings coupling coefficient. If the leakage inductance creates large V_{CC} variations within the converter output range, the 28 V upper V_{CC} limits gives a comfortable operating margin and will let you focus on other more important design parameters.

Further to this part description, it is time to explore the demonstration board schematic.

December, 2010 − Rev. 2

Publication Order Number:
AND8468/D

The Adapter Schematic

The adopted schematic appears in Figure 1. You can see the NCP1250 surrounded by components whose roles are to perform the functions detailed in the above lines. Let us start the description by the left side of the board.

The mains is applied on the rectifying diode bridge through an EMI filter made of a 10 mH common−mode choke. Its leakage inductance is used together with C_{11} to form a differential mode filter. A resistors string (R_{15}, R_{17} and R_{20}) ensures the discharge of this capacitor when the power cord is un−plugged. These resistors must be carefully calculated to fulfill the IEC−950 safety standards as they can obviously hamper the no−load standby power. Additional filtering and protection devices can be necessary (VDR, spark−gaps) to improve the filter as you start qualifying the final prototype for safety and surge robustness.

The controller drives a 6 A / 600 V power MOSFET where a small PNP transistor helps to strengthen the turn−off event for an improved efficiency.

Start−up and Self−Supply

The start−up network benefits from the very low current consumption of the NCP1250. With a 15 μA maximum current, the part can be cranked with a weak start−up current which is good for the standby power. By connecting the start−up network made of R_2, R_3 and R_7 to the half−wave−rectified mains, the dissipation on this network is reduced compared to a direct connection on the bulk capacitor. Furthermore, in case of a latched event, the V_{CC} on the part will collapse at a faster pace when the user un−plugs the converter as no additional current can maintain the V_{CC} capacitor voltage on the controller. This is different from a situation where the bulk capacitor is slowly discharged at power−off and maintains the voltage on the V_{CC} capacitor for a long time before the reset occurs. In our case, the resistors have been calculated following the data−sheet guidelines. They ensure the lowest static consumption while keeping the start−up sequence below 3 seconds at the lowest input line. We have tested the start−up sequence with the board delivering 3 A while powered from a 85 Vrms input voltage (Figure 2). In this worst case, the time at which the full output voltage is ready remains below the 3 s limit, giving some margin for the nominal case at 100 Vrms. Please note that the various leakages to earth brought by the oscilloscope and other active loads have to be minimized during this test to avoid altering the start−up time.

The start−up sequence is linked to the V_{CC} capacitor value. A small value will bring a short start−up time but can possibly engender a hiccup at power−on. A sufficient level of energy must be stored in this capacitor as it is the only source of energy at power−on before the auxiliary winding takes over the controller supply. In the NCP1250, the reason why the Under Voltage Lock Out (UVLO) has been placed high enough is to increase the available CV^2 term. This helps to lower the storage capacitor value while improving the start−up time. Unfortunately, in these low−standby power supplies, the recurrence of the switching pulses in light load conditions can be very long. In this situation, as the refresh of the V_{CC} capacitor is made by bunches (the part operates in skip cycle) there are chances that the V_{CC} level slowly goes down until it touches the UVLO low level of the part which initiates a new start−up sequence. If we grow the V_{CC} capacitor, the start−up time will suffer. A possible solution is that described in Figure 3. It consists in splitting the capacitors and isolating them via a simple diode.

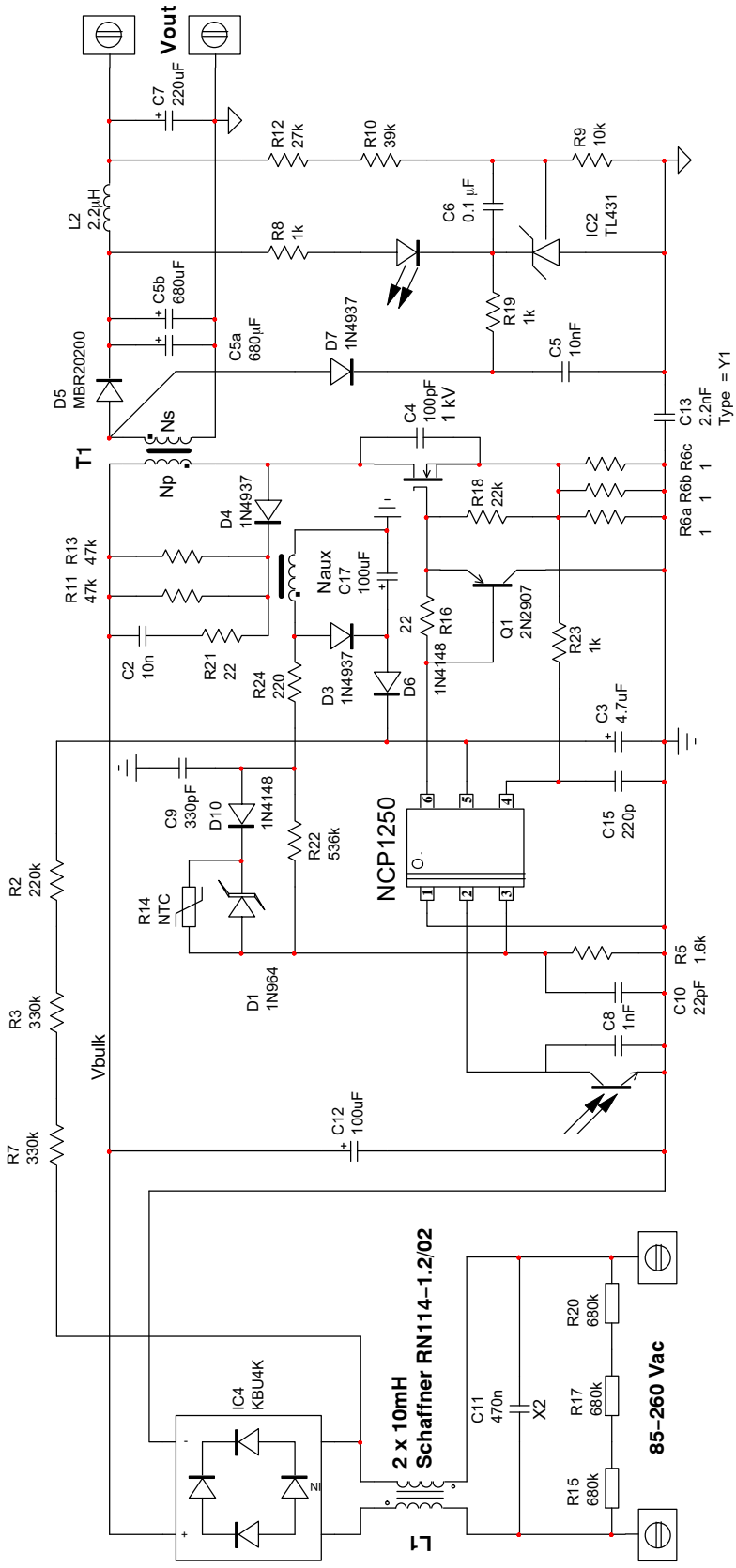


Figure 1. The Adapter Uses All the Features Brought by the NCP1250 to Implement a High−Performance 60 W Converter

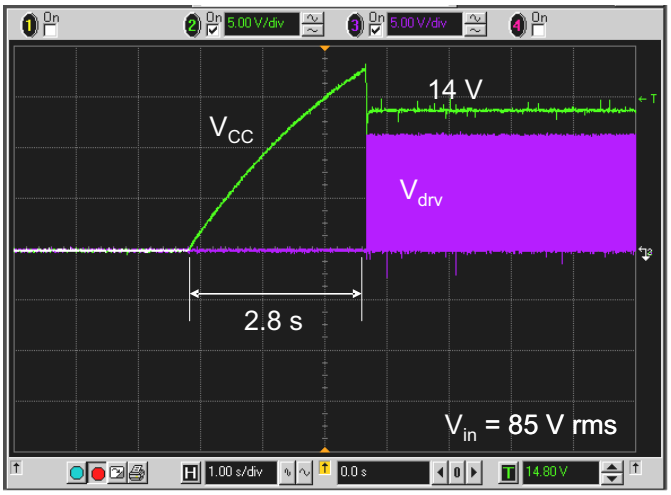


Figure 2. The Start−up Sequence is Below 3 s When Powered from a 85 Vrms Input Voltage While Delivering 3 A

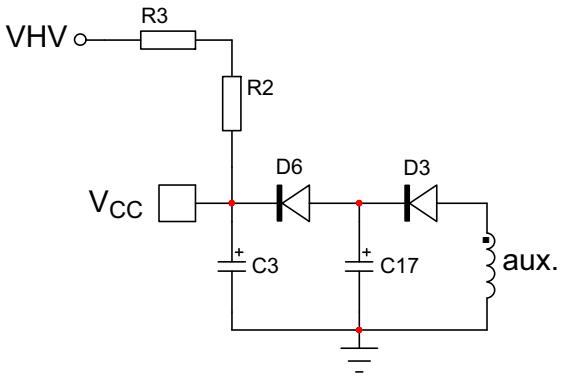


Figure 3. The Split Supply Lets You Power the Controller with a Small V_{CC} Capacitor, Decoupled from a Larger Value Directly Connected to the Auxiliary Winding

In this case, the start−up time involves C_3 only as D_6 decouples the discharged capacitor C_{17} from the charging circuit. When the auxiliary winding charges C_{17}, the voltage across its terminals increases until it completely supplies the controller. In standby, the circuit is decoupled by a capacitor equal to $C_3 + C_{17}$, enough to maintain the V_{CC} in light to no load operations. In the application board, we have successfully tested a 4.7 μF value for C_3 and a 100 μF capacitor for C_{17}.

The start−up sequence also involves the internal 4 ms soft−start. During this time, the peak current setpoint is linearly increased from a very low value up to the allowable maximum. This soft−start circuitry is activated upon a fresh start−up but also every time a restart is attempted, e.g. in an auto−recovery fault mode.

Protections

There are several protections required by ac−dc adapters for the notebook market. They are listed below:

1. Short Circuit Protection, SCP: the adapter must sustain a permanent short−circuit on its output without being destroyed. When the fault has disappeared, the adapter must recover from the protection mode and deliver the rated power again.
2. Over Voltage Protection, OVP: in case the loop is broken, e.g. the optocoupler is destroyed or the TL431 divider network is affected, the adapter must be immediately stopped and remain in that state until the user cycles the input power for reset.
3. Over Temperature Protection, OTP: if the temperature of the adapter exceeds a certain ambient value, there is a risk of destruction. To avoid this from happening, a thermal sensor permanently monitors the temperature and in case it exceeds the limit set by the designer, the adapter shuts down permanently. Again, the adapter is reset when the user cycles the input power and the temperature has decreased.
4. Over Power Protection, OPP: for some power supplies, it is important that the maximum output current stays in control in worse case conditions, e.g. when the load is drawing more current that what it should, without being a real short−circuit. In our design, the nominal output current is 3.2 A and must stay below 4.5 A in all input voltage conditions.

Let us know check how each requirement has been separately addressed.

Short−Circuit Protection

The protection is ensured by monitoring the current sense signal on pin 4. When this voltage exceeds the maximum internal current setpoint (0.8 V without OPP signal or less when OPP is active), the internal 100 ms timer is started. The timer is reset if the current sense signal goes back below the maximum internal current setpoint. If the timer completes its cycle, meaning the fault has been present longer than 100 ms, all driving pulses are immediately stopped and the part reduces its consumption to around 1 mA. As the V_{CC} decreases, it eventually touches the UVLO low level of 8.9 V where the part re−enters the start−up mode: V_{CC} rises up again and when reaching 18 V, the circuit pulses, attempting to re−start. A kind of auto−recovery burst mode takes place, ensuring a low average input power. There are two cases that we can think of:

1. when the auxiliary and the power winding are well coupled, a short−circuit on the secondary side, very close to the board output, also collapses the auxiliary winding on the primary side. As a result, the internal timer does not have time to reach completion and the pulses are interrupted by the UVLO level. This is what Figure 4 shows you with a burst of 17/205 = 8.3%.

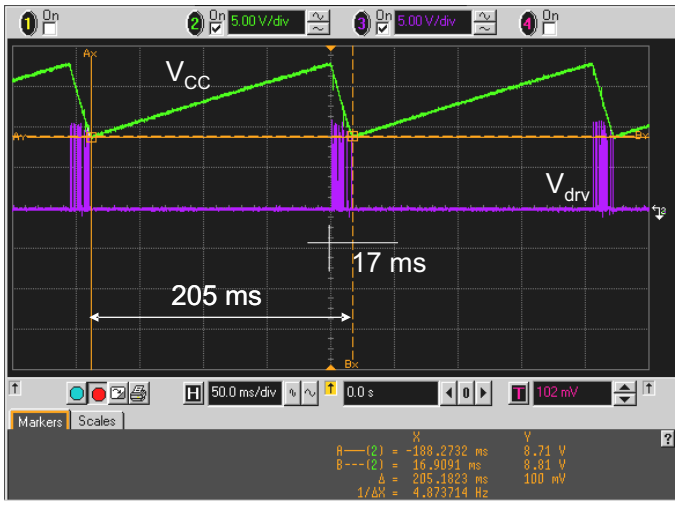


Figure 4. The Auxiliary Winding Collapses in Presence of a Short−Circuit at the Board Output. The Duty−Ratio in Burst Mode is Rather Low, Implying a Weak Averaged Power on the Input

2. when the short−circuit is applied at the end of the cable, there are chances that the auxiliary voltage does not collapse, keeping the controller alive despite an over current on the secondary side. The timer can therefore count up to 134 ms (typical) and make the part enter auto−recovery as before however with the longer recurrence. This is what Figure 5 shows. Again, a low duty−ratio in burst mode guarantees a low average input power (0.13/1.3 = 10%).

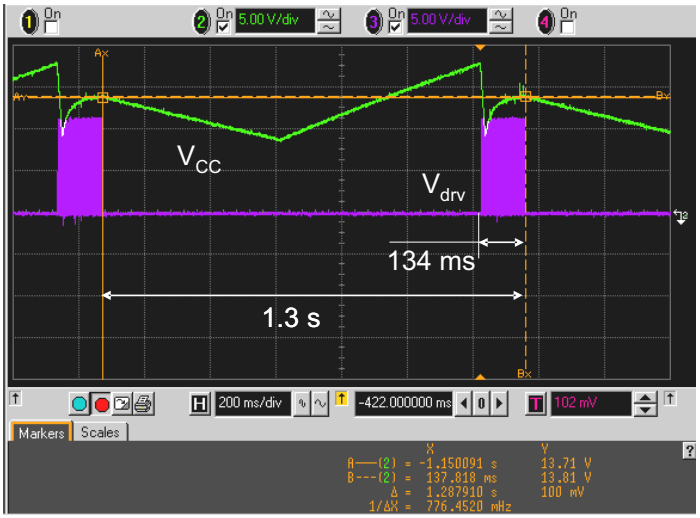


Figure 5. In This Case, the Timer Interrupts the Switching Pulses after 100 ms and the Part Enters Auto−Recovery

Over Voltage Protection

When the optocoupler is broken or when the TL431 divider network is affected by a severe drift (or one of its resistor is missing or features a wrong value), then the output voltage can escape from the limits imposed by the specifications: this is an over voltage condition. In the majority of cases, this condition is considered hazardous for the downstream load and the adapter must completely shut off. The NCP1250 features a dedicated input for this purpose, pin 3. Without entering into its implementation details, the pin actually combine two functions which are Over Power Protection (see below) and latch input. The latch input works by observing the level on pin 3 after the power MOSFET has been turned off. If the voltage on this pin exceeds 3 V four consecutive times, then the part permanently latches off. The latch is maintained by an internal SCR which vigorously puts the V_{CC} pin down to around 7 V. The part then stays latched as long as the injected current keeps above 30 μA. If the current passes below this value, the part is reset. To avoid the reaction to spurious signals, a 1 μs delay is inserted before observing pin 3 after the power MOSFET has been turned off.

As pin 3 combines the OPP function with a negative bias, we shall not disturb it during the on time with a positive

level. Therefore, our OVP circuit must stay transparent when the power switch is activated but must trip the latch, if necessary, during the off time only. In order to inject a dc signal during the off time, the simplest way is to use the auxiliary winding and a Zener diode. The winding swings to $-(N_{aux}/N_P)V_{in}$ during the on time and to $-(N_{aux}/N_S)V_{out}$ during the off time. In these equations $-(N_{aux}/N_S)N_P$ respectively refer to the turns on the auxiliary, secondary (power) and primary windings. Figure 6 portrays an arrangement of resistors and capacitors around pin 3 that meet the OVP biasing requirements. First, a simple RC filter is installed on the signal path to filter out unwanted signal and calm down the high dV/dt naturally present on the auxiliary signal. The negative signal for OPP is routed via R_{22}/R_5. However, as the Zener diode could also be forward biased by the negative signal naturally present on the auxiliary winding, the series diode D_{10} provides the necessary isolation during the on time. During the on time, pin 3 only receives a portion of the negative signal through R_{22}/R_5 while the Zener diode D_4 stays silent. When an OVP event occurs, the voltage increases during the off time only until the 3 V level is reached and exceeded during 4 consecutive clock cycles. At this point, the NCP1250 latches off by stopping all pulses and vigorously pulling down its V_{CC} pin.

We have captured several oscilloscope shots to illustrate the behavior of the circuit. Figure 7 displays the signal collected on pin 3 of the controller, in lack of OVP event (normal operation). The signal is clean, despite a rather large overshoot at turn off, due to the various parasitic capacitances on the signal path. As can be seen, the amplitude is still small with a 100 mV/div vertical scale. Also, the controller includes a 1 μs blanking window that shields the adapter against adverse trips.

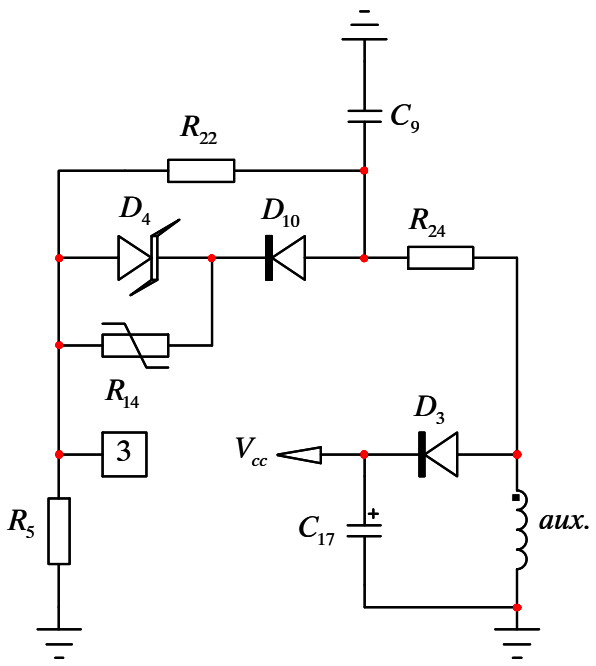


Figure 6. A Zener Diode Activates When the Auxiliary Level is Out of Range and Trips the Internal Latch

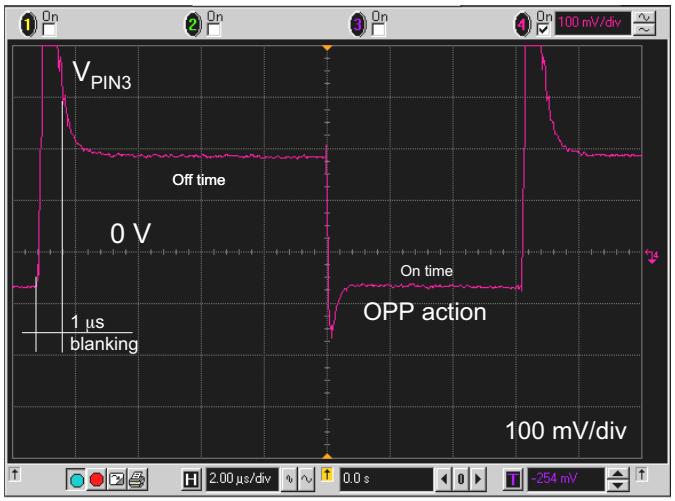


Figure 7. The Signal on Pin 3 Shows Some Overshoots Given the High dV/dt on the Auxiliary Winding. However, They Remain of Low Amplitude (100 mV/div) and are Internally Ignored Due to a 1 µs Blanking Window.

On the contrary, Figure 8 shows an oscilloscope shot where the optocoupler LED has been purposely short−circuited. At the point of the event, we can see the rectified auxiliary voltage (the V_{CC} level) together with pin 3 voltage building up. Please note that the growth is only positive as it should be. When the total voltage reaches the Zener level (15 V) plus the latch−off threshold (3 V), the part permanently stops pulsing. It is around 18 V on the auxiliary V_{CC}.

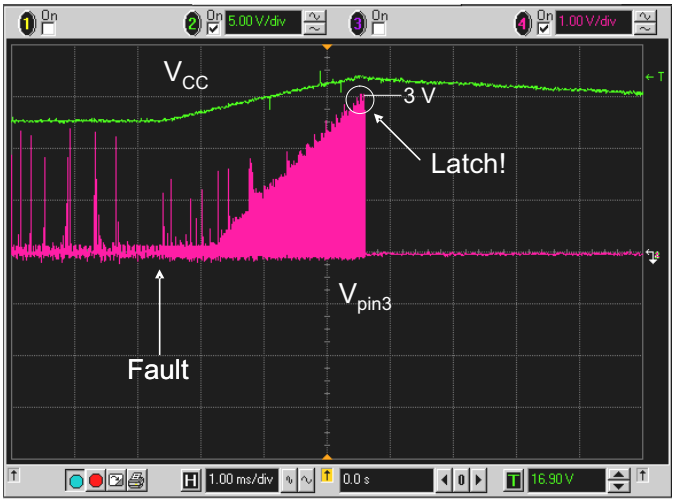


Figure 8. An OVP Has Been Triggered. The Voltage Only Grows Positively (the Negative OPP Signal is Not Affected) Until the 3 V Level is Reached. At This Point, the Controller Latches Off.

Over Temperature Protection

OTP can be implemented by connecting a Negative Temperature Coefficient resistor (NTC) across the Zener diode. This is what is shown in Figure 6. In this position, when the temperature increases, the NTC resistor starts to decrease and lifts up pin 3 voltage. Thanks to diode D_{10}, this lift is only positive. When the level reaches 3 V, the part simply latches off and requires a reset before re−start. Reset occurs when the user cycles the input voltage.

We have selected an NTC type from Vishay, exhibiting a 100 kΩ resistor value at room temperature (25°C). Since we would like the adapter to enter over temperature protection at an ambient of 100 °C, what is the NTC resistor value at this point? According to the specifications, it is 5.8 kΩ. As the auxiliary voltage plateaus to 14 V during the off time, what value should be the pull−down resistor R_5 on Figure 6? Considering a 0.6 V forward drop for the diode D_{10} and a latch−off level of 3 V, the voltage across the NTC in fault mode must be:

$$V_{NTC} = 14 - 3 - 0.6 = 10.4\ V \qquad \text{(eq. 1)}$$

Based on the 5.8 kΩ NTC resistor at 100°C, the current inside the device must be:

$$I_{NTC} = \frac{10.4}{5.8k} \approx 1.8\ mA \qquad \text{(eq. 2)}$$

As such, the bottom resistor R_5, can easily be calculated to develop 3 V when a current given by Equation 2 circulates:

$$R_5 = \frac{3}{1.8m} \approx 1.6\ k\Omega \qquad \text{(eq. 3)}$$

We tested the demonstration board with the calculated setup and the test revealed a trip point around 103°C, close to what was expected. The precision on this trip point depends on the auxiliary voltage precision of course, but also on the circulating current in fault mode. We recommend selecting NTC types which show a resistor at the trip point rather low in order to force a decently low pull−down resistor R_5. A low value for R_5 helps to improve the noise immunity and limits the leakage effects in the OPP pin at high temperature.

Over Power Protection

A current−mode power supply works by setting the inductor peak current according to the output power demand. The inductor current is transformed into a voltage by a sense resistor, R_6 in our adapter. The peak current setpoint depends on the error voltage delivered on the feedback loop pin. In our adapter, this is the current forced by the TL431 on the secondary side and reflected to the primary over pin 2 of the NCP1250. As detailed in the data−sheet, the current setpoint inside the circuit depends on pin 2 level divided by 4.2. In fault conditions, when the loop is lost, the feedback level can go up to 5 V. To avoid any current runaway, the maximum voltage setpoint is safely clamped to 0.8 V. In that case, the maximum peak current in the inductor cannot exceed:

$$I_{Lp,max} = \frac{V_{limit}}{R_6} \qquad \text{(eq. 4)}$$

With three paralleled 1 Ω resistors, we expect a maximum peak current to be:

$$I_{Lp,max} = \frac{0.8}{0.33} = 2.4\ A \qquad \text{(eq. 5)}$$

Unfortunately, the observed peak current depends on several factors among which the total propagation delay plays an important role. The propagation delay t_{prop} is the total time taken by the control chain to bring the MOSFET gate down when the peak current limit has been reached. Obviously, before the turn−off order propagates to the MOSFET gate, the peak current keeps rising. Equation 4 must thus be updated to the following one:

$$I_{Lp,max} = \frac{V_{limit}}{R_6} + \frac{V_{bulk,max}}{L_P} t_{prop} \qquad \text{(eq. 6)}$$

The control chip, alone, is rather fast: 100 ns typically. However, the drive capability and the series drive resistors naturally hamper the turn−off time. Typical total propagation delays are therefore in the vicinity of 250 ns − 300 ns. Back to Equation 5 and considering a rectified voltage $V_{bulk,max}$ of 370 Vdc (265 Vac input), the inductor peak current becomes:

$$I_{Lp,max} = \frac{0.8}{0.33} + \frac{370}{600\mu} 350n = 2.4 + 0.22 = 2.6\ A \qquad \text{(eq. 7)}$$

This 200 mA difference represents a theoretical 8.3% peak current increase compared to the original calculation. On the adapter, we have measured the maximum output current that can be delivered at low and high line conditions. The results appear below:

V_{in} = 120 V, $I_{out,max}$ = 4.1 A
V_{in} = 370 V, $I_{out,max}$ = 5.7 A

As you can read, the power dispersion goes up to 108 W versus 78 W at low line. The 8.3% peak current increase cannot, alone, justify this difference. The explanation lies in the operating mode change between high line and low line. In Continuous Conduction Mode (CCM), at low line, we store the following energy:

$$E_P = \frac{1}{2} L_P \left(I_{peak,max}^{\ 2} - I_{valley}^{\ 2} \right) \qquad \text{(eq. 8)}$$

However, at high line, the peak current is indeed slightly increased by 8.3% but because the off−time has expanded, the valley current I_{valley} is much smaller than at low line: we are going into the Discontinuous Conduction Mode. If I_{valley}^2 also goes down in Equation 8, you naturally store more energy into the inductor and the output power runs away. This situation is obviously not acceptable and a means has to be found to harness this available power.

The easiest way to reduce the delivered power at high line is to act upon the maximum peak current setpoint. There are several ways to do that, however, all of the known methods are either dissipative (direct bulk connection) or they affect the standby power with a permanent offset. The proprietary technique adopted in the NCP1250 differs from the above by offering a unique non−dissipative compensation method that does not hamper the standby power. Figure 9 discloses the adopted circuitry. In this application, a portion of the negative swing present on the auxiliary winding (D_3 anode) negatively biases pin 3 via a resistive divider made of R_{22} and R_5. The collected voltage is then directly added to the internal 0.8 V reference voltage. In other words, at low line, the negative level on pin 3 is weak and the 0.8 V setpoint is barely affected. On the contrary, at high line, the generated negative voltage on pin 3 directly subtracts from the reference voltage and contributes to lower it. The amount of decrease can be scaled through the divider network division ratio.

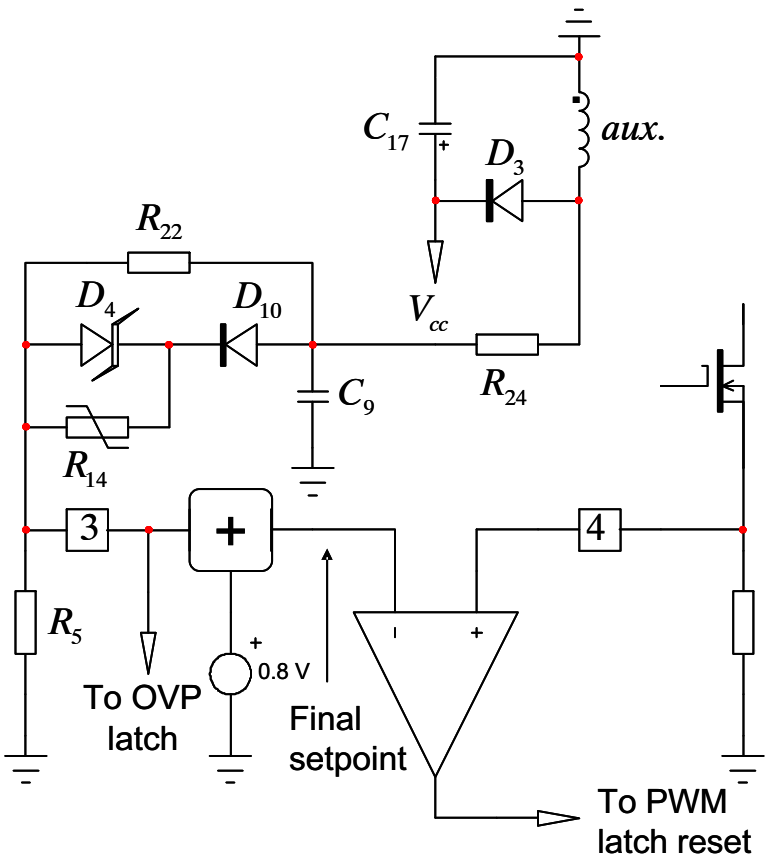


Figure 9. The Negative Voltage Present on Pin 3 is Simply Added to the Internal Reference Voltage to Create the Final Setpoint.

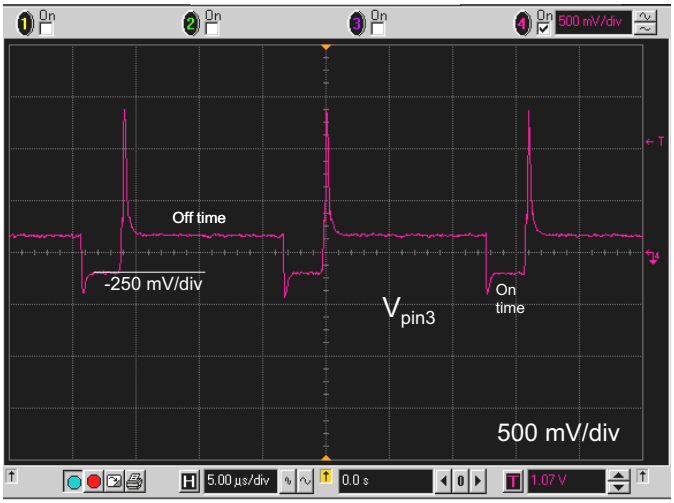


Figure 10. Pin 3 Signal Swings Negatively During the On Time. This Voltage is Directly Subtracted from the Internal 0.8 V Voltage Reference to Create a Reduced Setpoint.

The calculation of the OPP resistors, R_{22} and R_5, is rather straightforward. If you combine the OPP with the OTP and OVP as exemplified above, R_5 is imposed. It is 1.6 kΩ in our case. Suppose we need a 250 mV decrease from the 0.8 V set point. The transformer exhibits a turns ratio N_{aux}/N_P of 0.18. With a 375 V input (maximum value), the voltage swing on the auxiliary anode is:

$$V_{anode} = -(N_{aux}/N_P)V_{in,max} = -0.18 \times 375 = -67.5\ V \quad \text{(eq. 9)}$$

Considering the −250 mV of OPP, we need to drop over R_{22} a voltage of:

$$V_{R22} = 67.5 - 0.25 = 67.25\ V \qquad \text{(eq. 10)}$$

The current circulating the pull down resistor R_5 with a 250 mV bias will be:

$$I_{R5} = \frac{250m}{1.6k} = 156\ \mu A \qquad \text{(eq. 11)}$$

Combining Equations 10 and 11, we have:

$$R_{22} = \frac{67.25}{156\ \mu A} = 431\ k\Omega \qquad \text{(eq. 12)}$$

In the application board, the selected resistor will be a 536 kΩ. A typical signal as applied on the OPP pin is displayed in Figure 10. The 375 Vdc bulk voltage generates a −250 mV dc level during the on−time event. As the resistors installed on the auxiliary winding are of rather high values, the dissipated power is small and does not hamper the standby power. Furthermore, since we decrease the maximum peak current setpoint only, the skip level remains untouched, leading to a very good efficiency in light load conditions. We have carried new measurements of maximum currents over the demonstration board once the OPP circuitry has been put back in place. We found the following values:

V_{in} = 120 V, $I_{out,max}$ = 3.8 A
V_{in} = 370 V, $I_{out,max}$ = 4.1 A

Needless to say that these numbers are simply excellent. They confirm the good performance brought by the proprietary principle implemented in the NCP1250.

In designs where no OTP has to be implemented, we recommend to fix R_5 to 1 kΩ. Higher impedances could lead to leakages at high temperatures. Values up to 3 kΩ are acceptable.

Driving the Power MOSFET

The driving capability of the NCP1250 remains reasonably high given the size of the component. The demonstration board hosts a 6 A device. To speed−up the turn−off time and reduce the driving losses, we have installed an inexpensive PNP transistor, Q_1, to help pulling the gate to ground. Figure 11 shows the adopted scheme, rather classical: when the DRV pin is low, Q_1 conducts and actively pulls the gate down. When the DRV pin is high, Q_1 remains silent. R_{18} ensures the MOSFET is turned off in case the controller is not properly wired in the production chain. The turn−off event is extremely fast, as shown in Figure 12.

As the V_{CC} voltage of the NCP1250 can go as high as 28 V, it is important to limit the gate−source voltage to a level well below 20 V. The vast majority of MOSFET data−sheets state a $R_{DS(on)}$ measured at a 10 V V_{GS}. No need to over bias the MOSFET, beyond 10 V, the reduction in the $R_{DS(on)}$ would not be substantial. For this reason, the NCP1250 safely limits the excursion of the driving voltage to 12 V typically when V_{CC} is high. Figure 13 portrays a scope shot obtained when V_{CC} was purposely set to 20 V.

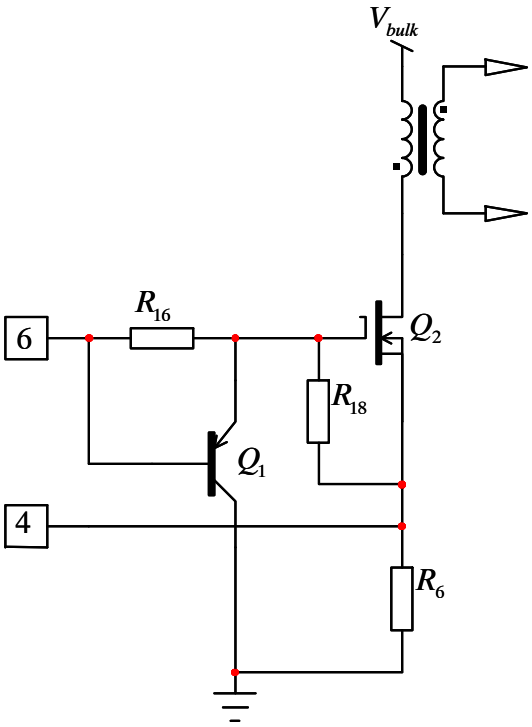


Figure 11. A Simple PNP Placed Across the Source and the Gate of the MOSFET Helps to Accelerate the Turn−off Time.

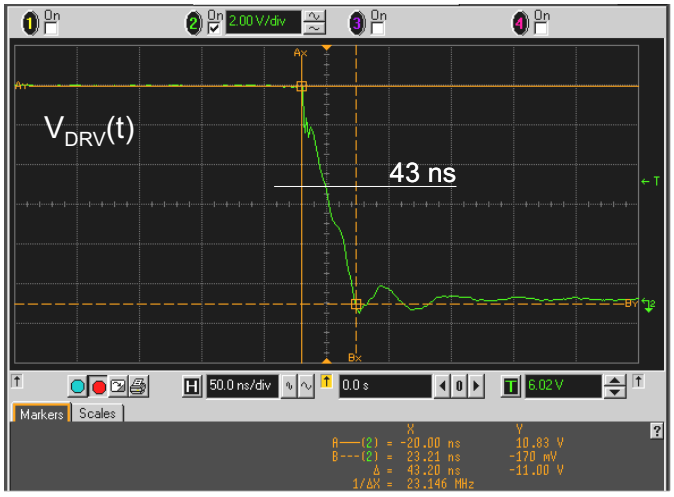


Figure 12. The PNP Presence Clearly Benefits to the Turn−off Event.

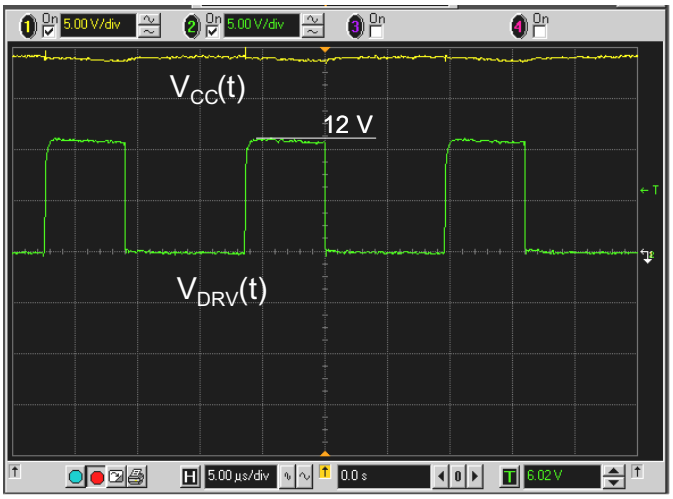


Figure 13. The Gate−Source Voltage is Safely Clamped to 12 V Typical, Protecting the MOSFET in Case of High V_{CC} Values.

For this 60 W adapter, we have selected a NDF06N60Z, a 6 A / 600 V device from ON Semiconductor. The component exists in a TO−220 fully isolated version and avoids using an isolator between the tab and the heatsink.

The Secondary Side Feedback

The feedback is made around a classical TL431 network. We used the automated spreadsheet to evaluate the component values based on 1 kHz bandwidth target. A thorough description of the method is given in Ref. [2]. In an effort to further decrease the no−load standby power, we have implemented a proprietary technique around the TL431. As you well know, the data−sheet specifies a minimum biasing current of 1 mA. Usually, this minimum bias is ensured by paralleling a 1 kΩ resistor with the optocoupler LED which exhibits a 1 V forward drop. If this extra current plays a positive role in the converter performance at high output levels, it is obviously detrimental to the standby power since it permanently draws 19 mW in our 19 V example. The idea is to get rid of this bias in standby mode, without affecting the transient response in case the load is suddenly re−applied. Figure 14 shows you the idea we came up with. The principle is extremely simple: the capacitor C_5 delivers a voltage equal to that of the output at full load, i.e. 19 V. These 19 V are used to bias the TL431 via R_{19}. As the load is getting lighter, the controller enters the skip cycle mode. Given the time constant offered by C_5 together with the load made of R_{19} and the TL431 bias, the voltage across C_5 cannot be maintained: its average value collapses and the TL431 bias disappears. In case the load is suddenly re−applied, the bias is automatically regenerated as the controller expands the duty−cycle and the response is not affected. With a 19 V output, this technique helps to save roughly 40 mW seen from the primary side. Please note that the authorization of using this patented bias suppression technique is only granted to customers using ON Semiconductor PWM controllers.

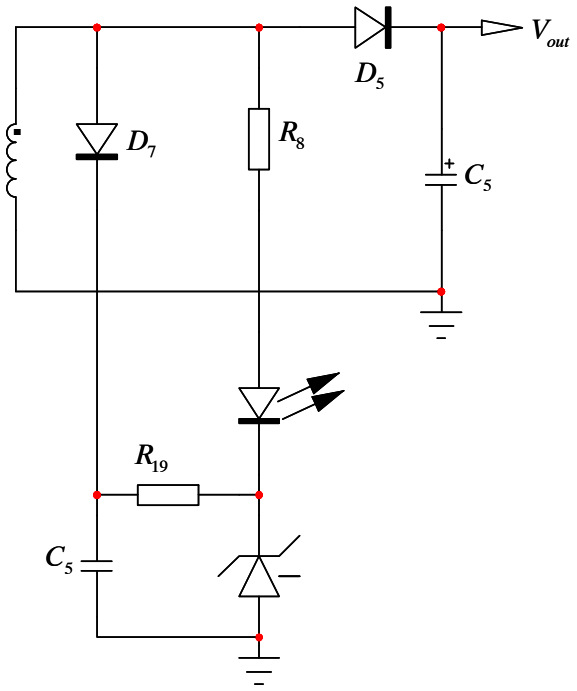


Figure 14. A Simple Peak Rectifier Generates a Voltage Across C5 Whose Amplitude Falls Down as the Controller Starts to Skip Cycle.

The Transformer

The transformer we have used is made of a PQ26/25. The turns ratio was computed to offer a 15% safety margin on the MOSFET maximum voltage. Since we used a 600 V device, the turns ratio can be computed as described in Ref. [1]:

$$N = \frac{k_c\left(V_{out} + V_f\right)}{BV_{dss}k_D - V_{os} - V_{bulk,max}} \quad \text{(eq. 13)}$$

In this equation:

k_c is the distance between the clamp voltage and the reflected voltage. For a k_c of 1, the clamp voltage equals the reflected voltage and the dissipation is infinite. If k_c is too high, then you lose dynamics on the drain voltage and crop the safety margin. Reasonable values range from 30% to 60%. For this design, we will set it to 1.5.

k_D represents the derating factor for the MOSFET. We usually set it 15%, which, applied to a 600 V MOSFET limits the maximum allowable voltage to 600 x 0.85 = 510 V.

V_{os} expresses the natural overshoot brought by the clamp diode. It can be as high as 20 V and must be carefully accounted for in the turns ratio selection.

V_{out} and V_f are respectively the output voltage and the secondary diode forward voltage.

$V_{bulk,max}$ in a universal mains application can reach up 375 Vdc.

Applying the above values in Equation 13, we find the following turns ratio:

$$N = \frac{1.5 \times (19 + 0.6)}{600 \times 0.85 - 20 - 375} = 0.255 \quad \text{(eq. 14)}$$

We will choose a turns ratio of 0.25, $N_P : N_S$ = 1:0.25. Looking for a 13 V auxiliary V_{CC}, the turns ratio of the auxiliary winding is simply:

$$N_P : N_{aux} = \frac{13.6}{19}\frac{N_P}{N_S} = \frac{13.6}{19} \times 0.25 \approx 0.18 \quad \text{(eq. 15)}$$

Based on this turns ratio, the secondary diode is going to see the following Peak Inverse Voltage (PIV) at high line (265 Vrms):

$$PIV = \left(\frac{N_S}{N_P}\right)V_{bulk,max} + V_{out} \quad \text{(eq. 16)}$$

$$= 0.25 \times 375 + 19 = 112\ V$$

Considering a 100%−derating factor, we selected a 200 V diode. Given the dc output current of 3 A, a MBR20200 in TO−220 has been chosen.

The primary inductor has been selected to make the converter operate in CCM at low line and enter DCM at high line in moderate loading conditions. We calculated a primary inductor of 600 μH. The transformer construction details are available at the end of this application note.

Efficiency Performance

The NCP1250 excels in terms of efficiency and standby power. We have made a series of tests on the proposed adapter, carried at both high and low lines. The results appear below. They include a 1.2 m long cable from the adapter to the load.

Output Power	Efficiency – V_{in} = 100 Vrms (%)	Efficiency – V_{in} = 230 Vrms (%)
15 W – 25%	89.11	87.91
30 W – 50%	88.95	88.76
45 W – 75%	88.54	89
60 W – 100%	87.47	89
Average efficiency	88.52	88.67

NO−LOAD STANDBY POWER

Output Power	Input Power – V_{in} = 100 Vrms (mW)	Input Power – V_{in} = 230 Vrms (mW)
0	40	87

LIGHT LOAD EFFICIENCY

Output Power	Input Power – V_{in} = 100 Vrms (W)	Input Power – V_{in} = 230 Vrms (W)
0.5 W	0.68	0.74
0.7 W	0.91	0.98

The performance is linked to the combined action of the frequency foldback and the skip cycle operation at constant peak current. Please note that the no−load standby power includes the 2 MΩ discharge resistors string placed across the X2 capacitor on the input filter. These numbers are excellent considering a low−voltage controller featuring a start−up network.

Transient Response

The loop small−signal response has been measured and is the object of a dedicated application note. Please refer to Ref. [2] for more details. Loop stability is an important matter and must be seriously considered when working on high−volume projects. No trials and errors in the laboratory while observing the transient response, please! J However, once the loop has been thoroughly reviewed and analyzed, some transient tests can be performed to check that everything is ok. In our case, the output has been loaded by a current step from 0.1 A to 3.5 A with a slew−rate of 1 A/μs. Two input voltages have been considered, 100 Vrms and 230 Vrms. Such a wide loading step is a quite stringent test but as shown in Figure 15, the response at the board level stays within 1.6% of the nominal voltage of 19 V.

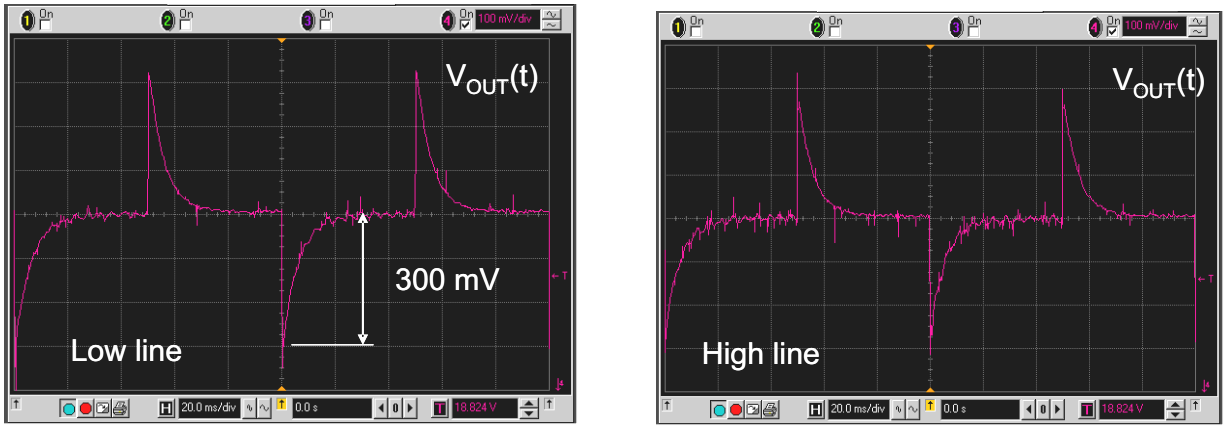


Figure 15. The Transient Response at Low Line and High Line Are Almost Identical and Do Not Show Signs of Instabilities

Conclusion

This application note describes how an ac−dc converter meeting all new efficiency challenges can be built with the new NCP1250. Despite a small TSOP−6 package and a limited amount of pins, the performance of the final board nicely competes against other more complex circuits by offering a similar set of options plus some unique features such as the non−dissipative OPP circuit. This makes the part the ideal candidate where space constraints, performance and cost sensitivity have to be combined.

References

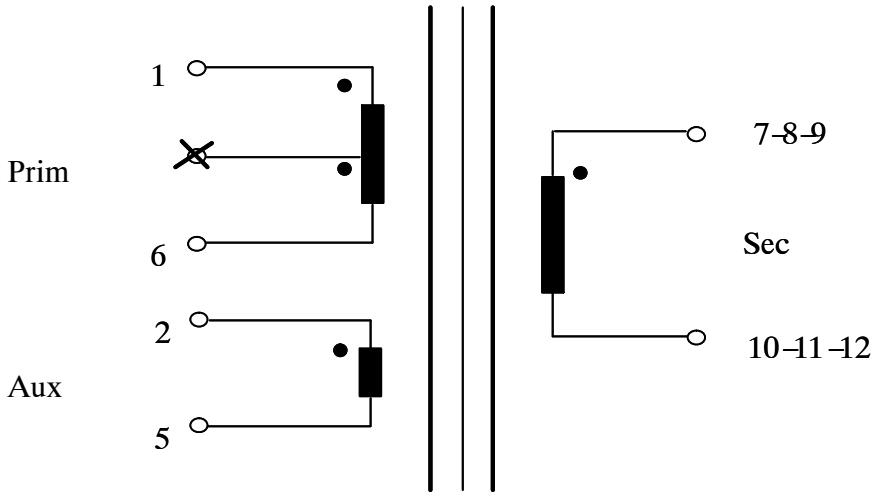
1. C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw−Hill, 2008
2. AND8453, “Loop Control Design of an ac−dc Adapter Using the NCP1250”, www.onsemi.com

1APPENDIX I – TRANSFORMER CONSTRUCTION DETAILS

Table 1. BILL OF MATERIAL

Description & Reference	Material
Bobbin PQ26/25 12 pins ref. TDK BPQ26/25−1112CP	FR phenol − Pin material: steel wire (solder plated)
Core PQ26/25 ref. MAGNETICS 0_42625UG A_L = 310 nH/T^2	Ferrite P material
Wire Ø0.50 mm, MAGNESOL UN180, ESSEX	Enameled copper 2UEW, thermal class 180°C
Wire Ø0.30 mm, MAGNESOL UN180, ESSEX	Enameled copper 2UEW, thermal class 180°C
Wire Ø0.50 mm, **triple−insulated wire** RUPATEX B	Enameled copper + 3 ETFE−insulated layers
Adhesive film thickness : 50 μm ref. VON ROLL 51587	Polyester
Varnish ref. DOLPHS AC−46	Polyurethane

Electrical Diagram



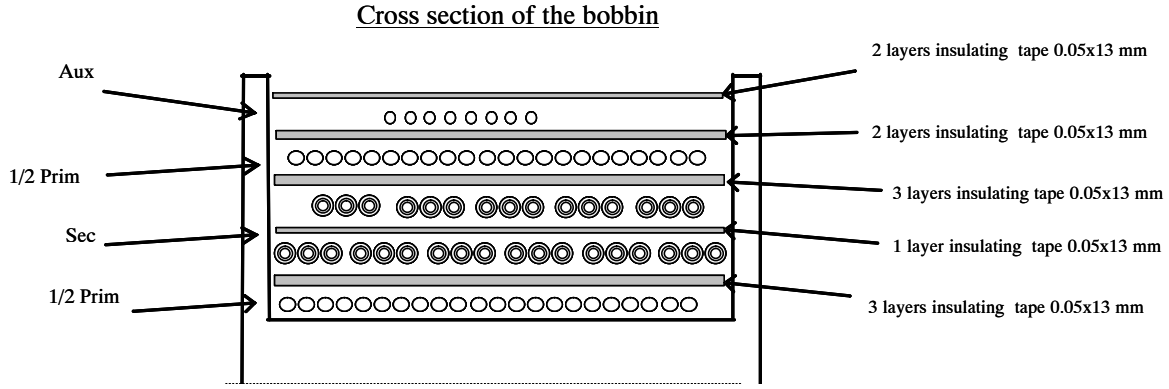
Winding Characteristics

Table 2. WINDING INSTRUCTIONS

Windings	Start	Finish	N (turns)	wire n x Diam.	Total Section	Details
1/2 Prim	1	3	22	1 x 0.50 mm 2UEW, therm. cl. H	0.1963 mm^2	Final insulation: 3 polyester layers, thick.: 50 μm
Sec	7−8−9	10−11−12	11	3 x 0.50 mm TEX−E, therm. cl. B	0.5890 mm^2	Trifilar winding. 1 layer polyester thick.: 50 μm onto first winding layer. Final insulation: 3 polyester layers, thick.: 50 μm
1/2 Prim	3	6	22	1 x 0.50 mm 2UEW, therm. cl. H	0.1963 mm^2	Final insulation: 2 polyester layers, thick.: 50 μm
Aux	2	5	8	1 x 0.30 mm 2UEW, therm. cl. H	0.0707 mm^2	Final insulation: 2 polyester layers, thick.: 50 μm

Notes:

Winding Assembly Diagram



Assembly and Special Treatment

- Core is assembled with adhesive polyester film, thickness: 50 μm, width: 10 mm, A_L=310 nH/T^2, center−leg gapped.
- Pin n°3 cut at welding level.
- Assembly “bobbin−core” is impregnated with polyester varnish.
- Ink jet mark on polyester film at the transformer top.

Electrical Specifications

Table 3. ELECTRIC STRENGTH

50 Hz, 1 minute	Primary	Secondary	Aux	Core
Primary		3000 Vac	1500 Vac	1500 Vac
Secondary	3000 Vac		3000 Vac	1500 Vac
Aux	1500 Vac	3000 Vac		1500 Vac
Core	1500 Vac	1500 Vac	1500 Vac	

Table 4. INDUCTANCES AND RESISTANCES MEASUREMENTS

Description	Measurement Conditions (RLC METER, WK 4230)	Value
INDUCTANCES		
L_{p_open}	Pins 1−6, Sec and Aux open, series measurement, 1 V/10 kHz	604 μH
L_{p_short}	Pins 1−6, Sec and Aux shorted, series measurement, 1 V/50 kHz	4.2 μH
L_{sec_open}	Pins 7,8,9−10,11,12, Prim and Aux open, series measurement, 1 V/10 kHz	38.1 μH
L_{sec_short}	Pins 7,8,9−10,11,12, Prim and Aux shorted, series measurement, 1 V/50 kHz	0.31 μH
RESISTANCES		
R_{prim}	dc resistance, T_a = 25°C	0.222 Ω
R_{sec}	cc resistance, T_a = 25°C	19.3 mΩ
R_{aux}	dc resistance, T_a = 25°C	0.135 Ω

Magnetizing inductance:

$L_m = k \cdot L_{p\_open} = 602\ \mu H$

Leakage inductance:

$$L_{leak} = (1 - k)L_{p\_open} = 2.1\ \mu H \text{ with } k = \sqrt{1 - \frac{L_{p\_short}}{L_{p\_open}}}$$

Typical Signals

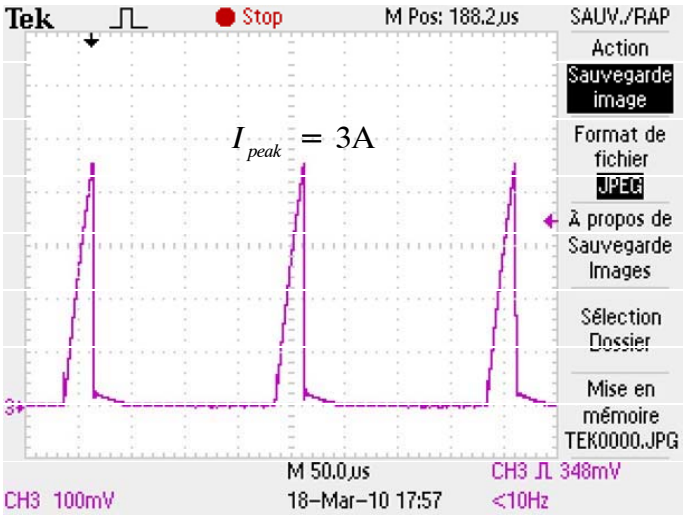


Figure 16. Magnetizing Current
T_{Core} = 70°C

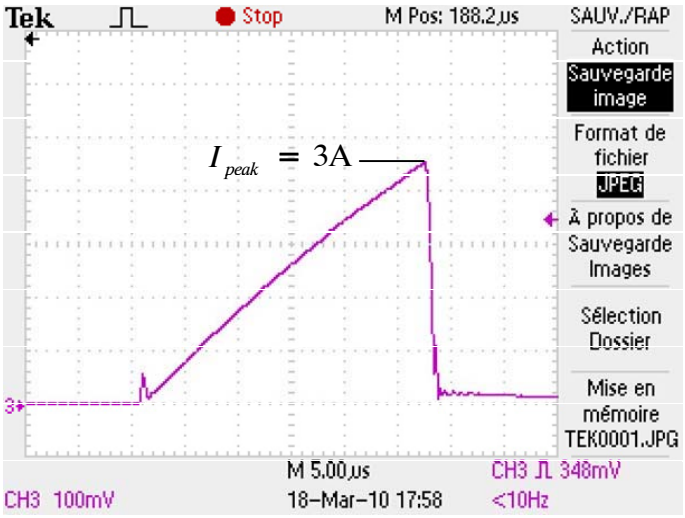


Figure 17. Zoom on the Magnetizing Current
T_{Core} = 70°C

The saturation occurs for a peak current of 3.7 A at a 70°C core temperature. As we have three paralleled 1 Ω resistors (0.33 Ω), the maximum peak current authorized by the controller is 0.8/0.33 = 2.42 A leaving us a good safety margin.

Assembled Transformer

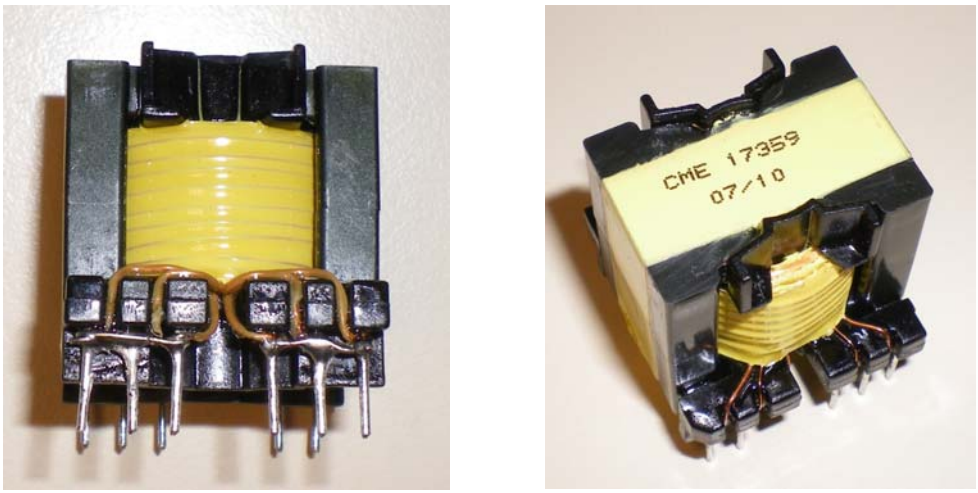


Figure 18. Some Views of the Transformer Once Fully Assembled

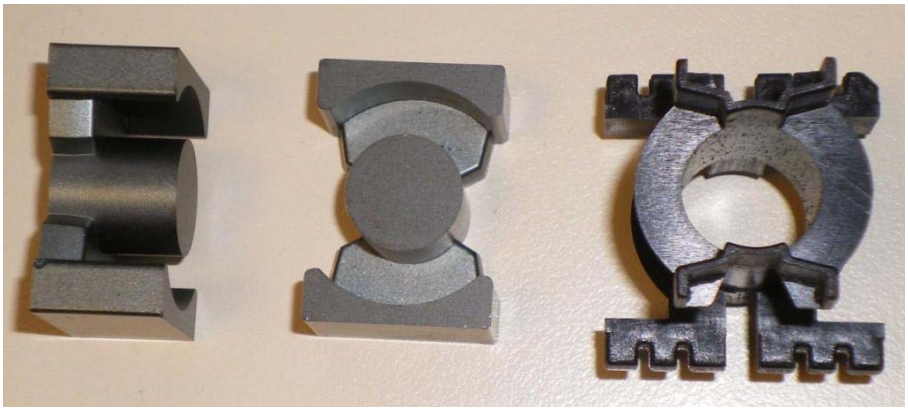


Figure 19. The PQ26/25 Pot Core and the Associated Bobbin

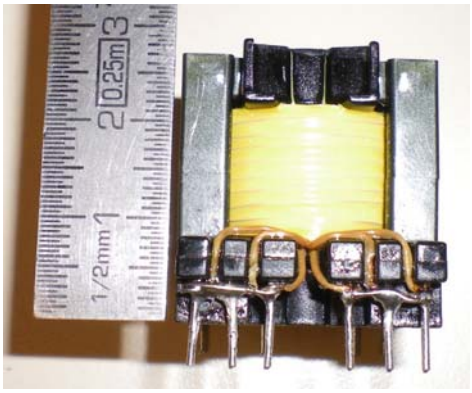


Figure 20. Transformer Height Once Mounted on the PCB

This transformer has been designed and manufactured by the following French company:

CME transformateurs
01160 – St Martin du Mont – France
Tel.: +33 (0)4 74 35 55 11
Fax.: +33 (0)4 74 35 53 97
web: www.cmetransformateur.com
e−mail: contact@cmetransformateur.com

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb–Free	Comments
C1, C10	2	Non existing								
C2	1	high–voltage capacitor	10 nF / 630 Vdc		through–hole	Vishay	MKT1822310635	Yes	Y	
C3	1	electrolytic capacitor	4.7 μF / 35 V		through–hole	Panasonic	ECA1VAD4R7X	Yes	Y	
C4	1	ceramic capacitor	100 pF / 1000 V		through–hole	Panasonic	ECKA3A101KBP	Yes	Y	
C5	1	ceramic capacitor	10 nF		SMD1206	Multicomp	MC1206B103K500CT	Yes	Y	
C5a, C5b	2	electrolytic capacitor	680 μF / 35 V		through–hole	Rubycon	35ZL680M12.5X20	Yes	Y	
C6	1	film capacitor	0.1 μF		through–hole	Multicomp	MCRR50104X7RK0050	Yes	Y	
C7	1	electrolytic capacitor	100 μF / 25 V		through–hole	Rubycon	25ML100M8X9	Yes	Y	
C8	1	ceramic capacitor	1 nF		SMD1206	Multicomp	MC1206B102K500CT	Yes	Y	
C9	1	ceramic capacitor	330 pF		SMD1206	Multicomp	MC1206B331K500CT	Yes	Y	
C11	1	X2 capacitor	470 nF / 275 Vac		through–hole	Evox Rifa	PHE840MY6470MD14R06L2	Yes	Y	
C12	1	high–voltage electrolytic capacitor	100 μF / 400 V		through–hole	Panasonic	ECA2GM101	Yes	Y	
C13	1	EMI Y1 capacitor	2.2 nF / 250 Vac		through–hole	CERAMITE	440LD22	Yes	Y	
C15	1	ceramic capacitor	220 pF		SMD1206	Multicomp	MC1206B221K500CT	Yes	Y	
C17	1	electrolytic capacitor	100 μF / 35 V		through–hole	Panasonic	ECA1VM101	Yes	Y	
D1	1	Zener diode	18 V / 0.5 W		SOT23	ON Semiconductor	BZX84C18LT3G	Yes	Y	
D3, D4, D7	2	fast diode	1N4937		through–hole	ON Semiconductor	1N4937G	Yes	Y	
D5	1	power diode	MBR20200		TO220	ON Semiconductor	MBR20200	No	Y	
D6	1	signal diode	1N4148		through–hole	NXP	1N4148	Yes	Y	
D10	1	signal diode	1N4148		SOD123	ON Semiconductor	MMSD4148T3G	Yes	Y	
HS1, HS2	2	heat sink				SEIFERT	KL195/25.4SW	Yes	Y	
IC2	1	shunt regulator	TL431		TO92	ON Semiconductor	TL431CLOG	Yes	Y	
IC4	1	diode bridge	KBU4K		through–hole	Multicomp	KBU4K	Yes	Y	
J1		jumper	–		through–hole	Multicomp	JR–201S(PCB)	Yes	Y	
J2		jumper			through–hole	WEIDMULLER	PM5.08/2/90	Yes	Y	
L1	1	common mode inductor	2 * 10 mH / 1.2 A		through–hole	Schaffner	RN114–1.2/02	Yes	Y	
L2	1	inductor	2.2 μH / 6 A		through–hole	Wurth Elektronik	744772022	Yes	Y	
M1	1	high–voltage MOSFET	6 A / 600 V		TO220	ON Semiconductor	NDF06N60ZG	No	Y	
Q1	1	PNP transistor	BC857		SOT23	ON Semiconductor	BC857ALT1G	Yes	Y	

Designator	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Pb–Free	Comments
R2	1	mains–connected resistor	220k / 1/4 W		through–hole	Multicomp	MF25220K	Yes	Y	
R3, R7	2	mains–connected resistor	330k / 1/4 W	5%	through–hole	Multicomp	MF25330K	Yes	Y	
R5	1	resistor	1.6k	5%	SMD1206	Vishay	CRCW12061K60FKEA	Yes	Y	
R6a, R6b, R6c	3	power resistor	1/1 W	5%	SMD2512	Vishay	CRCW25121R00FKEA	Yes	Y	
R8, R23	1	resistor	1k / 1/4 W	5%	through–hole	Multicomp	MF251K	Yes	Y	
R9	1	resistor	10k	5%	SMD1206	Vishay	CRCW120610K0FKEA	Yes	Y	
R10	1	resistor	39k	5%	SMD1206	Vishay	CRCW120639K0FKEA	Yes	Y	
R11, R13	2	power resistor	47k / 3 W	5%	through–hole	Vishay	PR03000204702JAC00	Yes	Y	
R12	1	resistor	27k	5%	SMD1206	Vishay	CRCW120627K0FKEA	Yes	Y	
R14	1	NTC thermal sensor	100k @ 25°C		through–hole	Vishay	NTCLE100E3104JB0	No	Y	5.8k @ 100°C
R15, R17, R20	3	mains–connected resistor	680k	5%	SMD1206	Vishay	CRCW1206680K00FKEA	Yes	Y	
R16	1	resistor	22	5%	SMD1206	Vishay	CRCW120622R0FKEA	Yes	Y	
R18	1	resistor	47k	5%	SMD1206	Vishay	CRCW120647K0FKEA	Yes	Y	
R19	1	resistor	1k	5%	SMD1206	Vishay	CRCW12061K00FKEA	Yes	Y	
R21	1	power resistor	22/1 W	5%	through–hole	Vishay	PR01000102209JR500	Yes	Y	
R22	1	resistor	536k	5%	SMD1206	Vishay	CRCW1206536KFKEA	Yes	Y	
R24	1	resistor	220 / 1/4 W	5%	through–hole	Multicomp	MF25220R	Yes	Y	
TP1, TP2, TP3, TP4	4	plastic feet				RICHCO	TCBS–801	Yes	Y	
T1	1	PQ 26/25 flyback transformer			through–hole	CME France	17359–00	No	Y	
U1	1	optocoupler	SFH6156–2			Vishay	SFH6156–2	No	Y	
U3	1	65 kHz controller	NCP1250B		TSOP6	ON Semiconductor	NCP1250B	No	Y	

PUBLICATION ORDERING INFORMATION

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