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# Mains Synchronization for PLC Modems

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APPLICATION NOTE

### Introduction

The sensitivity of a communication receiver strongly depends on a correct and reliable synchronization with the transmitter. In power line communication (PLC), the zero crossing of the mains is commonly used for this synchronization. This application note describes the purpose of synchronization and the effects of mismatch (see Problem section); the synchronization used by ON Semiconductor PLC modems (see Synchronization in ON Semiconductor PLC Modems section). Additionally, five zero crossing detection circuits are described and compared (see Zero Crossing Detections Circuits section).

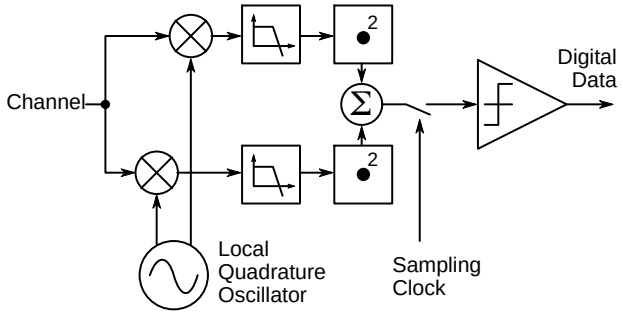


**Figure 1. Simple ASK Demodulator**

### Conclusion

Five zero crossing detector circuits were discussed. The non-isolated detector (see Non−Isolated Circuit section) can be used if no galvanic isolation is required. The conventional topology (see Conventional Detection section) is not suitable to PLC modem applications. The three other circuits (see Low−Voltage Charge Store, Circuit with High−Voltage Charge Storage, and Circuit with Reduced−Length Output Pulse sections) show decreasing power consumption and increasing complexity. Table 2 summarizes measured power consumption at 230 VRMS, component count and a rough cost estimate relative to the conventional solution.

It is critical to compensate the delay introduced by the zero crossing detector which skews the physical bit stream and the bit sampling clock.

In a first step the ZC_ADJUST parameter allows a first adjustment independent of the baud rate in steps of 13 μs.

In a second step the firmware will automatically fine-tune the timing.

### Problem

*Bit Synchronization*

Consider the coherent ASK (amplitude shift keying) demodulator of Figure 1. Although a simplification, it illustrates the importance of correct timing.

In Figure 2, waveforms are shown for this demodulator. The original bit stream and the resulting ASK signal (top signals) are put on the channel by the transmitter. For a noise-free channel, the signal after the filter would also be noise-free. In practice, the noise added by the channel is also present after the filter.

When using an optimally aligned sampling clock, the noise and inter-symbol interference (ISI) is tolerable. However, when the receiver samples too late (bottom traces), the detector often misses. Similarly, an early sampling clock will also cause additional bit errors.

The same problem is found in FSK demodulation. Figure 3 shows the digital part of the receiver of the NCN49597 and NCN49599 modems.

When communicating over the power line, a clock signal cannot be sent along with the data. To synchronize the bit sampling clock, the mains zero crossing is commonly used as an alignment point for the transmission clock, and the baud rate is chosen to be a multiple of the mains frequency.

The communication standard will dictate how the transmission clock is linked to the actual mains zero crossing. The PL110 standard (KNX over power line) requires that bits are aligned to the mains zero crossing (without delay); the ON−PL110 firmware provided by ON Semiconductor is compliant with this requirement[1].

[1]For completeness' sake we add other standards have different requirement. For instance, the IEC 61334 standard requires a delay of 120 ± 20 μs from the mains zero crossing to the start of the first bit of physical frame. Refer to [1] for details. Please note ON Semiconductor does not provide support the IEC 61334 protocol.

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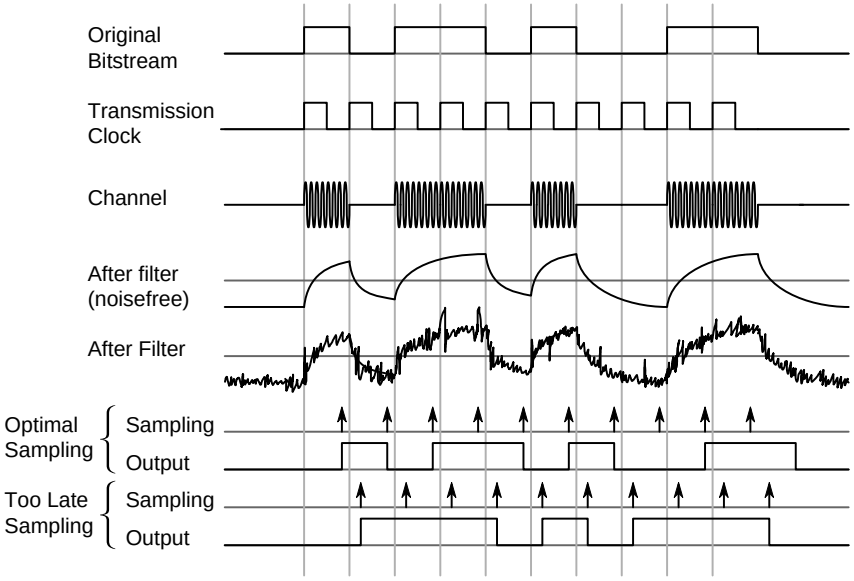


**Figure 2. The Coherent Demodulator of Figure 1: Waveforms and the Resulting Data when Sampling Optimally and too Late**

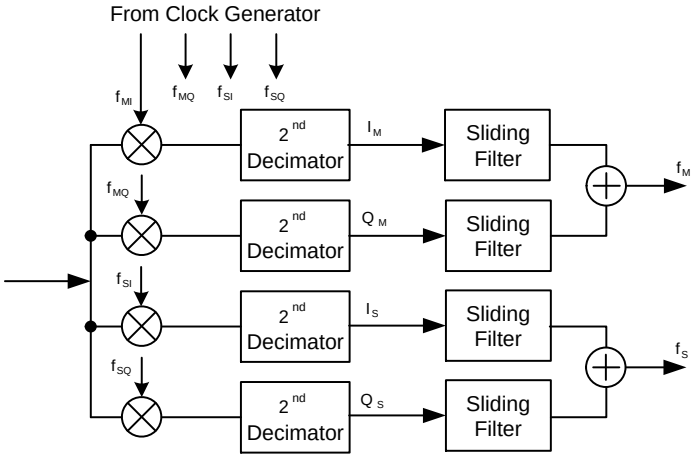


**Figure 3. Digital Part of the Receiver of the NCN49597/9**

*Frame Synchronization*

In addition to bit synchronization the receiver also needs to know the start of the physical frame. Obviously, a frame can only start on a physical bit boundary.

The PL110 protocol is indifferent to frame alignment: a frame can start at the start of any bit slot[2].

**Synchronization in ON Semiconductor PLC Modems**

Figure 4 shows a block diagram of the synchronization flow in the NCN49597 and NCN49599 PLC modems designed by ON Semiconductor. From the mains, an external zero crossing detector derives a synchronous (50 or 60 Hz) low-voltage clock; it is coupled to the modem through the ZC_IN pin. In the modem a digital PLL constructs the *bit clock* as a multiple of the mains frequency. Additionally the *chip clock* is generated at a rate 8 times faster than the bit clock.

Figure 5 shows the same diagram on a signal level.

[2]For completeness' sake, we note the IEC standard also requires that a frame starts on the frame clock, a signal with a period of multiple mains periods. The exact period depends on the baud rate, but a frame clock start is always aligned on a mains zero crossing.

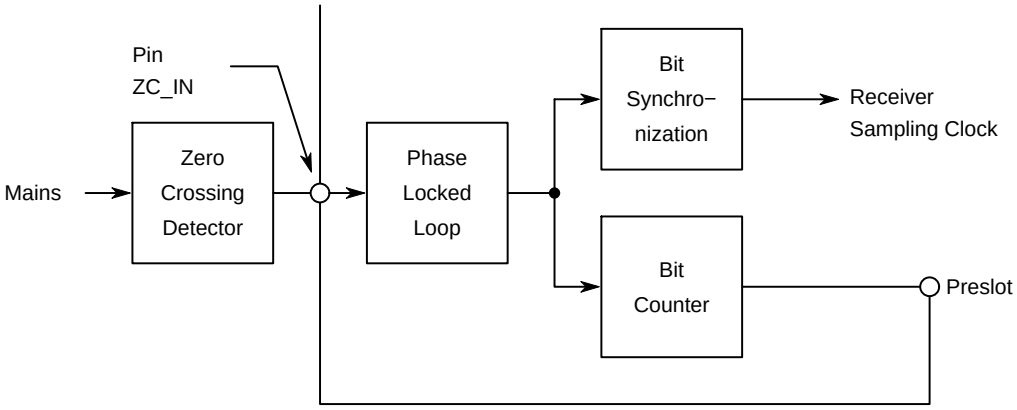


**Figure 4. NCN49597 and NCN49599 Bit and Frame Synchronization**

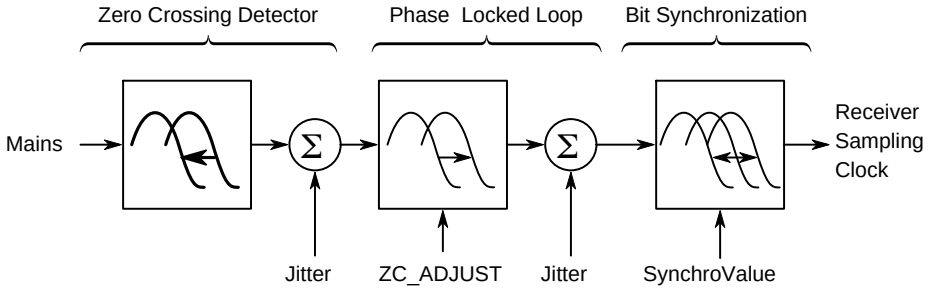


**Figure 5. NCN49597/9 Synchronization Signal Diagram. Note the Direction of Delay Arrows**

Inevitably, the zero crossing detector suffers from a delay (typically 50–500 ms) and from jitter (typically 2–100 ms).

The phase locked loop can shift the zero crossing signal *forward* (i.e., the inverse of a delay). The amount of this shift is controlled through the ZC_ADJUST register and can be varied between 0 and 3.3 ms. The adjustment period or granularity is 13 μs. Additionally, jitter of 25 $\mu s_{pk-pk}$ is added.

A third time shift is controlled by the SynchroValue setting. This adjustment allows shifting the sampling clock from −3 to +4 chip clock period in steps of 1 chip period. The transmitter clock is only dependent on the bit clock; SynchroValue only alters the behavior of the receiver. The optimal synchro bit value is deduced automatically by the firmware; no used interaction is required or possible.

Please note that the ON Semiconductor PL110 software solution can use zero crossing information, but does not require it; the software can automatically synchronize to other nodes. This is especially used for communication over DC lines.

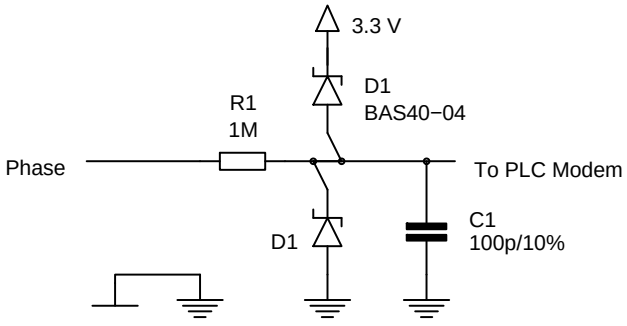


**Figure 6. Non-Isolated Zero Crossing Detector**

*Delay Adjustment*

To obtain the desired delay from the mains zero crossing to the bit clock (120 μs for IDIS, 0 μs for PL110) the ZC_ADJUST register should be used.

As an example, if a zero crossing detector with a characterized total delay of 95 μs is used with the ON−PL110 firmware, the best possible ZC_ADJUST value is 7 ($7 \times 13 = 91$ μs).

### Zero Crossing Detection Circuits

The zero crossing detector generates the mains synchronization signal for the modem. The input is the mains; the output is a 3.3 V TTL signal.

If isolation between modem and mains is not required this circuit can be very simple (see Non−Isolated Circuit section).

Most applications however require galvanic isolation. Optocouplers are an obvious choice, and their conventional application circuit in PLC is described below. However, this circuit has substantial disadvantages (see Conventional Detection section). In Low−Voltage Charge Store, Circuit with High−Voltage Charge Storage, and Circuit with Reduced−Length Output Pulse sections, we present improved circuits.

In the following, we assume a 230 V mains with variations of −30% and +20%. However, bills of materials for 120 V mains circuits appear in Appendix.

*Non-Isolated Circuit*

When no galvanic isolation between the mains and the modem is required, a very simple zero crossing circuit can be used (Figure 6).

To protect the ESD protection cell of the modem pin, Schottky diodes reduce the mains voltage to a 0–3.3 V level. A resistor of 1 MΩ limits the current. It is advisable to add a small capacitor to limit the effects of noise and interference.

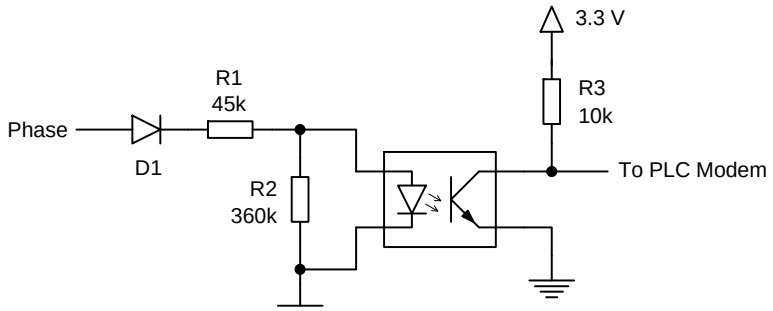


**Figure 7. Conventional Isolated ZC Schematic (Variant 1)**

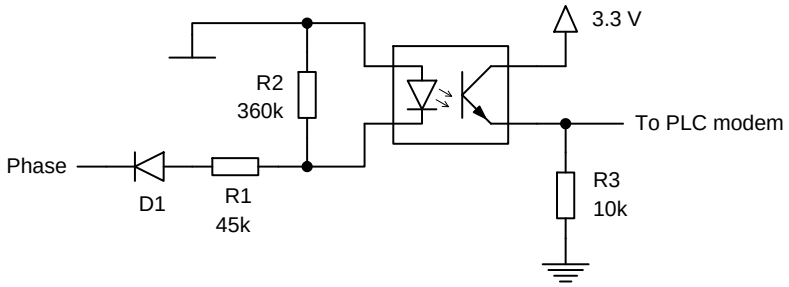


**Figure 8. Conventional Isolated ZC Schematic (Variant 2)**

*Conventional Detection*

Two conventional zero crossing detection circuits are shown in Figures 7 and 8.

Diode D1 protects the LED from reverse voltage and reduces dissipation by half. No current flows through the LED at the zero crossing itself, so the detection is significantly delayed. For example, if the peak amplitude of the LED current is set to 5 mA and if the optocoupler needs 0.5 mA to toggle the shift in time would be in the order of 300 μs. Much bigger currents are drawn after they are no longer needed.

Component Selection

None of the components are critical. It is often convenient to realize the 330 kΩ resistor as a series of smaller resistors. This allows the use of smaller and cheaper packages without exceeding the voltage rating.

The delay introduced by the capacitor can be compensated with the ZC_ADJUST modem setting.

Edge Behavior

The PLL in ON Semiconductor PLC modems synchronizes on the rising edge of the detector output.

The modem can compensate the unavoidable detector delay with an on-chip setting. However, this feature is only effective with constant delay.

Because the rising edge is generated while the LED current is very low the delay is strongly dependent on the current transfer ratio (CTR) of the optocoupler and the *V–I* curve of the LED. These characteristics vary widely from optocoupler type to type and from sample to sample. They also vary with ageing and temperature.

Most optocouplers have no specification for LED currents below 1 mA at all − especially on the turnoff time and it's variation over temperature, device and lifetime. This is especially true for the cheaper optocouplers that would be the first choice for volume production of PLC modems.

The rising edge timing also depends on the actual mains voltage. During measurements, a coefficient of −0.17 μs/V was found (i.e. a higher voltage results in less delay).

It must be noted that the quality and timing of the rising edge is an important difference between the two schematics shown.

In the first variant the rising edge occurs when the optocoupler turns off. Optocoupler turn-off is slower and subjected to larger variations than turn-on. The result is a substantial delay and larger variations of that delay in the field. Additionally, the signal to the PLC modem will occur prior to the actual zero crossing, since the actual transition comes when the half-wave is almost over and drive current for the LED diminishes. Modems made by ON Semiconductor cannot compensate for this.

The second variant is better in this regard. The rising edge is now influenced by the turn-on characteristics of the photo-transistor, and will occur after the actual zero crossing.

In conclusion, the conventional detector suffers from a large and uncontrollable delay. The second variant circuit is only marginally better than the first.

Component Selection

The breakdown voltage of $D_1$ must be sufficient while the leakage current must be small; other parameters are not critical.

The combined value of $R_1$ is calculated for a somewhat arbitrarily chosen peak current under worst case conditions. For a nominal mains voltage of 230 $V_{AC}$ and a desired peak current of 5 mA

$$R_1 = \frac{\sqrt{2} \cdot V_{mains,RMS}(1 - 30\%) - V_{D1} - V_{LED}}{I_{Peak}} \qquad \text{(eq. 1)}$$

$$\approx \frac{228\ V - 0.6\ V - 3\ V}{5\ mA} = 45\ k\Omega$$

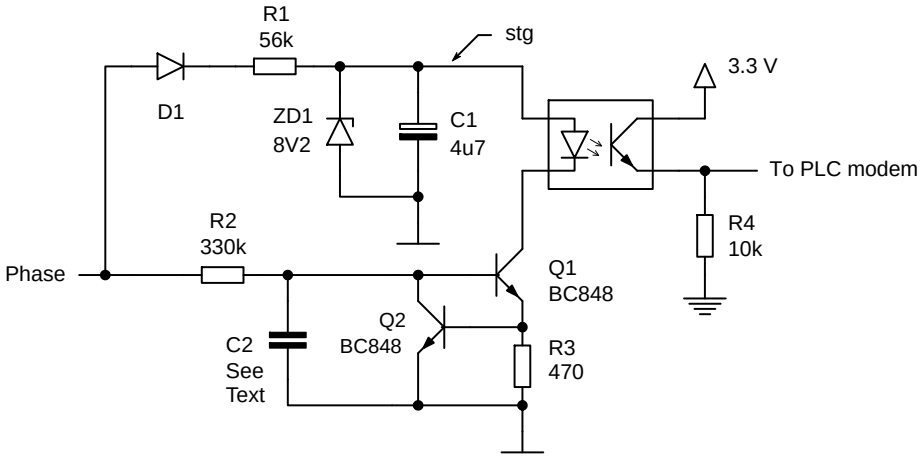


**Figure 9. Improved Isolated ZC Schematic**

The calculation of the power dissipation must take the highest possible mains voltage into account. This results in:

$$P = 50\% \cdot \frac{\frac{(V_{Mains} \cdot 120\%)}{2}}{R_1} = 850\ mW \qquad \text{(eq. 2)}$$

The dissipation rating of $R_1$ and cooling arrangements must ensure reliable operation over the full operating temperature range.

$R_1$ also has to withstand the maximum voltage on the power line; often a series connection of SMD resistors is advantageous to maintain the benefits of surface mounting while meeting the maximum voltage requirements.

$R_2$ is required to avoid breakdown of the optocoupler LED. It is sized to ensure the current through $R_2$ is negligible.

*Low-Voltage Charge Storage*

An improved ZC circuit can be used to ensure more reliable operation without excessive dissipation or high-end optocouplers (Figure 9).

$D_1$, $R_1$, $C_1$ and $ZD_1$ form a simple power supply. The charge on $C_1$ allows current for operating the LED to be drawn at the time of zero crossing, when the conventional solution has negligible current drive capabilities at that time.

Two NPN transistors, $Q_1$ and $Q_1$ form a constant current sink. Local negative feedback yields a constant voltage over $R_3$ (this is the base-emitter voltage of $Q_2$, some 650 mV at the design operating point), and as consequence a constant current through $R_3$.

If the current gain of both transistors is high enough this is about equal to the collector current of $Q_1$ and the LED current.

The power line turns on the CCS during the positive half-wave, when the current through $R_2$ is sufficient to power up the base of $Q_1$. During the negative half wave the $Q_1$ base voltage is forced to about −0.65 V as the base-collector junction of $Q_2$ is forward biased, clamping the mains voltage.

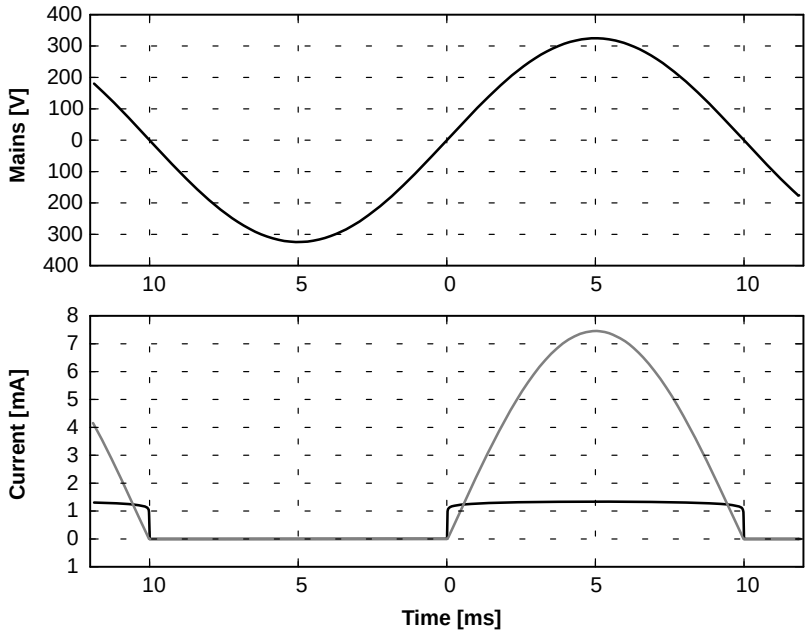


**Figure 10. Current Waveforms through the LED for the Conventional (Grey) and the Improved Detector (Black).**

Figure 10 shows the simulated currents for the conventional (grey trace) and the improved (black) ZC circuits. The LED drive current for the improved circuit is much close to an ideal square wave, which significantly narrows the uncertainty window in which the zero crossing will be detected.

In the conventional circuit the current is much smaller close to the real zero crossing − 160 μA at 300 μs after the actual zero crossing. With the improved ZC circuit 1 mA is reached in 40 μs, and this delay can be further shortened with some reduction of $R_2$.

The measured delay between the actual power line zero crossing and the isolated side of 6 HCPL−817 optocouplers, in both the conventional and the improved circuits, is represented in Table 1.

The total device-to-device variation is reduced from 93 μs to 24 μs. An even bigger effect is expected with optocouplers with worse CTR at low LED currents.

Additionally, measurements on TCET−1109, SFH615A−3 and NEC 2501 optocouplers show a type-to-type variation of only 10 μs.

It is important to note that these measurements are done at room temperature and without any ageing. Drive techniques used in the improved ZC circuit will also reduce further variations in the field.

**Table 1. MEASURED DELAY OF THE CONVENTIONAL AND THE IMPROVED ZERO CROSSING DETECTOR**
(6 HCPL−817 Optocoupler Samples)

| Sample | Conventional Circuit | Improved Circuit |
|---|---|---|
| 1 | 374 μs | 70 μs |
| 2 | 281 μs | 52 μs |
| 3 | 298 μs | 46 μs |
| 4 | 298 μs | 61 μs |
| 5 | 298 μs | 62 μs |
| 6 | 290 μs | 55 μs |

Component Selection

The reverse polarity protection diode $D_1$ must withstand the peak reverse voltage expected on the mains. Besides from leakage (which should be below 100 μA in the full operating temperature range) there are no special requirements for this diode.

The LED drive current in the suggested schematics is around 1.3 mA, and is defined by the 650 mV voltage drop over the 470 Ω value of $R_3$. Increasing this current is certainly possible, but will also require proportional change in other components since all the currents will proportionally scale.

The value of the reservoir capacitor $C_1$ suggested in Figure 2 (4.7 μF) is a good compromise between voltage ripple and start-up time. The available charge current is limited by the power dissipation in $R_1$ and the need to keep the efficiency high. Values shown in Figure 2 give a start-up time of 50 ms for proper zero cross detection and 250 ms until $C_1$ is fully charged.

The voltage ripple is below 500 mV, which is no problem for the CCS performance. The current ripple through $C_1$ is small (below 1 mA) so part selection is straightforward. The rated voltage must exceed the 8.2 V zener voltage.

The choice of $R_1$ is directed by the average current balance. If $R_1$ is too low excess power is dissipated in the zener diode. If $R_1$ is too high, LED current will be limited by $R_1$ and not by the current source; the circuit will behave identical to the conventional solution.

The current drawn over the positive half-wave dominates. Over this period a constant current of 1.3 mA is drawn by the LED. To ensure the voltage is well stabilized by the zener diode about as much current must flow through the zener. Over the same period the average current through $R_1$ can be approximated as the RMS voltage of the mains divided by $R_1$.

It follows the latter current must be sufficiently higher than the load currents under worst case conditions, which comprises:

- Lowest mains voltage anticipated; in our case 230 $V_{RMS}$ · 30%
- Highest LED current:
  - The 650 mV *VBE* typical for room temperature would grow to 800 mV at −55°C
  - The lowest $R_3$ value foreseen: as an example, 5% resistance tolerance

Together this would result in 1.8 mA (a 30% increase).

For this design example this would result in 63 kΩ. We select an E12 value of 56 kΩ. Once the value has been chosen the worst-case power dissipation can be calculated. Again, we approximate the current through $R_1$ as the RMS mains voltage (now the highest possible) divided by the worst-case $R_1$ during half of the time. This results in (230 $V_{RMS}$ + 20%) 2 / (56 kΩ · 5% tolerance) / 2 = 715 mW.

Again, depending on cost considerations $R_1$ may be split in series-connected lower value resistors.

$R_2$ can be reduced 2 to 3 times if further improvement of the delay is desired at the expense of additional power dissipation. However, a constant delay is more important than a small delay.

$Q_1$ and $Q_2$ operate at $V_{CE}$ < 10 V and $I_C$ ≈ 1 mA. High current gain is desired. The BC848 shown in Figure 9 is a reasonable choice; a large number of alternatives is available.

The value of $R_4$ is a compromise. Low values result in lower delay times while higher values ensure less circuit sensitivity to the CTR of the optocoupler. 10 kΩ will be reasonable in most designs. It is always a good idea, though, to check a couple of values (e.g. 3.3 kΩ and 33 kΩ) prior to volume production start. A full voltage swing at the ZC pin is advisable for reliable operation. If the voltage swing is below 3.3 V the designer must verify that the CTR of the selected optocoupler is sufficient at the designed current.

For the design example discussed above a CTR of 100% would give 1.3 mA in the photo-transistor, which should be more than sufficient to get the full voltage swing on the ZC pin.

In case optocouplers with significantly different CTR (Current Transfer Ratio) for low LED forward currents have to be used the values of $R_1$, $R_2$ and $R_3$ may have to be scaled (down) accordingly. For example, if a drive current of 2.5 mA is found to be sufficient with another series of optocouplers their values would need to be decreased two times. This would inevitably increase power drained from the mains and higher component cost and is most likely never desired, which limits the choice of optocouplers.

However, the demands towards optocouplers are even higher in the conventional schematic; therefore the improved ZC schematic is advantageous also when cost reduction is targeted with lower grade optocouplers.

The optocoupler remains the key in isolated ZC designs. However, finding low-cost devices with even not low but at all specified turn-on times at 1 mA drive currents over temperature and lifetime is often a problem. As a general rule devices specified with highest CTR at lowest LED forward current would be significantly better. The improved design relaxes the optocoupler requirements since the trigger point is made less sensitive to characteristics variations.

Compared to the design example above for the conventional detector, the dissipation is not much lower, but the timing is now reliable. The component cost has only increased marginally.

*Circuit with High-Voltage Charge Storage*

If a further reduction of power consumption is required the circuit depicted in Figure 11 can be employed. The basic operating principle remains the same; however, the regulated voltage is now derived directly from the mains and is thus much higher (about 300 $V_{DC}$ instead of 8.2 $V_{DC}$).

Additionally, the base resistor $R_2$ of Figure 9 has been replaced by a diode-resistor combination, halving the power dissipated in $R_2$. To ensure the base voltage of $Q_1$ is

well-controlled during the negative half-cycle, $R_3$ has been added.

The power consumption is now halved compared to the circuit of Figure 9 at somewhat higher cost. For a full comparison refer to the Appendix.

Measured waveforms are shown in Figure 12 (solid black). The upper pane shows the mains input and the top plate voltage of $C_1$; below the output signal is shown. The third pane shows the currents[3] through the optocoupler diode (rectangular wave current) and the total current flowing into the circuit.

Three simulated waveforms are also shown (dashed grey lines): the $C_1$ top plate voltage and both currents.

The difference between the simulated and measured LED current is small, but this leads to a more pronounced difference in the most critical parameter: the lowest voltage on $C_1$. This once again underlines the importance of carefully verifying circuit behavior.

[3]After capture, both signals were low-pass filtered with a bandwidth of 30 kHz to reduce displayed noise. It was verified this filtering does not hide significant signal features.

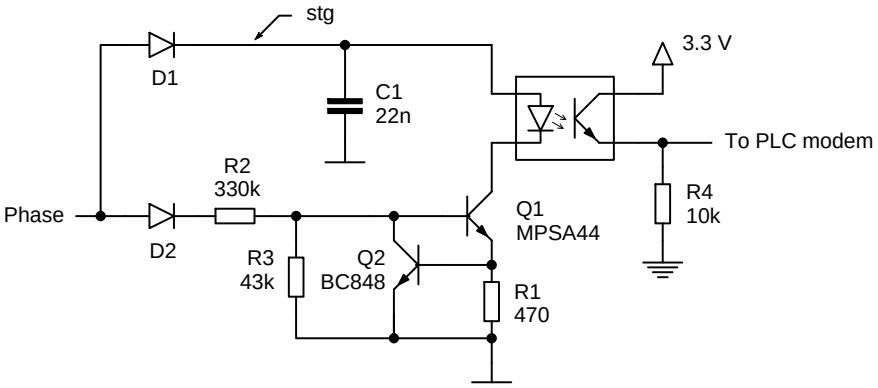


**Figure 11. Schematic of the Detector with High-Voltage Charge Storage**

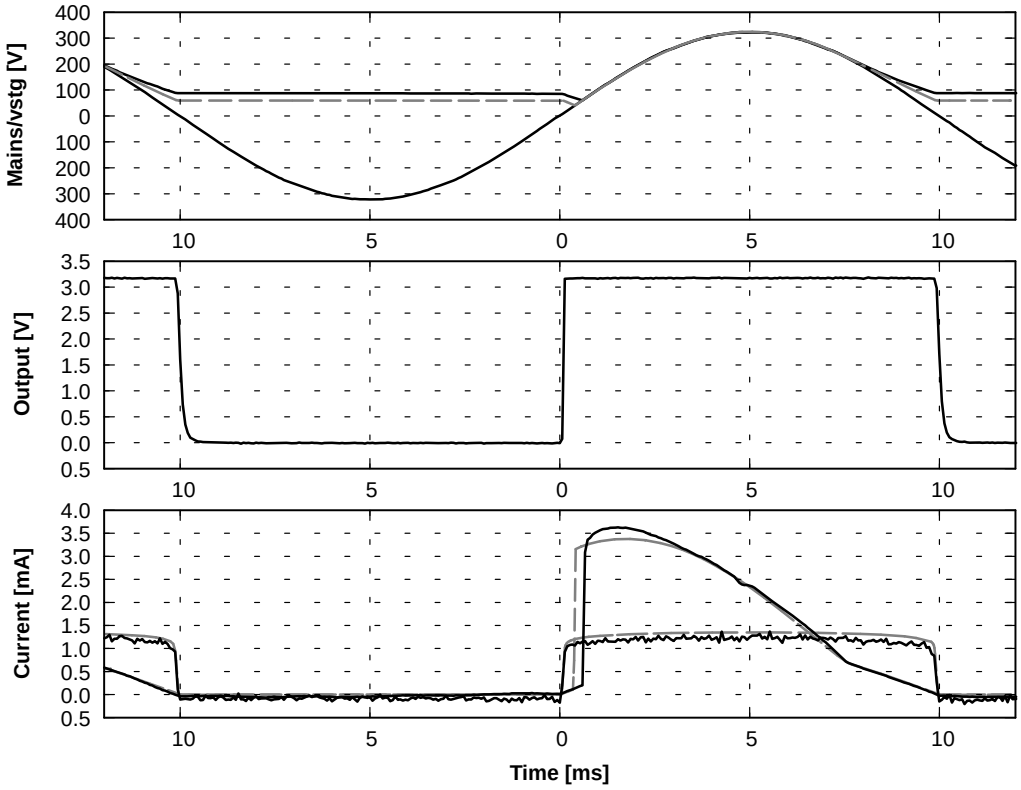


**Figure 12. Measured (Solid Black) and Simulated Signals for the High-Voltage Charge Storage Pulse Detector**
(Refer to the text for details)

Component Selection

First chose the minimal allowable voltage on $C_1$, $VC_{1,min}$. The current source requires some voltage drop to function properly. The drop across the LED must be added to this. $VC_{1,min}$ = 10 V is a safe starting point; a lower value does not result in a substantial cost gain.

$C_1$ is recharged during the rising half of the positive mains period. The charge on $C_1$ is used from $t = t_{start}$, when

$$\frac{d}{dt} V_{Mains}(t) \Big|_{t = t_{Start}} = \frac{I_{LED}}{C_1} \quad \text{(eq. 3)}$$

which leads immediately to

$$\sqrt{2} \cdot V_{Mains} \cdot 2\pi \cdot f_{Mains} \cdot \cos\left(2\pi \cdot f_{Mains} \cdot t_{Start}\right) = \frac{I_{LED}}{C_1} \quad \text{(eq. 4)}$$

At the falling zero crossing, the current source switches off. The charge is again used from the rising zero crossing until the mains voltage rises to $V_{C1}(t) + V_D$. By design requirement, at this point $V_{C1}(t = t_{min}) = V_{C1,min}$. It may be seen that

$$t_{min} = \frac{1}{2\pi \cdot f_{Mains}} \arcsin \frac{V_{C1,min}}{\sqrt{2} \cdot V_{Mains,RMS}} \quad \text{(eq. 5)}$$

The worst-case condition is a low mains voltage. As an example, if a 30% drop below nominal is foreseen,

$$C_1 > I_{LED} \cdot \frac{\frac{1}{2} \cdot t_{Mains} - t_{Start} + t_{min}}{\sqrt{2}\min V_{Mains,RMS} - V_{Q1,min}} = \frac{V_T}{R_1} \cdot \frac{\frac{1}{2} \cdot t_{Mains} - t_{Start} + t_{min}}{\text{nom } V_{Mains,RMS}(1 - 30\%) - V_{Q1,min}} \quad \text{(eq. 6)}$$

As the right hand side of Equation 6 depends on $C_1$, an analytical expression for $C_1$ is not readily deduced, but a numerical value of 18 nF can be calculated for the conditions given. Simulation confirms this.

The only requirements for the diodes are sufficient breakdown voltage and low leakage current. The peak voltage rating of $D_2$ should allow for the highest mains peak voltage expected. The peak voltage rating of $D_1$ should exceed *twice* the mains peak voltage; the voltage over $C_1$ doubles the voltage over $D_1$ during the negative mains alternation.

$C_1$ and $Q_1$ must be high-voltage types. An MPSA44 transistor (suggested for $Q_1$) has a collector-emitter breakdown voltage of 400-V. $Q_2$ can be a low-voltage transistor; BC848 is suggested. $R_1$ can be designed as before, keeping in mind that $C_1$ must scale with the desired LED current (Equations 4 and 6).

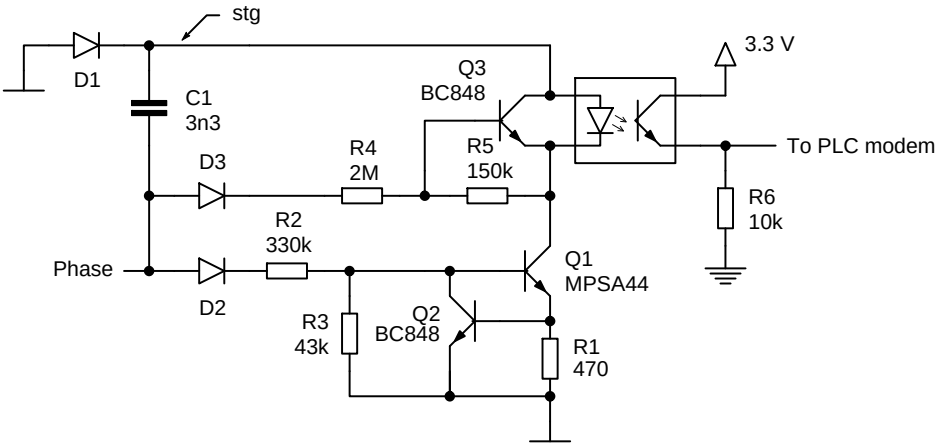


**Figure 13. Schematic of the Detector with Reduced Output Pulse Length**

*Circuit with Reduced-Length Output Pulse*

Even lower power consumption can be obtained at the cost of a more complex circuit (Figure 11).

During the first half of the negative half-cycle, $C_1$ is charged through $D_1$. During the second half, $D_1$ no longer conducts and the voltage on the top plate of $C_1$ (the net denoted 'stg' in Figure 13) rises together with the mains voltage.

Slightly after the zero crossing, the current source ($Q_1$, $Q_2$, &c.) switches on and the charge on $C_1$ is consumed. Therefore, the LED will not conduct during the full positive half-cycle. The exact conduction time will depend on the charge on $C_1$. Thus, the average LED current consumption can be reduced to a very low value.

In contrast to the circuits discussed before the output pulse duty cycle is now substantially less than 50%. However, as all ON Semiconductor modems synchronize on the rising edge of the zero crossing detector output, correct alignment is maintained.

While the rising edge is well defined by the turn-on of the current source, the falling edge is significantly less controlled if the output duty cycle is less than 25%. In this operating mode, the mains voltage continues to rise even after the charge on $C_1$ has been depleted. This results in an low but ill-defined current through the optocoupler LED; in turn, this results in an ill-defined falling edge.

Although correct operation can be maintained by buffering the output with a logic gate, the solution depicted

in Figure 13 is more robust. After the voltage on *stg* falls below the mains voltage, $Q_3$ bypasses the optocoupler LED entirely, resulting in a clean falling edge.

Some measured waveforms are shown in Figure 14 and the top place voltage of $C_1$; below the output signal is shown. The third pane shows the currents[4] through the optocoupler diode (rectangular wave current) and the total current consumption of the circuit. Three simulated waveforms are also shown (dashed grey lines): the $C_1$ top plate voltage and both currents.

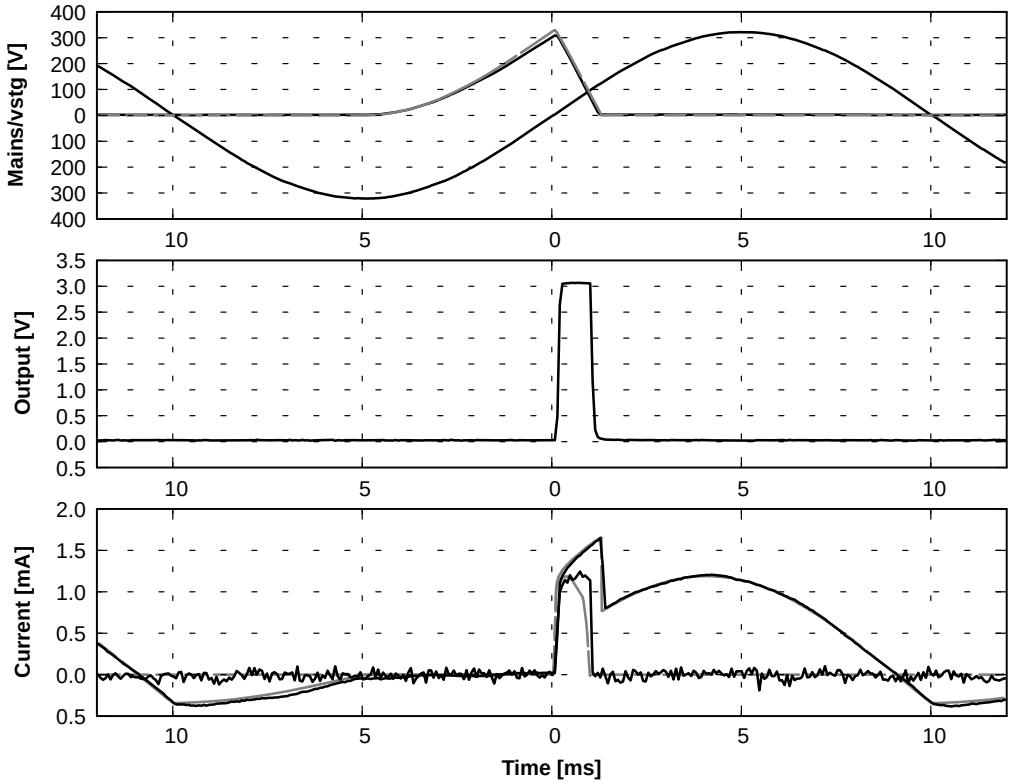


**Figure 14. Measured (Solid Black) and Simulated Signals for the Reduced-Length Output Pulse Detector**
(Refer to the text for details)

Compared to the circuit of Figure 11, the power consumption is halved again, with the component cost somewhat higher. For a full comparison refer to the conclusion (see Appendix).

The value can be easily calculated if the pulse time is short. Under this condition, a first-order approximation of the mains voltage around the zero-crossing can be employed. The voltage $V_C$ over the capacitor diminishes as current is drawn. The voltage on the net *stg* is then given by (with $t = 0$ at the positive zero crossing)

$$V_{stg}(t) = V_{Mains}(t) + V_C(t) \qquad \text{(eq. 7)}$$

$$\approx t \left.\frac{dV_{Mains}(t)}{dt}\right|_{t=0} + \left(V_C(t=0) - \frac{t \cdot I_{LED}}{C_1}\right)$$

When the capacitor charge has been exhausted $V_{stg}(t) \approx 0$; by solving for $t$ one can determine the value of $C_1$ for a given LED current, mains voltage and pulse time $t$. The actual pulse will be somewhat shorter due to $Q_3$. The 3.3 nF value given maintains an 800 ms pulse even if the mains voltage is 30% below nominal.

The diodes $C_1$ and $Q_1$ must be high-voltage types. Both $Q_2$ and $Q_3$ can be low-voltage transistors. $R_1$ can be changed as before, keeping in mind that $C_1$ must scale with the desired LED current.

The power dissipation of the components should not be problematic, but the voltage rating of $R_2$ and $R_4$ must be sufficient to withstand the mains voltage.

Component Selection

Again, the value of $C_1$ must allow for reliable operation under worst-case conditions; that is, under low mains voltage.

All diodes should have a peak voltage rating exceeding the highest expected mains peak voltage.

*Safety*

Safety must be considered carefully for measurements. A current as low as 30 mA through the heart can be lethal. Recommendations for safer measurements on circuit with deadly voltages such as zero crossing detectors are beyond the scope of this document; they can be found in [2] and [3, section Safety].

[4]As in Figure 12, the currents are band-limited to 30 kHz.

**Table 2. ZERO CROSSING CIRCUITS COMPARED**
(Measurement power consumption, component count and cost relative to the conventional solution.)

| Circuit | Components | 230 $V_{AC}$ Variant | | 120 $V_{AC}$ Variant | Figure |
|---|---|---|---|---|---|
| | | Cost | Dissipation | Dissipation | |
| Non-Isolated | 3 | 0.2 | 50 mW | 30 mW | 6 |
| Conventional | 5 | 1.0 | 590 mW | 290 mW | 7 |
| Low-Voltage Charge Storage | 10 | 1.5 | 610 mW | 400 mW | 9 |
| High-Voltage Charge Storage | 10 | 1.9 | 230 mW | 120 mW | 11 |
| Reduced-Length Output Pulse | 15 | 2.3 | 110 mW | 50 mW | 13 |

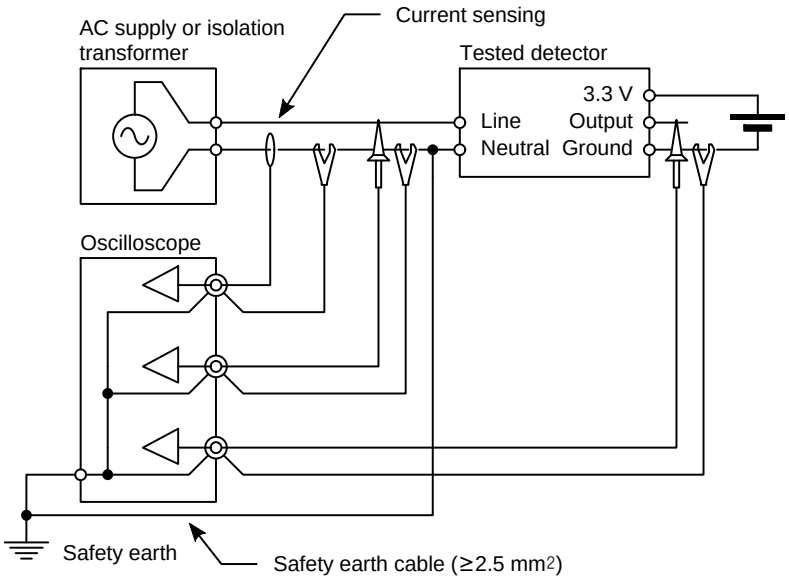


**Figure 15. Measuring the Power Consumption, Delay and Jitter of a Zero Crossing Detector**

*Evaluating Circuits*

Already noted several times in the preceding sections, it can not be stressed enough the designed circuit must be tested thoroughly. The substantial variation in available optocoupler types will require a complete evaluation over temperature and mains voltage. Part-to-part variations must also be considered carefully.

Fortunately, testing a zero crossing detector is fairly simple. An adjustable AC source (either an AC laboratory supply or an autotransformer) must be available to verify correct operating within the design voltage range.

To measure the current, a current probe may also be used provided it is sufficiently sensitive.

Alternatively, use a small series resistor (about 100 Ω) in the neutral line and acquire the signal across it with an oscilloscope. A high-voltage differential probe is the safest measurement method (Figure 16, right) but a generic probe can be used if care is taken to ensure safety (Figure 16, left).

Noise can be especially problematic with switch-mode AC sources. The current, and therefore the voltage across the resistor, is small. If noise and tones interfere with the measurement, a filter may be used. The filters shown in Figure 16 have a 3 dB bandwidth exceeding 10 kHz.

The consumed power is derived from the current waveform by integrating with the measured mains voltage waveform[5]. Low-pass filtering the acquired oscilloscope data can improve the accuracy of the measured power consumption value. Software such as Numerical Python, Matlab or Octave are useful for this.

Jitter may be estimated by triggering the oscilloscope on the true mains zero crossing and configuring the display to show persistent traces[6]. As an example, the screen image of Figure 17 shows the mains (left trace) and the detector output. A jitter of approximately 6.8 μs is found with the oscilloscope cursors. The average delay is about 93 μs.

Alternatively, a script can repeatedly measure the delay. This approach has the advantage that statistical data becomes available.

[5]Multiplying the current with the RMS voltage of course overestimates the dissipation as it includes reactive power. This power is especially significant for the reduced-length output pulse circuit.
Care must be taken to deskew the current and voltage measurements. Skew between both is especially significant when using a split-core current probe.

[6]Tektronix, who introduced this feature, calls this “digital phosphor”.

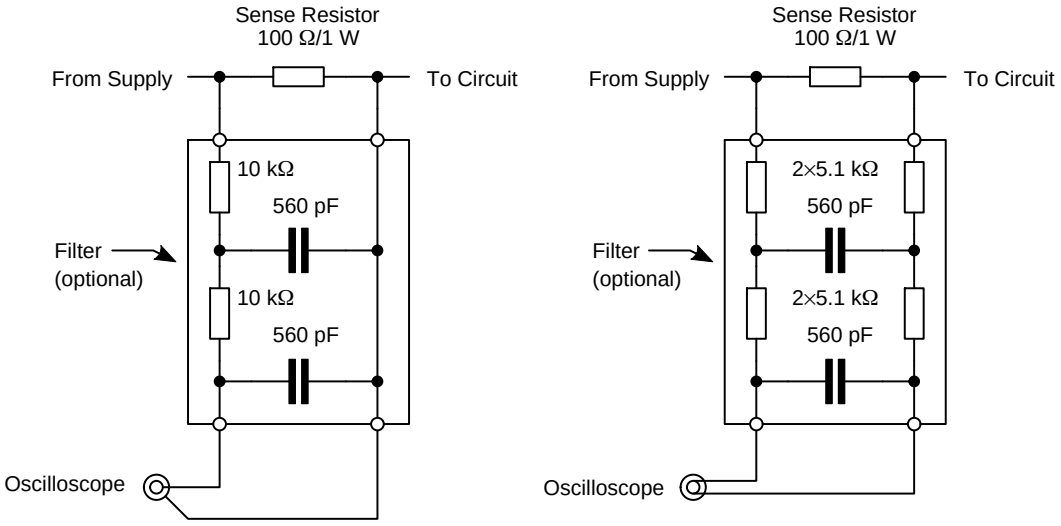


**Figure 16. Measuring the Current with a Single-Ended (Left) or Differential Oscilloscope Probe (Detail of Figure 15)**

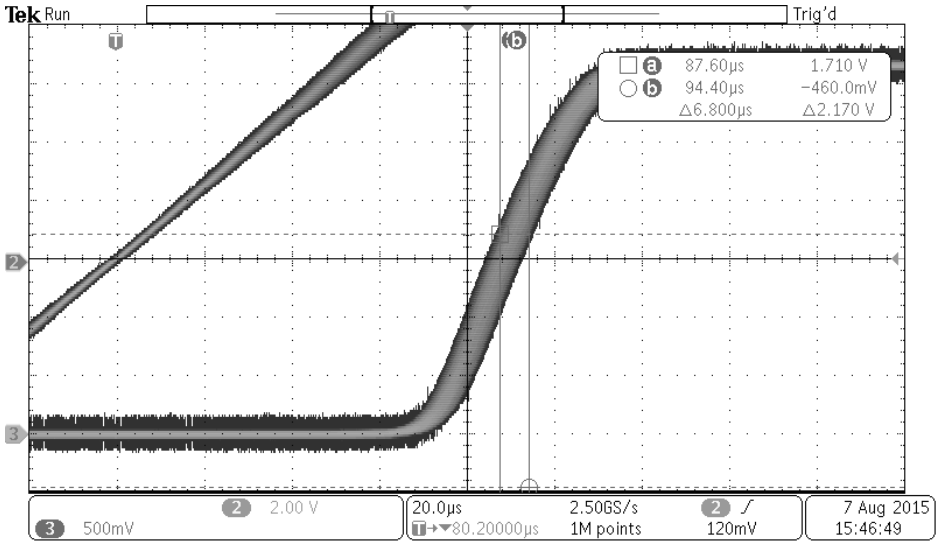


**Figure 17. Measuring the Output Jitter Current with an Oscilloscope Configured to Show Persistent Traces. Mains (Left) and Detector Output are Shown**

Volume Production

Optocoupler characteristics can vary from batch to batch, especially at low drive currents.

Therefore, we recommend to measure the delay as part of outgoing testing in volume production.

*Summary*

Table 2 compares the power dissipation of the zero crossing detector circuits discussed above. For the 230 $V_{AC}$ variant, a cost estimate relative to the conventional solution is also given.

## APPENDIX

### Component Lists

The following bills of materials are given as an example only. In practice, the choice of optocoupler will drive the design.

The optocoupler and its pull-up resistor are not included.

*Non-Isolated Detection*

**Table 3. NON-ISOLATED DETECTION**

| Component | 230 $V_{AC}$ Variant | 120 $V_{AC}$ Variant |
|---|---|---|
| C1 | 100 pF | 150 pF |
| D1 | BAS40−04 | BAS40−04 |
| R1 | 1 MΩ | 510 kΩ |

*Conventional Detection*

Values are given for a 5 mA peak current; this choice must be verified for the selected optocoupler.

**Table 4. CONVENTIONAL DETECTION**

| Component | 230 $V_{AC}$ Variant | 120 $V_{AC}$ Variant |
|---|---|---|
| D1 | S1FLJ | BAS21LT1G |
| R1 | 43 kΩ | 24 kΩ |
| R2 | 300 kΩ | 300 kΩ |
| R3 | 10 kΩ | 10 kΩ |

*Low-Voltage Charge Storage*

Values are given for a 1.3 mA peak current; this choice must be verified for the selected optocoupler. It might be convenient to replace the BC848 transistors by a dual transistor such as the NTJD4401NT2G.

**Table 5. LOW-VOLTAGE CHARGE STORAGE**

| Component | 230 $V_{AC}$ Variant | 120 $V_{AC}$ Variant |
|---|---|---|
| C1 | 4.7 μF/16 V | 4.7 μF/16 V |
| C2 | See Text | See Text |
| D1 | S1FLJ | BAS21LT1G |
| Q1, Q2 | BC848BWT1G | BC848BWT1G |
| R1 | 56 kΩ | 22 kΩ |
| R2 | 330 kΩ | 160 kΩ |
| R3 | 470 Ω | 470 Ω |
| R4 | 10 kΩ | 10 kΩ |
| ZD1 | MM3Z8V2ST1G | MM3Z8V2ST1G |

*High-Voltage Charge Storage*

**Table 6. HIGH-VOLTAGE CHARGE STORAGE**

| Component | 230 $V_{AC}$ Variant | 120 $V_{AC}$ Variant |
|---|---|---|
| C1 | 22 nF/450 V | 33 nF/450 V |
| D1 | S1FLK | S1FLJ |
| D2 | S1FLJ | BAS21LT1G |
| Q1 | MPSA44 | MMBTA42LT1G |
| Q2 | BC848BWT1G | BC848BWT1G |
| R1 | 470 Ω | 470 Ω |
| R2 | 330 kΩ | 160 kΩ |
| R3 | 43 kΩ | 43 kΩ |
| R4 | 10 kΩ | 10 kΩ |

*Reduced-Length Output Pulse*

**Table 7. REDUCED-LENGTH OUTPUT PULSE**

| Component | 230 $V_{AC}$ Variant | 120 $V_{AC}$ Variant |
|---|---|---|
| C1 | 3.3 nF/450 V | 6.8 nF/250 V |
| D1, D2, D3 | S1FLK | BAS21LT1G |
| Q1 | MPSA44 | MMBTA42LT1G |
| Q2, Q3 | BC848BWT1G | BC848BWT1G |
| R1 | 470 Ω | 470 Ω |
| R2 | 330 kΩ | 160 kΩ |
| R3 | 43 kΩ | 43 kΩ |
| R4 | 2 MΩ | 2 MΩ |
| R5 | 150 kΩ | 150 kΩ |
| R6 | 10 kΩ | 10 kΩ |

## REFERENCES

[1] IEC. Automatisation de la distribution àpar l'aide de systèmes de communication à courants porteurs − partie 4: Protocoles de communication de données − Section 32: Couche liaison de données − Contrôle de liaison logique (LLC), September 1996.
[2] Tektronix. Fundamentals of floating measurements and isolated input oscilloscopes, February 2005. Application note, online at http://info.tek.com/www−fundamentalsof−floating−measurements−andisolated−input−oscilliscopes.html
[3] Pierre Woestyn, Peter Cox, et al. *Evaluation kit for power-line communication user manual*. ON Semiconductor, July 2015.

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