ESD Protection Diode

Micro−Packaged Diodes for ESD Protection

ESD7421, SZESD7421

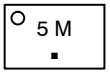
The ESD7421 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, automotive sensors, infotainment, MP3 players, digital cameras and many other applications where board space comes at a premium.

Specification Features

- Low Capacitance 0.3 pF
- Low Clamping Voltage
- Low Leakage 100 nA
- Response Time is < 1 ns
- IEC61000−4−2 Level 4 ESD Protection
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

XDFN2
(SOD−882)
CASE 711AM

MARKING DIAGRAM



5 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
ESD7421N2T5G	XDFN2 (Pb−Free)	8000 / Tape & Reel
SZESD7421N2T5G	XDFN2 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		±12 ±15	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	300	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

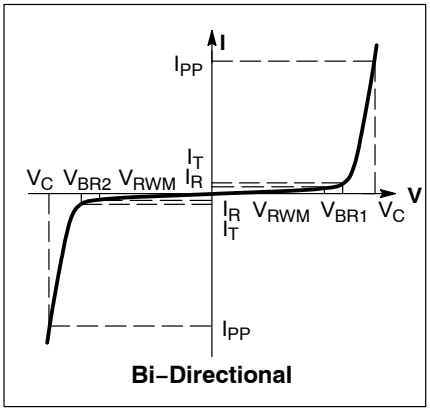
See Application Note AND8308/D for further description of survivability specs.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR1}	Breakdown Voltage @ I_T
V_{BR2}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Pin 1 to GND Pin 2 to GND		5 5	16 10	V
Breakdown Voltage	V_{BR1}	I_T = 1 mA, Pin 1 to GND	16.5			V
Breakdown Voltage	V_{BR2}	I_T = 1 mA, Pin 2 to GND	10.5		14	V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND V_{RWM} = 16 V, Pin 1 to GND		100	500 1.0	nA μA
Clamping Voltage (Note 2)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 2 and 3			
Clamping Voltage TLP (Note 3)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		35 38.1 −21 −29.5		V
Junction Capacitance	C_J	VR = 0 V, f = 1 MHz between I/O Pins and GND		0.3	0.6	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For test procedure see Figure 5 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

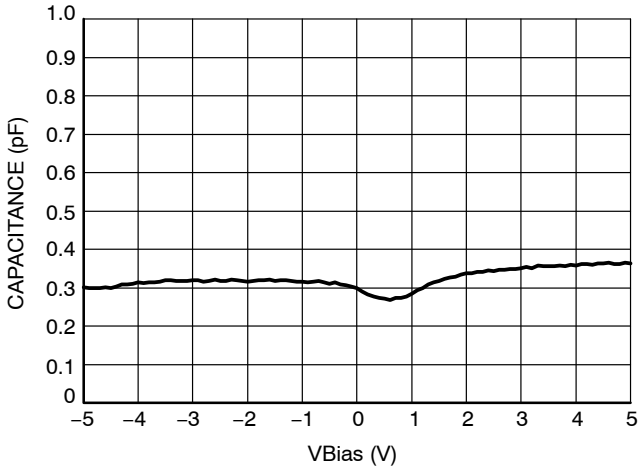


Figure 1. Typical CV Characteristic Curve
Pin1 to GND (GND connected to Pin2)

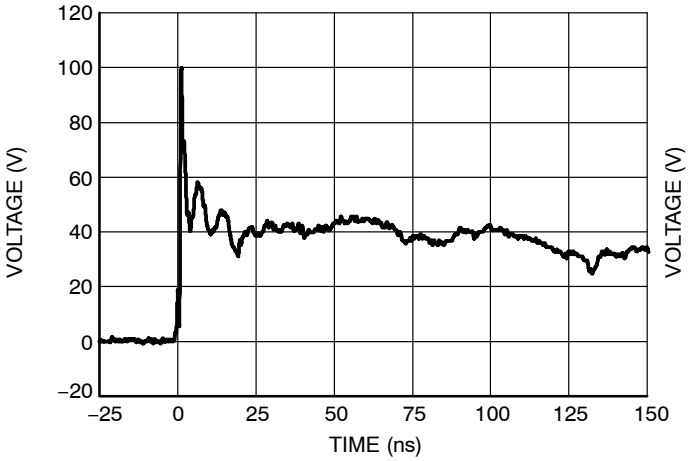


Figure 2. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage
Pin1 to GND (GND connected to Pin2)

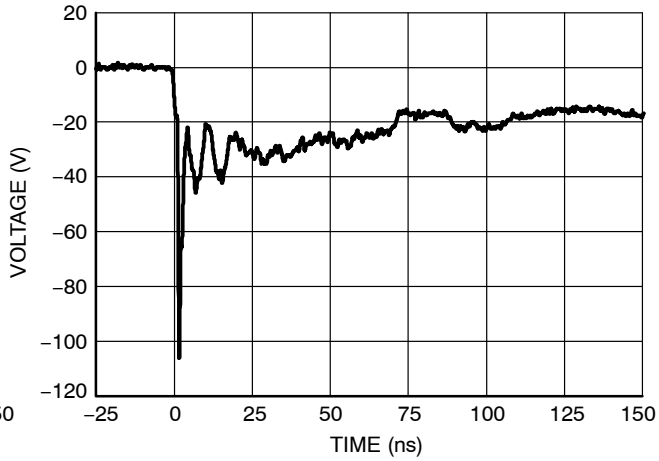


Figure 3. IEC61000−4−2 −8 kV Contact ESD Clamping Voltage
Pin1 to GND (GND connected to Pin2)

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

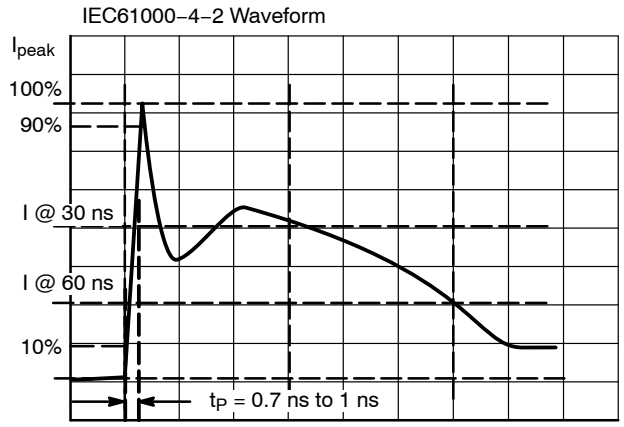


Figure 4. IEC61000−4−2 Spec

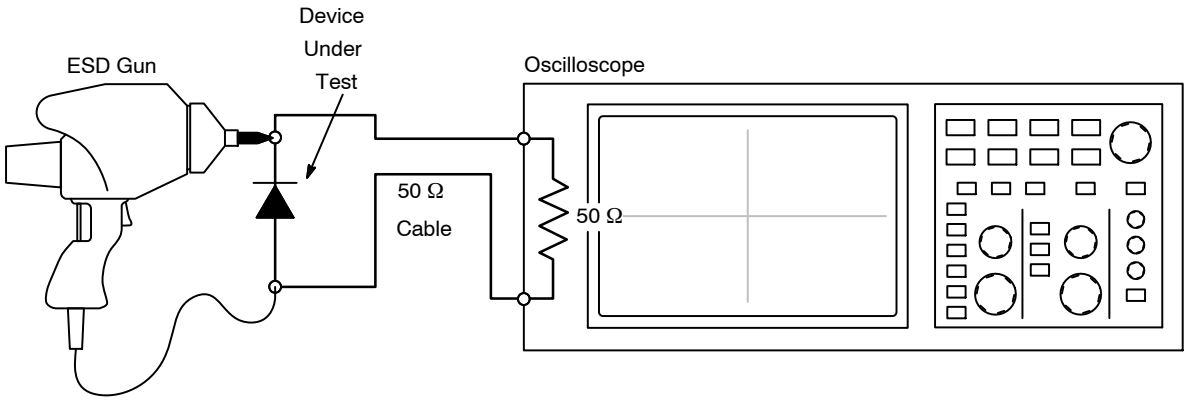


Figure 5. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

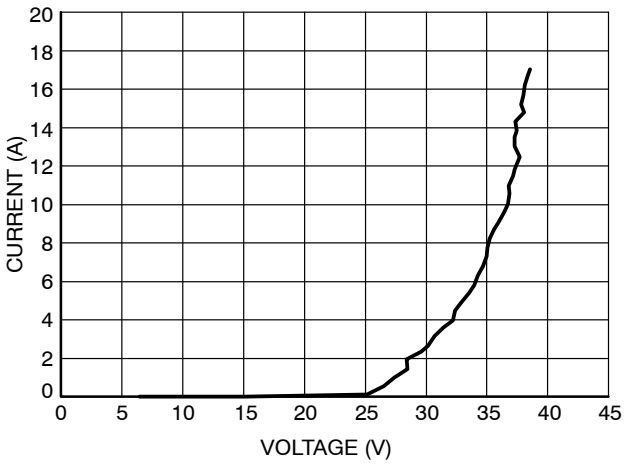


Figure 6. Positive TLP IV Curve

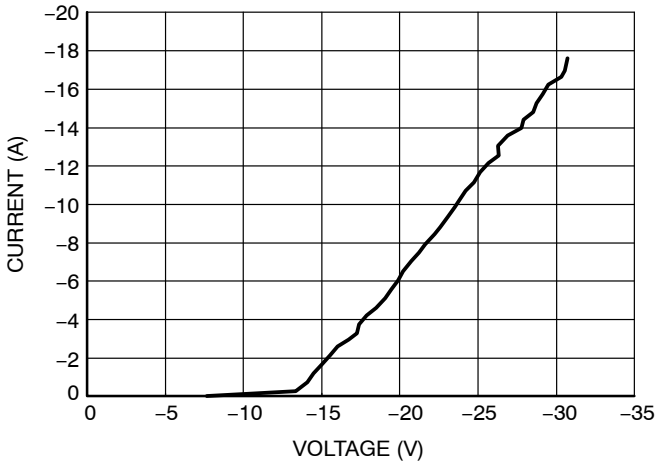


Figure 7. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

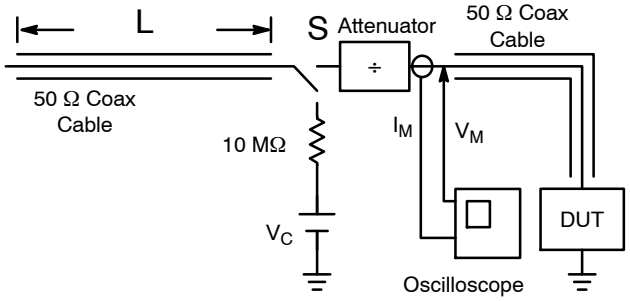


Figure 8. Simplified Schematic of a Typical TLP System

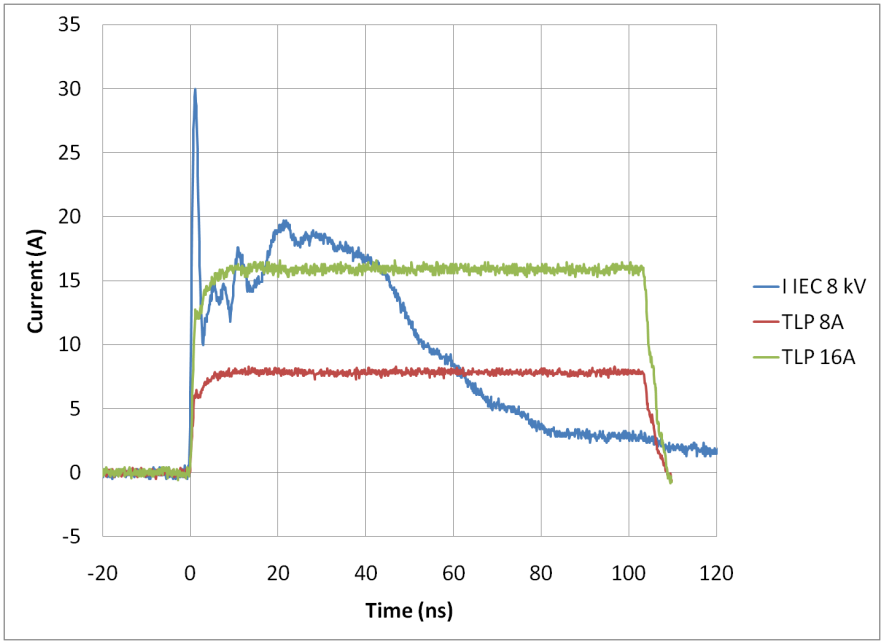


Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

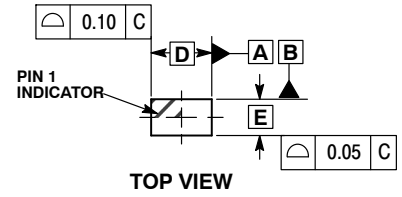
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

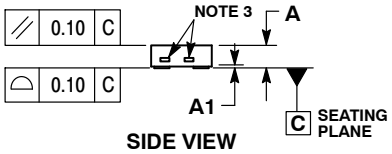
XDFN2 1.0x0.6, 0.65P (SOD−882)
CASE 711AM
ISSUE O

SCALE 8:1

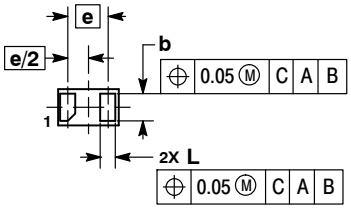
DATE 29 AUG 2012



TOP VIEW

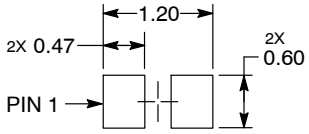


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDER FOOTPRINT*



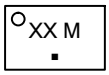
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS	
DIM	MIN	MAX
A	0.34	0.44
A1	−−−	0.05
b	0.43	0.53
D	1.00 BSC	
E	0.60 BSC	
e	0.65 BSC	
L	0.20	0.30

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

DOCUMENT NUMBER:	98AON82886E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	XDFN2 1.0X0.6, 0.65P (SOD−882)	PAGE 1 OF 1

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