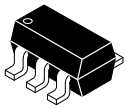
Single and Dual, Rail-to-Rail I/O, CMOS Amplifier

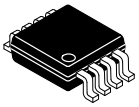
FAN4174, FAN4274

ON Semiconductor®

www.onsemi.com



SOT−23, 5 Lead
CASE 527AH−01



Micro8
CASE 846A−02

Description

The FAN4174 (single) and FAN4274 (dual) are voltage feedback amplifiers with CMOS inputs that consume only 200 μA of supply current per amplifier, while providing ±33 mA of output short−circuit current. These amplifiers are designed to operate 5 V supplies. The common mode voltage range extends beyond the negative and positive rails.

The FAN4174 and FAN4274 are designed on a CMOS process and provide 3.7 MHz of bandwidth and 3 V / μs of slew rate at a supply voltage of 5 V.

These amplifiers operate and are reliable over a wide temperature range of −40°C to +125°C.

The combination of extended temperature operation, low power, rail−to−rail performance, low−voltage operation, and a tiny package optimize this amplifier family for use in many industrial, general−purpose, and battery−powered applications.

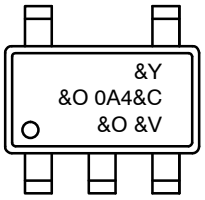
Features

- 200 μA Supply Current per Amplifier
- 3.7 MHz Bandwidth
- Output Swing to Within 10 mV of Either Rail
- Input Voltage Range Exceeds the Rails
- 3 V/μs Slew Rate
- 25 nV/√Hz Input Voltage Noise
- Replaces KM4170 and KM4270
- FAN4174 Competes with OPA340 and TLV2461; Available in a SOT23−5 Package
- FAN4274 Competes with OPA2340 and TLV2462; Available in MSOP−8 Package
- Fully Specified at +5 V Supplies
- These are Pb−Free Devices

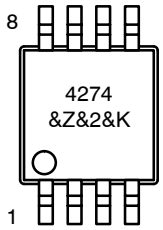
Applications

- Motor Control
- Portable / Battery−powered Applications
- PCMCIA, USB
- Mobile Communications, Cellular Phones, Pagers
- Notebooks and PDAs
- Sensor Interface
- A/D Buffer
- Active Filters
- Signal Conditioning
- Portable Test Instruments

MARKING DIAGRAM



0A4	= Specific Device Code
&Y	= Binary Year Coding
&O	= Plant Code Identifier
&C	= Single Digit Die Run Code
&V	= Eight−Week Data Coding



4274	= Specific Device Code
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

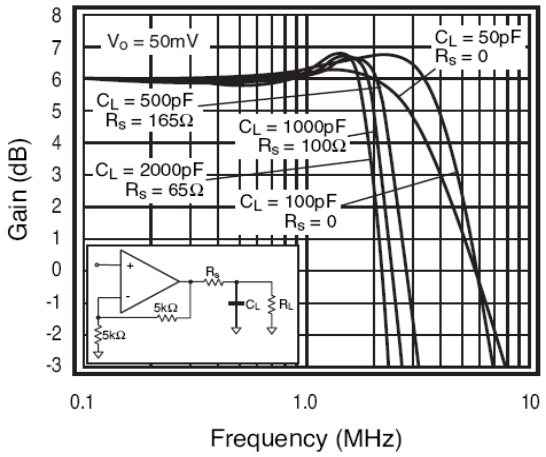


Figure 1. Frequency vs. Gain

TYPICAL APPLICATION

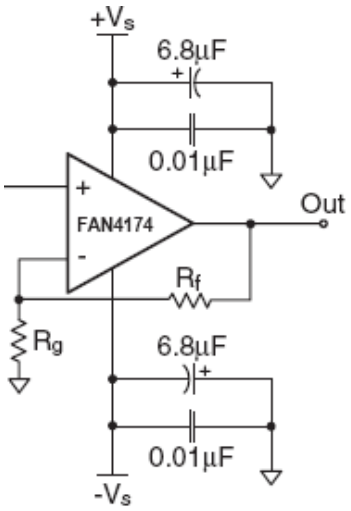


Figure 2. Typical Application Circuit

PIN CONFIGURATIONS

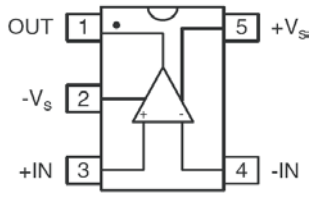


Figure 3. FAN4174 (SOT23)

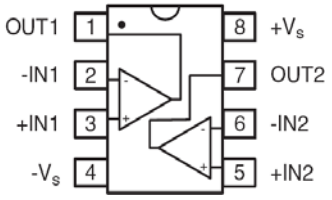


Figure 4. FAN4274 (MSOP)

FAN4174 PIN ASSIGNMENTS

Pin No.	Name	Description
1	OUT	Output
2	$-V_S$	Negative Supply
3	+IN	Positive Supply
4	−IN	Negative Input
5	$+V_S$	Positive Supply

FAN4274 PIN ASSIGNMENTS

Pin No.	Name	Description
1	OUT1	Output, Channel 1
2	−IN1	Negative Input, Channel 1
3	+IN1	Positive Input, Channel 1
4	$-V_S$	Negative Supply
5	+IN2	Positive Input, Channel 2
6	−IN2	Negative Input, Channel 2
7	OUT2	Output, Channel 2
8	$+V_S$	Positive Supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		0	6	V
V_{IN}	Input Voltage Range		$-V_S - 0.5$	$+V_S + 0.5$	V
T_J	Junction Temperature		−	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering, 10 Seconds		−	+300	°C
Θ_{JA}	Thermal Resistance (Note 1)	5−Lead SOT23	−	256	°C/W
		8−Lead MSOP	−	206	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Package thermal resistance JEDEC standard, multi−layer test boards, still air.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$+V_s$	Supply Voltage	2.30	5.25	V
T_A	Operating Temperature Range	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL SPECIFICATIONS AT +2.7 V (V_S = +2.7 V, G = 2, R_L = 10 kΩ to V_S / 2, R_F = 5 kΩ; unless otherwise noted)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN RESPONSE							
UGBW	−3 dB Bandwidth		G = +1	–	4.0	–	MHz
BW_{SS}				–	2.5	–	MHz
GBWP	Gain Bandwidth Product			–	4	–	MHz
TIME DOMAIN RESPONSE							
t_R, f_F	Rise and Fall Time		V_O = 1.0 V Step	–	300	–	ns
OS	Overshoot		V_O = 1.0 V Step	–	5	–	%
SR	Slew Rate		V_O = 3 V Step, G = −1	–	3	–	V/μs
DISTORTION AND NOISE RESPONSE							
HD2	2nd Harmonic Distortion		V_O = 1 V_{PP}, 10 kHz	–	−66	–	dBc
HD3	3rd Harmonic Distortion		V_O = 1 V_{PP}, 10 kHz	–	−67	–	dBc
THD	Total Harmonic Distortion		V_O = 1 V_{PP}, 10 kHz	–	0.1	–	%
e_n	Input Voltage Noise			–	26	–	nV/√Hz
X_{TALK}	Crosstalk (FAN4274)		100 kHz	–	−100	–	dB
DC PERFORMANCE							
V_{IO}	Input Offset Voltage (Note 2)			−6	0	+6	mV
dV_{IO}	Average Drift			–	2.1	–	μV/°C
I_{bn}	Input Bias Current			–	5	–	pA
PSRR	Power Supply Rejection Ratio (Note 2)		DC	50	73	–	dB
A_{OL}	Open−loop Gain		DC	–	98	–	dB
I_S	Supply Current per Amplifier (Note 2)			–	200	300	μA
INPUT CHARACTERISTICS							
R_{IN}	Input Resistance			–	10	–	GΩ
C_{IN}	Input Capacitance			–	1.4	–	pF
CMIR	Input Common Mode Voltage Range			–	−0.3 to 2.8	–	V
CMRR	Common Mode Rejection Ratio (Note 2)	FAN4174	DC, V_{CM} = 0 V to 2.2 V	50	65	–	dB
		FAN4274	DC, V_{CM} = 0 V to 2.2 V	50	65	–	
OUTPUT CHARACTERISTICS							
V_O	Output Voltage Swing (Note 2)		R_L=10 kΩ to V_S / 2	0.03	0.01 to 2.69	2.65	V
			R_L = 1 kΩ to V_S / 2	–	0.05 to 2.55	–	
I_{SC}	Short−Circuit Output Current			–	+34 / −12	–	mA
V_S	Power Supply Operating Range			–	2.5 to 5.5	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. 100% tested at 25°C.

ELECTRICAL SPECIFICATIONS AT +5 V (V_S = +5 V, G = 2, R_L = 10 kΩ to V_S / 2, R_F = 5 kΩ; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN RESPONSE						
UGBW	−3dB Bandwidth	G = +1, T_A = 85°C	–	3.7	–	MHz
		G = +1, T_A = 125°C	–	3.2	–	
BW_{SS}			–	2.3	–	MHz
GBWP	Gain Bandwidth Product	T_A = 85°C	–	3.7	–	MHz
		T_A = 125°C	–	3.2	–	
TIME DOMAIN RESPONSE						
t_R, f_F	Rise and Fall Time	V_O = 1.0 V Step	–	300	–	ns
OS	Overshoot	V_O = 1.0 V Step	–	5	–	%
SR	Slew Rate	V_O = 3 V Step, G = −1	–	3	–	V/μs
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	V_O = 1 V_{PP}, 10 kHz	–	−80	–	dBc
HD3	3rd Harmonic Distortion	V_O = 1 V_{PP}, 10 kHz	–	−80	–	dBc
THD	Total Harmonic Distortion	V_O = 1 V_{PP}, 10 kHz	–	0.02	–	%
e_n	Input Voltage Noise		–	25	–	nV/√Hz
X_{TALK}	Crosstalk (FAN4274)	100 kHz	–	−100	–	dB
DC PERFORMANCE						
V_{IO}	Input Offset Voltage[3]		−8	0	+8	mV
dV_{IO}	Average Drift		–	2.9	–	μV/°C
I_{bn}	Input Bias Current		–	5	–	pA
PSRR	Power Supply Rejection Ratio (Note 3)	DC	50	73	–	dB
A_{OL}	Open−loop Gain	DC	–	102	–	dB
I_S	Supply Current per Amplifier[3]		–	200	300	μA
INPUT CHARACTERISTICS						
R_{IN}	Input Resistance		–	10	–	GW
C_{IN}	Input Capacitance		–	1.2	–	pF
CMIR	Input Common Mode Voltage Range		–	−0.3 to 5.1	–	V
CMRR	Common Mode Rejection Ratio (Note 3)	DC, V_{CM} = 0 V to V_S	58	73	–	dB
OUTPUT CHARACTERISTICS						
V_O	Output Voltage Swing (Note 3)	R_L = 10 kΩ to V_S / 2	0.03	0.01 to 4.99	4.95	V
		R_L = 1 kΩ to V_S / 2	–	0.1 to 4.9	–	
I_{SC}	Short−Circuit Output Current		–	±33	–	mA
V_S	Power Supply Operating Range		–	2.5 to 5.5	–	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. 100% tested at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_S = +2.7 V, G = 2, R_L = 10 kΩ to V_S / 2, R_F = 5 kΩ; unless otherwise noted)

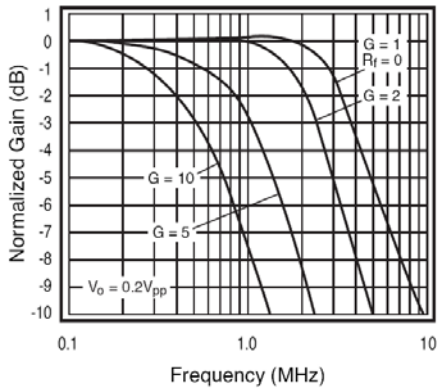


Figure 5. Non−Inverting Frequency Response (+5 V)

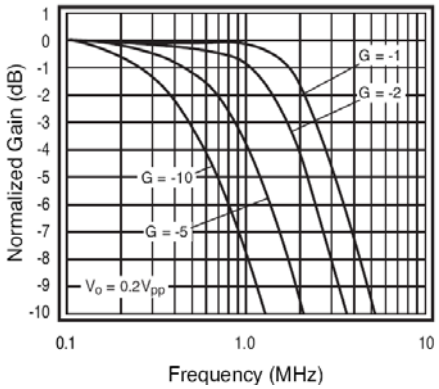


Figure 6. Inverting Frequency Response (+5 V)

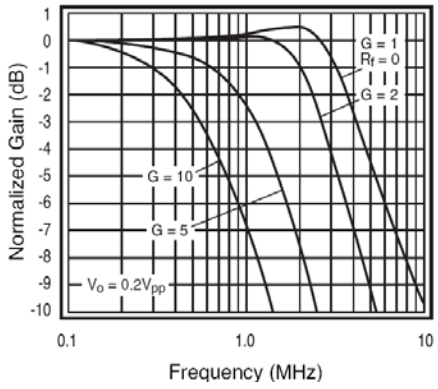


Figure 7. Non−Inverting Frequency Response

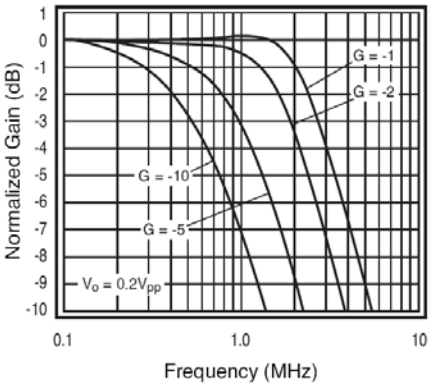


Figure 8. Inverting Frequency Response

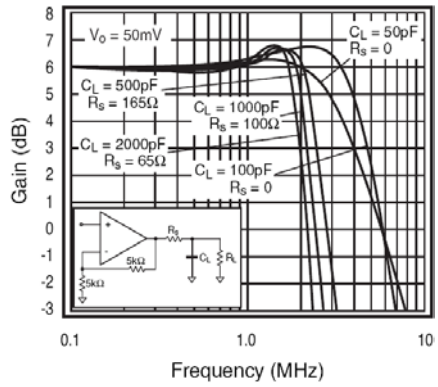


Figure 9. Frequency Response vs. C_L

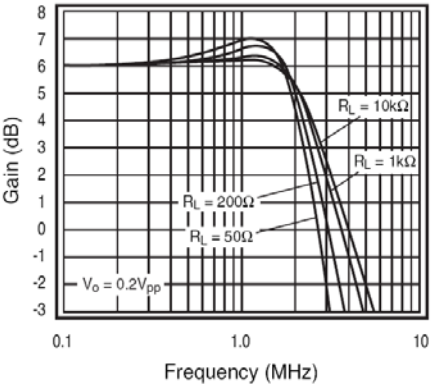


Figure 10. Open−loop Gain and Phase vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

(V_S = +2.7 V, G = 2, R_L = 10 kΩ to V_S / 2, R_F = 5 kΩ; unless otherwise noted) (continued)

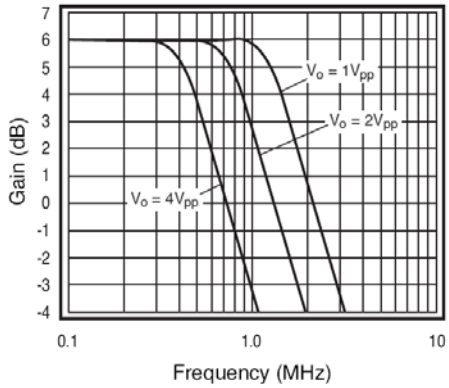


Figure 11. Large Signal Frequency Response (+5 V)

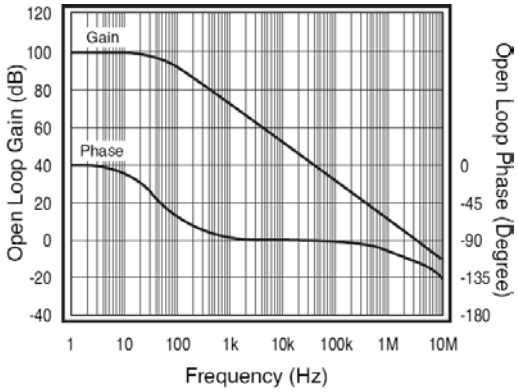


Figure 12. Open−loop Gain and Phase vs. Frequency

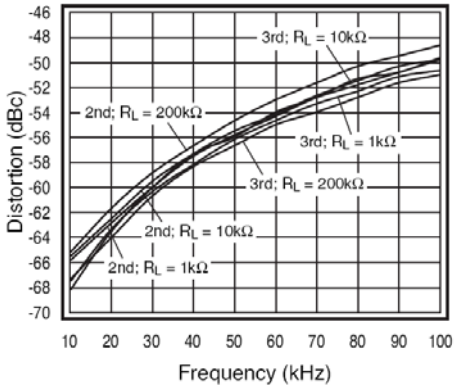


Figure 13. 2nd and 3rd Harmonic Distortion

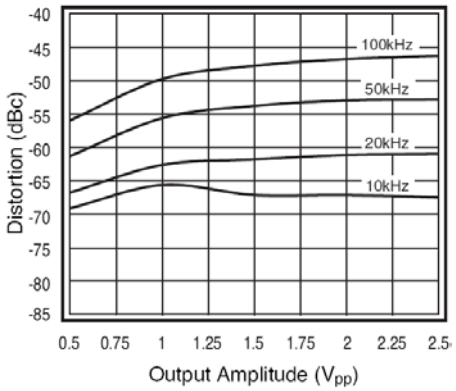


Figure 14. 2nd Harmonic Distortion vs. V_O

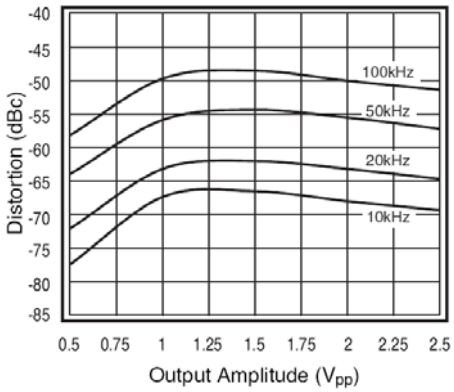


Figure 15. 3rd Harmonic Distortion vs. V_O

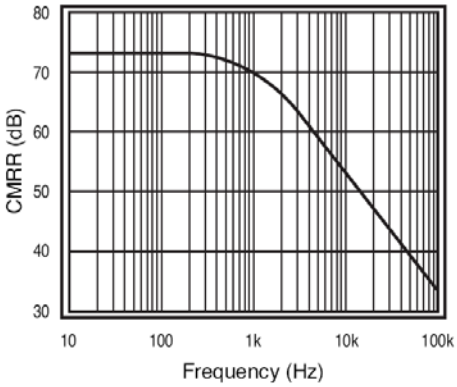


Figure 16. CMRR V_S = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

(V_S = +2.7 V, G = 2, R_L = 10 kΩ to V_S / 2, R_F = 5 kΩ; unless otherwise noted) (continued)

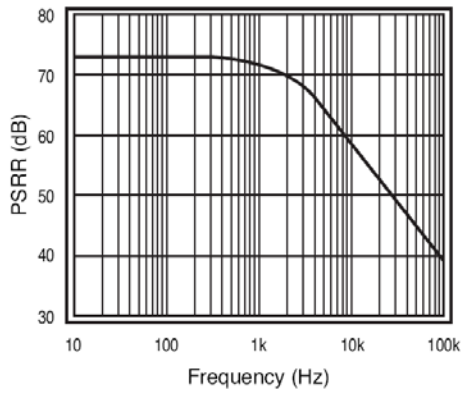


Figure 17. PSRR V_S = 5 V

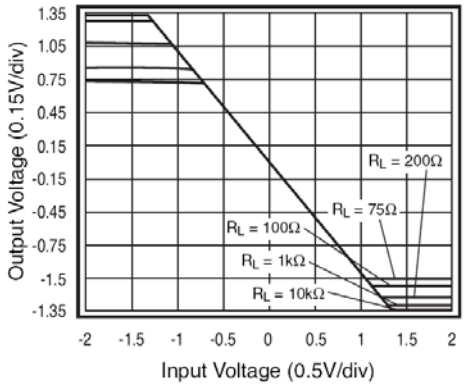


Figure 18. Output Swing vs. Load

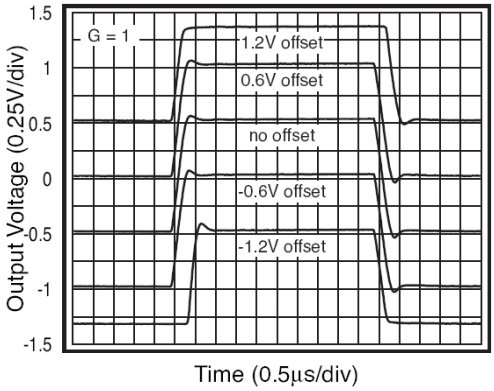


Figure 19. Pulse Response vs. Common−Mode Voltage

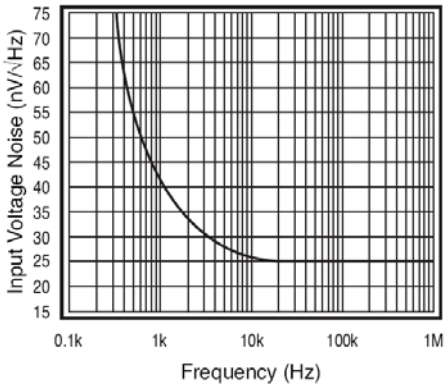


Figure 20. Input Voltage Noise

APPLICATION INFORMATION

General Description

The FAN4174 amplifier includes single−supply, general−purpose, voltage−feedback amplifiers, fabricated on a bi−CMOS process. The family features a rail−to−rail input and output and is unity gain stable. The typical non−inverting circuit schematic is shown in Figure 21.

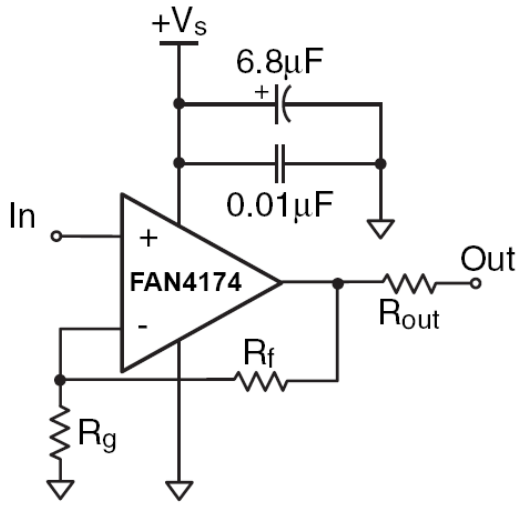


Figure 21. Typical Non−inverting Configuration

Input Common Mode Voltage

The common mode input range extends to 300 mV below ground and to 100 mV above V_S in single supply operation. Exceeding these values does not cause phase reversal; however, if the input voltage exceeds the rails by more than 0.5 V, the input ESD devices begin to conduct. The output stays at the rail during this overdrive condition. If the absolute maximum input V_{IN} (700 mV beyond either rail) is exceeded, externally limit the input current to ±5 mA, as shown in Figure 22.

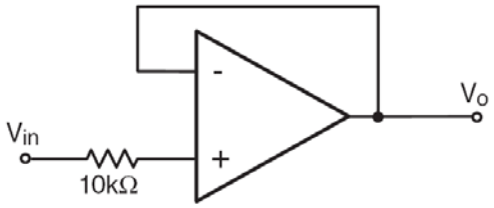


Figure 22. Circuit for Input Current Protection

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, performance degradation occurs. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the range is exceeded. The FAN4174 typically recovers in less than 500 ns from an overdrive condition. Figure 23 shows the FAN4174 amplifier in an overdriven condition.

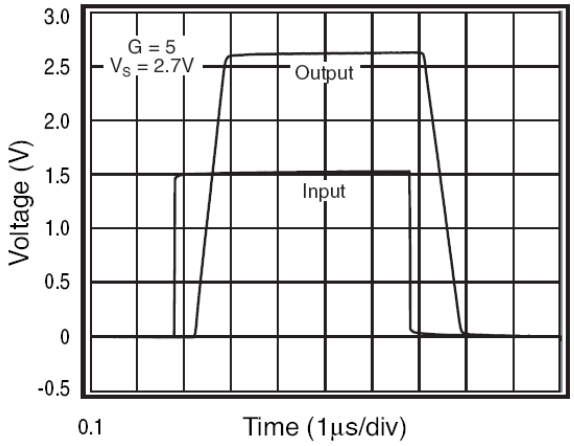


Figure 23. Overdrive Recovery

Driving Capacitive Loads

Figure 9 illustrates the response of the FAN4174 amplifier. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 24, improves stability and settling performance. R_S values in Figure 9 achieve maximum bandwidth with less than 2 dB of peaking. For maximum flatness, use a larger R_S. Capacitive loads larger than 500 pF require the use of R_S.

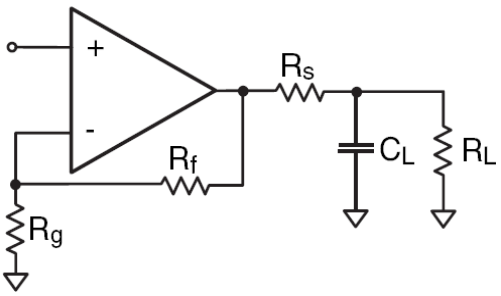


Figure 24. Typical Topology for Driving a Capacitive Load

Driving a capacitive load introduces phase−lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the FAN4174 amplifier requires a 300 Ω series resistor to drive a 100 pF load.

LAYOUT CONSIDERATIONS

General layout and supply bypassing play major roles in high−frequency performance. ON Semiconductor evaluation boards help guide high−frequency layout and aid in device testing and characterization. Follow the steps below as a basis for high−frequency layout:

1. Include 6.8 μF and 0.01 μF ceramic capacitors.
2. Place the 6.8 μF capacitor within 19.05 mm (0.75 inches) of the power pin.
3. Place the 0.01 μF capacitor within 2.54 mm (0.1 inches) of the power pin.
4. Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.

Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown in Figure 27 through Figure 30 for more information.

When evaluating only one channel, complete the following on the unused channel:

1. Ground the non−inverting input.
2. Short the output to the inverting input.

EVALUATION BOARD INFORMATION

The following evaluation boards are available to aid in the testing and layout of this device:

Table 1.

Board	Description	Product
KEB002	Single Channel, Dual Supply, 5 and 6−Lead SOT23	FAN4174IS5X
KEB010	Dual Channel, Dual Supply 8−Lead MSOP	FAN4274IMU8X

Evaluation board schematics are shown in Figure 25 and Figure 26; layouts are shown in Figure 27 through Figure 30.

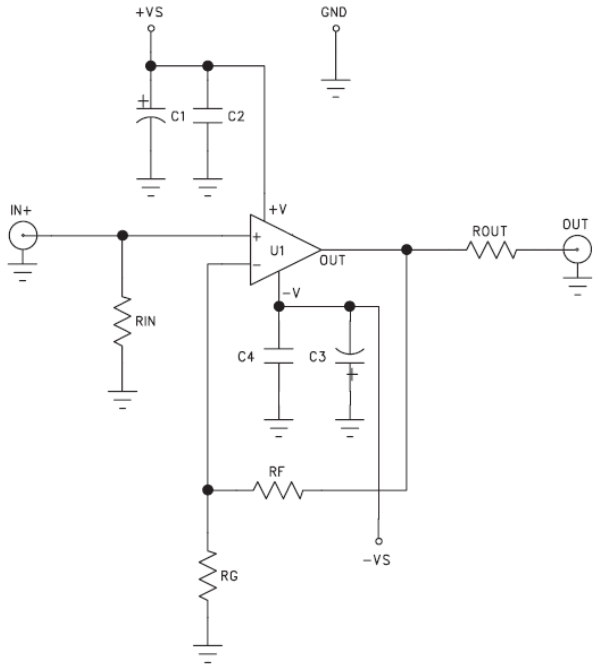


Figure 25. FAN4174 Evaluation Board Schematic (KEV002)

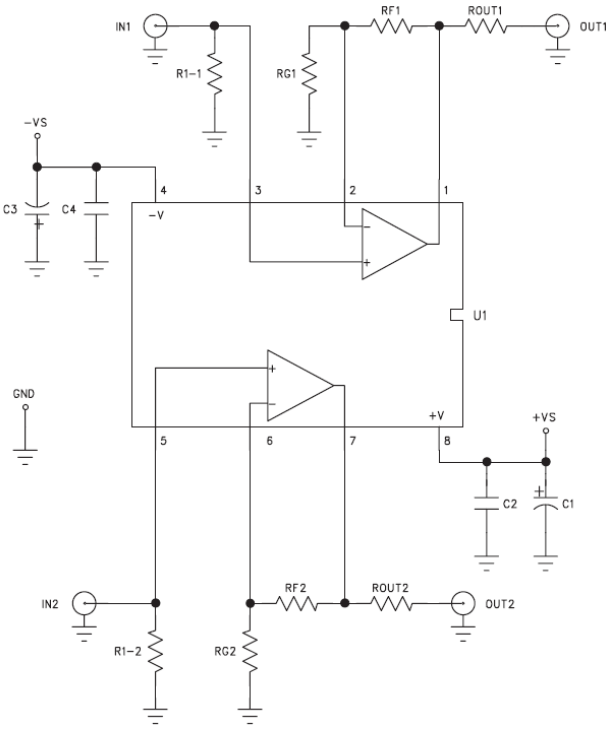


Figure 26. FAN4274 Evaluation Board Schematic (KEB010)

BOARD LAYOUT INFORMATION

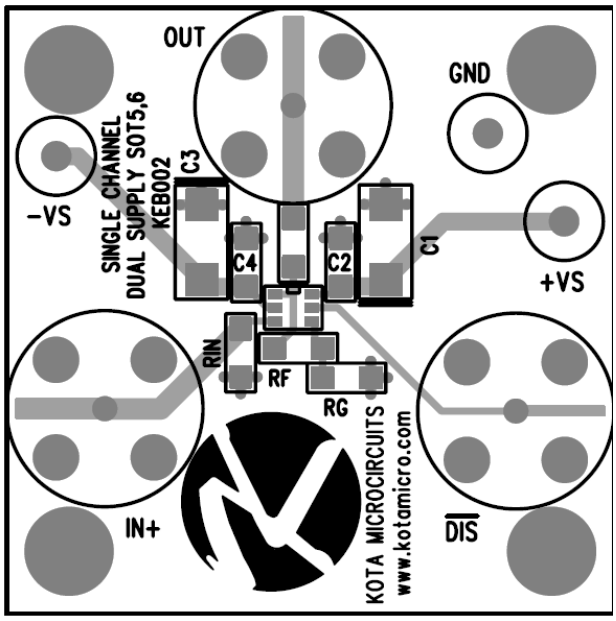


Figure 27. KEB002 (Top Side)

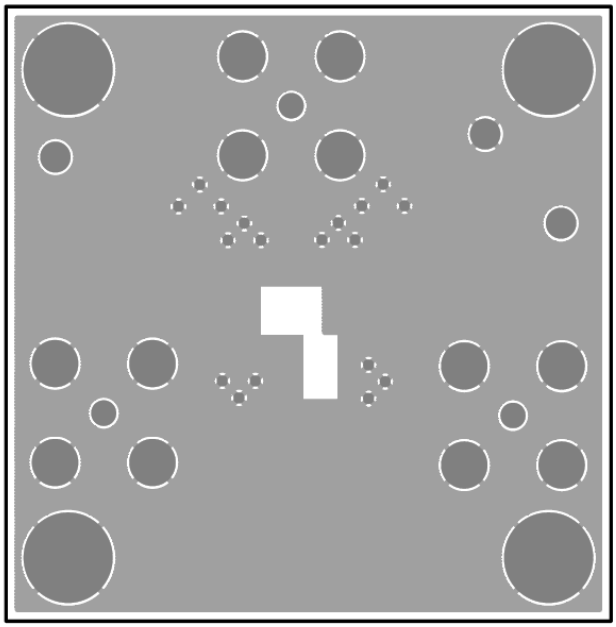


Figure 28. KEB002 (Bottom Side)

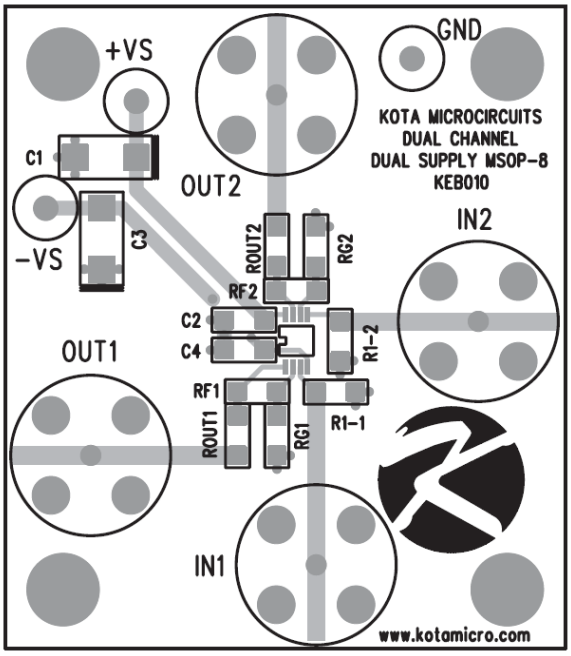


Figure 29. KEB010 (Top Side)

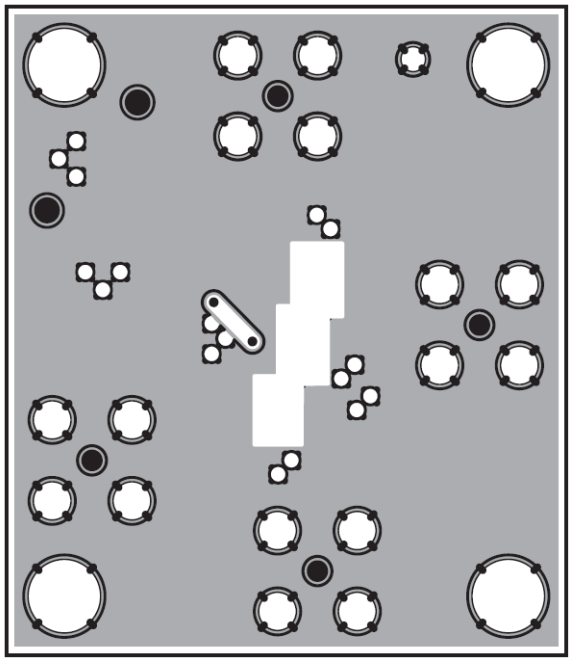
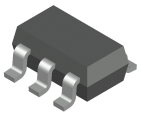


Figure 30. KEB010 (Bottom Side)

ORDERING INFORMATION

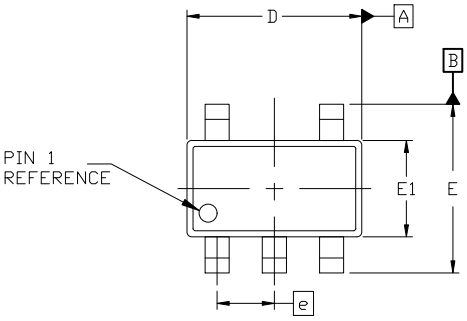
Device	Operating Temperature Range	Package	Shipping†
FAN4174IS5X	−40 to +125°C	SOT−23, 5 Lead (Pb−Free)	3000 / Tape & Reel
FAN4274IMU8X	−40 to +125°C	Micro8, Lead Molded Small−Outline (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

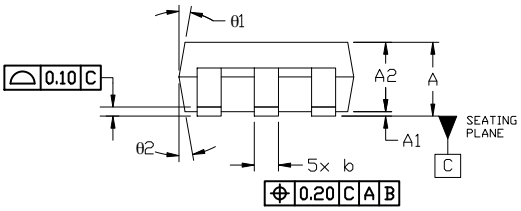


SOT−23, 5 Lead
CASE 527AH
ISSUE A

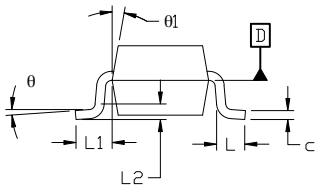
DATE 09 JUN 2021



TOP VIEW



SIDE VIEW

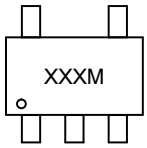


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

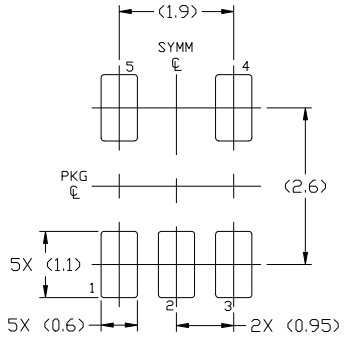
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



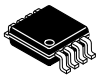
RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON34320E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−23, 5 LEAD**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

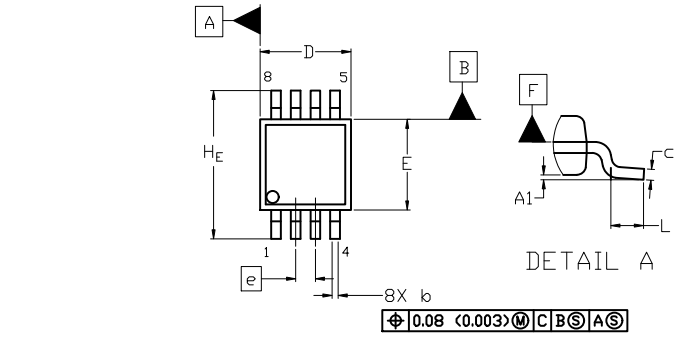
ON Semiconductor®

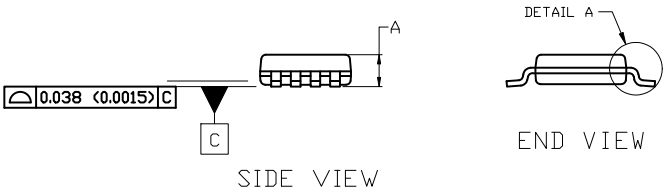


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

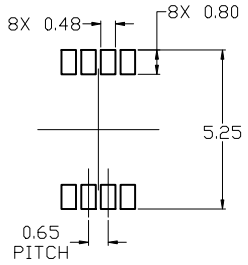
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

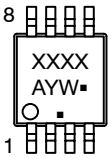


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales