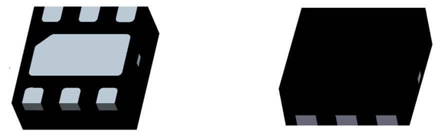
IntelliMAX™ Advanced Load Management Products

FPF1005 - FPF1006

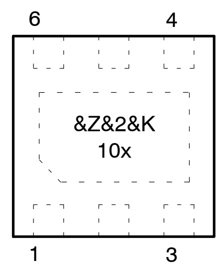
Pin 1



Bottom Top

WDFN6 2x2, 0.65P
CASE 511CY

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code (Year and Week)
&K = 2−Digit Lot Run Traceability Code
10x = Device Code (x = 5, 6,)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The FPF1005 & FPF1006 are low R_{DS} P−Channel MOSFET load switches with CMOS controlled turn−on targeting small package load switch applications. The input voltage range operates from 1.2 V to 5.5 V. Switch control is by a logic input (ON) capable of interfacing directly with low voltage control signals. In FPF1006, 120 Ω on−chip load resistor is added for output quick discharge when switch is turned off.

Both FPF1005 & FPF1006 are available in a small 2X2 MicroFET−6 pin plastic package.

Features

- 1.2 to 5.5 V Input Voltage Range
- Typical $R_{DS(ON)}$ = 50 mΩ @ V_{IN} = 5.5 V
- Typical $R_{DS(ON)}$ = 55 mΩ @ V_{IN} = 3.3 V
- ESD Protected, above 2000 V HBM
- These Devices are Pb−Free and are RoHS Compliant

Applications

- PDAs
- Cell Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Hot Swap Supplies
- RoHS Compliant

ORDERING INFORMATION

Part Number	Switch	Input Buffer	Output Discharge	ON Pin Activity	Package	Shipping†
FPF1005	55 mΩ, PMOS	Schmitt	NA	Active HIGH	(WDFN6), 2x2, 0.65P	3000 / Tape & Reel
FPF1006	55 mΩ, PMOS	Schmitt	120 Ω	Active HIGH	(WDFN6), 2x2, 0.65P	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL APPLICATION CIRCUIT

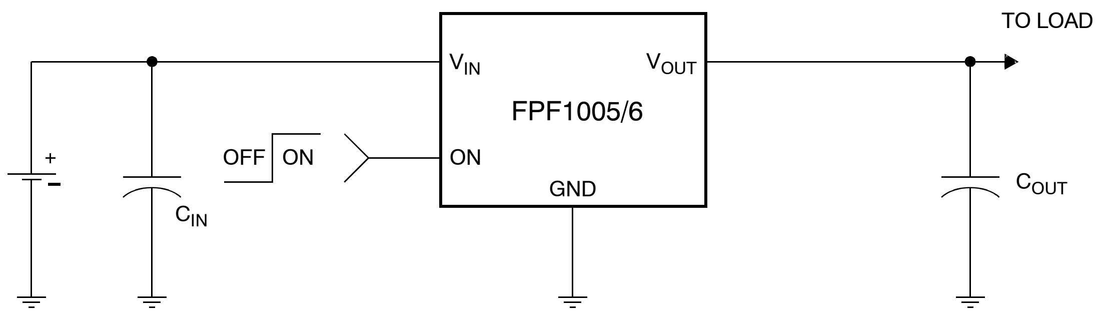


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

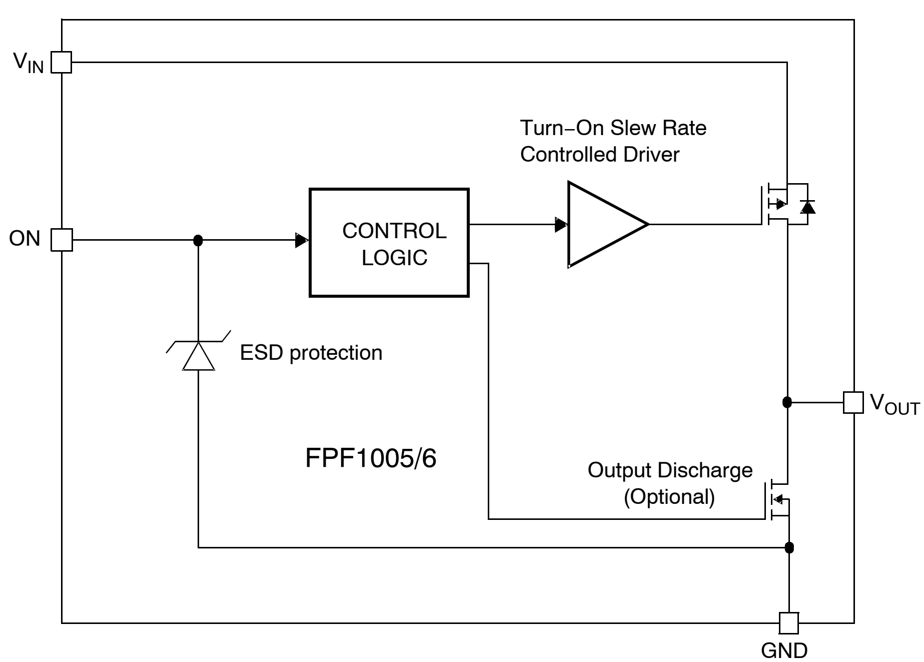


Figure 2. Functional Block Diagram

PIN CONFIGURATION

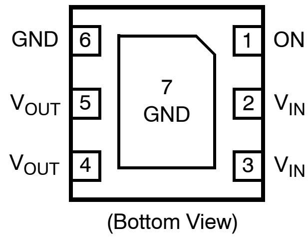


Figure 3. Pin Configuration

PIN DESCRIPTION

Pin	Name	Function
4, 5	V_{OUT}	Switch Output: Output of the power switch
2, 3	V_{IN}	Supply Input: Input to the power switch and the supply voltage for the IC
6, 7	GND	Ground
1	ON	ON/OFF Control Input

ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
V_{IN}, V_{OUT}, ON to GND		−0.3	6	V
Maximum Continuous Switch Current		–	1.5	A
Power Dissipation @ T_A = 25°C (Note 1)		–	1.2	W
Operating Temperature Range		−40	85	°C
Storage Temperature		−65	150	°C
Thermal Resistance, Junction to Ambient		–	86	°C/W
Electrostatic Discharge Protection	HBM	2000	–	V
	MM	200	–	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Package power dissipation on 1 square inch pad, 2 oz. copper board.

RECOMMENDED OPERATING RANGE

Parameter	Min	Max	Unit
V_{IN}	1.2	5.5	V
Ambient Operating Temperature, T_A	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = 1.2 to 5.5 V, T_A = −40 to +85°C unless otherwise noted. Typical values are at V_{IN} = 3.3 V and T_A = 25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BASIC OPERATION						
Operating Voltage	V_{IN}		1.2	–	5.5	V
Quiescent Current	I_Q	I_{OUT} = 0 mA, V_{IN} = V_{ON}	–	–	1	μA
Off Supply Current	$I_{Q(off)}$	V_{ON} = GND, OUT = open	–	–	1	μA
Off Switch Current	$I_{SD(off)}$	V_{ON} = GND, V_{OUT} = 0 V, @ V_{IN} = 5.5 V, T_A = 85°C	–	–	1	μA
		V_{ON} = GND, V_{OUT} = 0 V, @ V_{IN} = 3.3 V, T_A = 25°C	–	10	100	nA
On−Resistance	R_{ON}	V_{IN} = 5.5 V, T_A = 25°C	–	50	70	mΩ
		V_{IN} = 3.3 V, T_A = 25°C	–	55	80	
		V_{IN} = 1.5 V, T_A = 25°C	–	95	135	
		V_{IN} = 1.2 V, T_A = 25°C	–	165	250	
Output Pull Down Resistance	R_{PD}	V_{IN} = 3.3 V, V_{ON} = 0 V, T_A = 25°C, FPF1006	–	75	120	Ω
ON Input Logic Low Voltage	V_{IL}	V_{IN} = 5.5 V	–	–	1.25	V
		V_{IN} = 4.5 V	–	–	1.10	
		V_{IN} = 1.5 V	–	–	0.50	
ON Input Logic High Voltage	V_{IH}	V_{IN} = 5.5 V	2.00	–	–	V
		V_{IN} = 4.5 V	1.75	–	–	
		V_{IN} = 1.5 V	0.75	–	–	
ON Input Leakage		V_{ON} = V_{IN} or GND	−1	–	1	μA
DYNAMIC						
Turn On Delay	t_{ON}	V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, T_A = 25°C	–	10	–	μs
Turn Off Delay	t_{OFF}	V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, T_A = 25°C, FPF1005	–	50	–	μs
		V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, R_{L_CHIP} =120 Ω, T_A = 25°C, FPF1006	–	10	–	
V_{OUT} Rise Time	t_R	V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, T_A = 25°C	–	10	–	μs
V_{OUT} Fall Time	t_F	V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, T_A = 25°C, FPF1005	–	100	–	μs
		V_{IN} = 3.3 V, R_L = 500 Ω, C_L = 0.1 μF, R_{L_CHIP} =120 Ω, T_A = 25°C, FPF1006	–	10	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

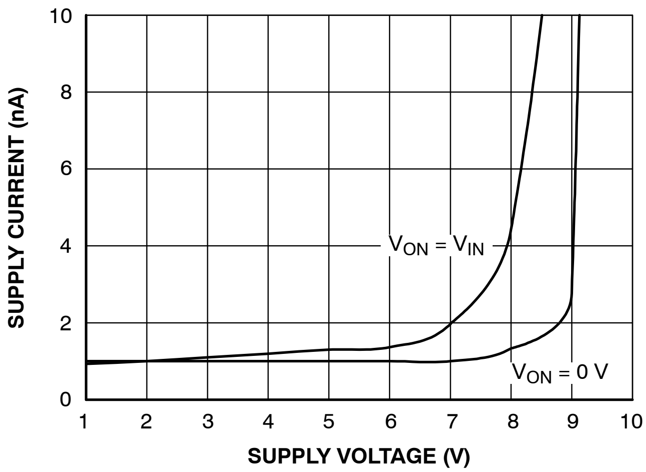


Figure 4. Quiescent Current vs. V_{IN}

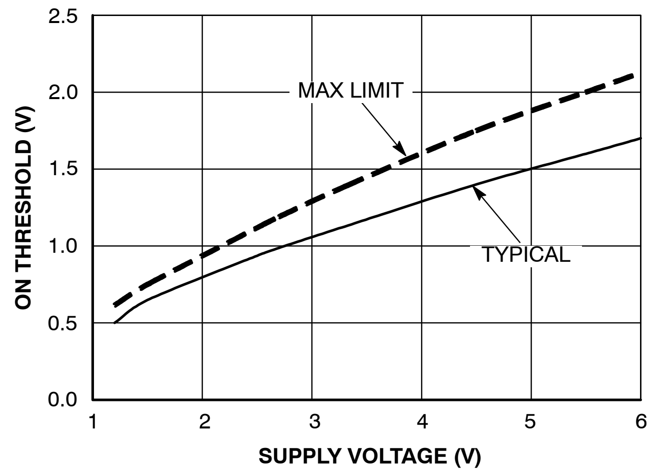


Figure 5. ON Threshold vs. V_{IN}

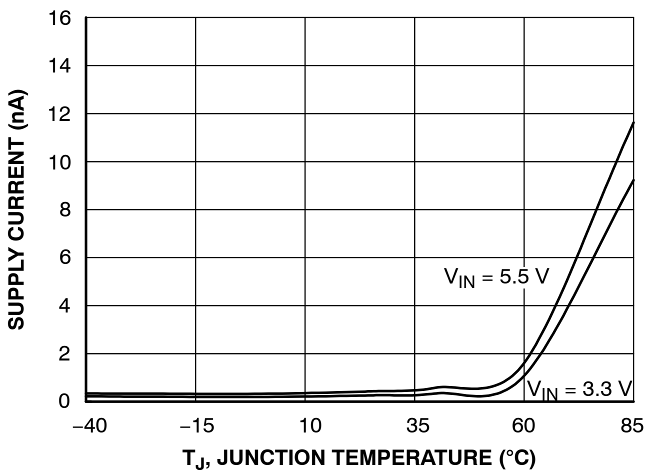


Figure 6. Quiescent Current vs. Temperature

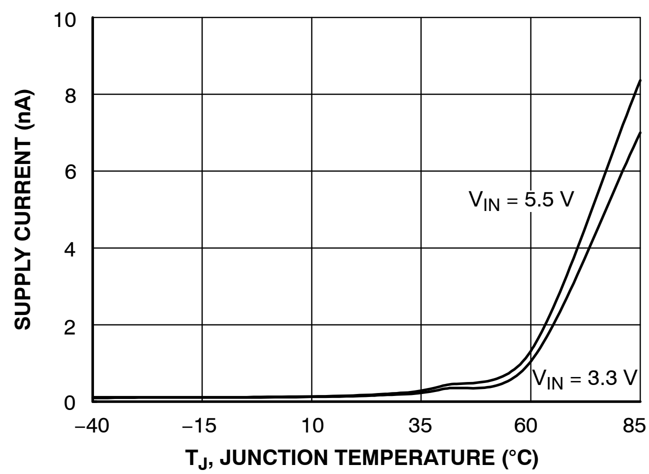


Figure 7. Quiescent Current (off) vs. Temperature

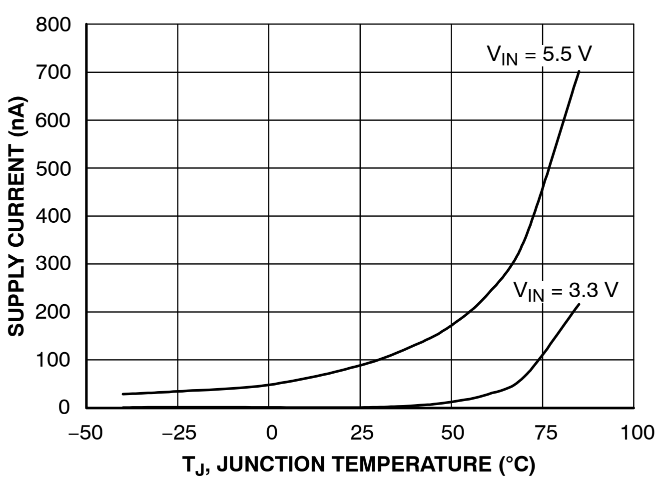


Figure 8. $I_{SWITCH-OFF}$ Current vs. Temperature

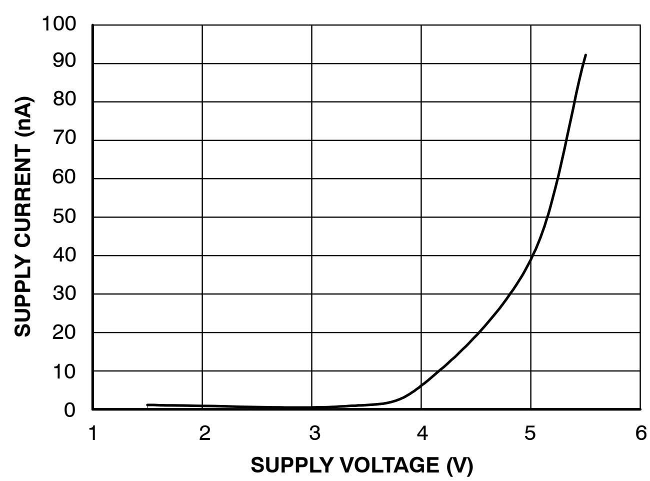


Figure 9. $I_{SWITCH-OFF}$ Current vs. V_{IN}

TYPICAL CHARACTERISTICS (continued)

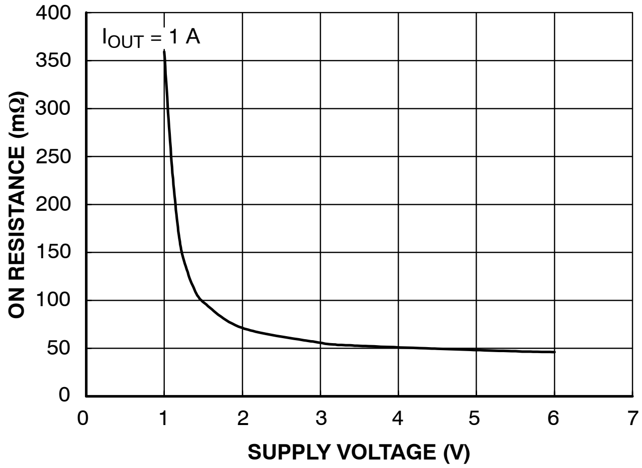


Figure 10. R_{ON} vs. V_{IN}

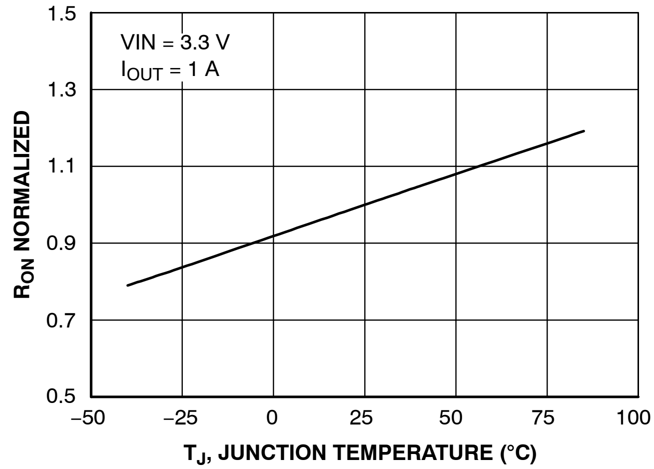


Figure 11. R_{ON} vs. Temperature

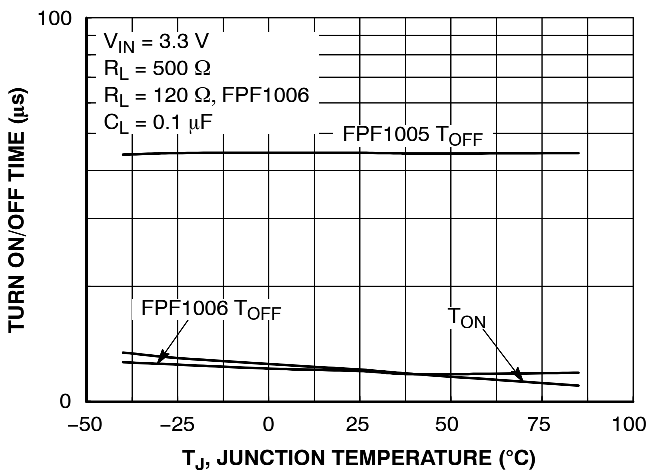


Figure 12. T_{ON}/T_{OFF} vs. Temperature

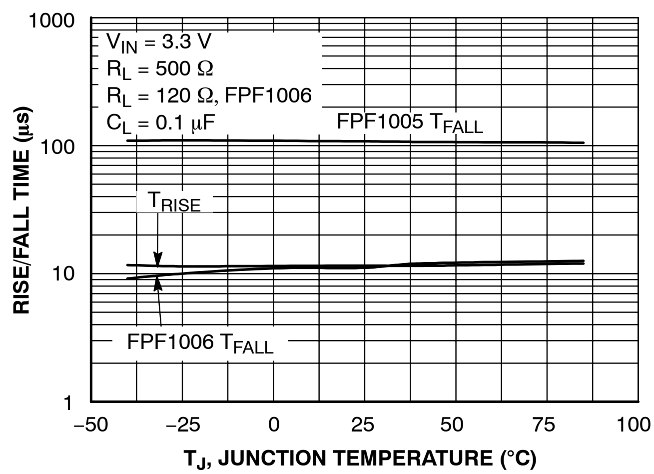


Figure 13. T_{RISE}/T_{FALL} vs. Temperature

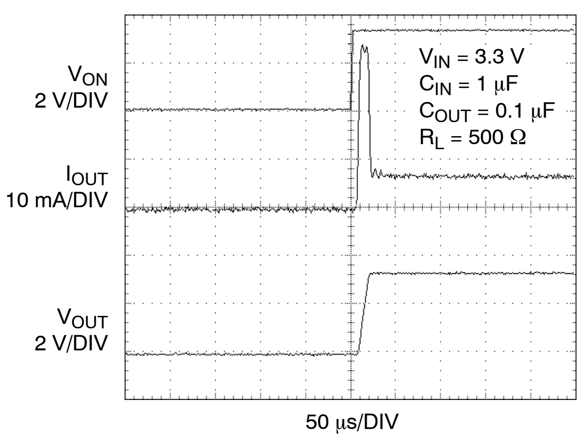


Figure 14. FPF1005 T_{ON} Response

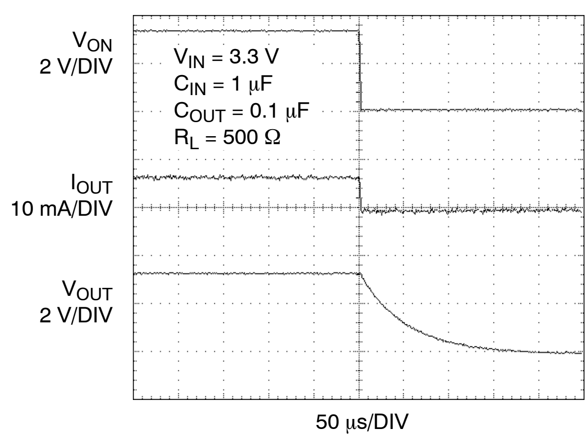


Figure 15. FPF1005 T_{OFF} Response

TYPICAL CHARACTERISTICS (continued)

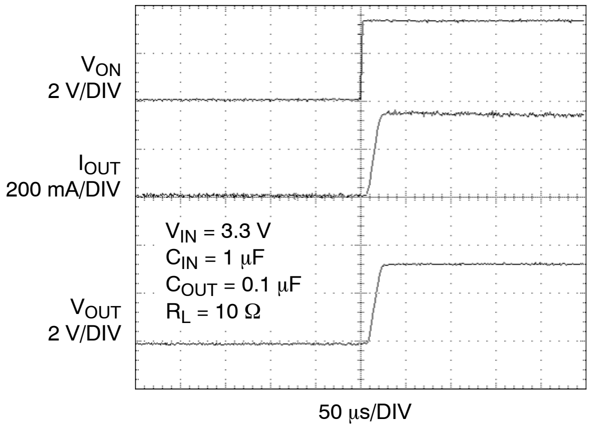


Figure 16. FPF1005 T_{ON} Response

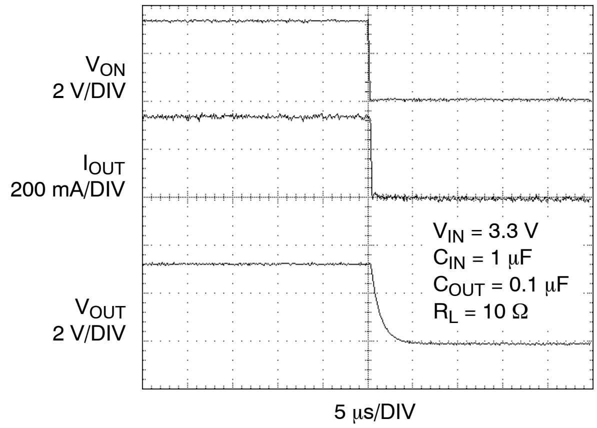


Figure 17. FPF1005 T_{OFF} Response

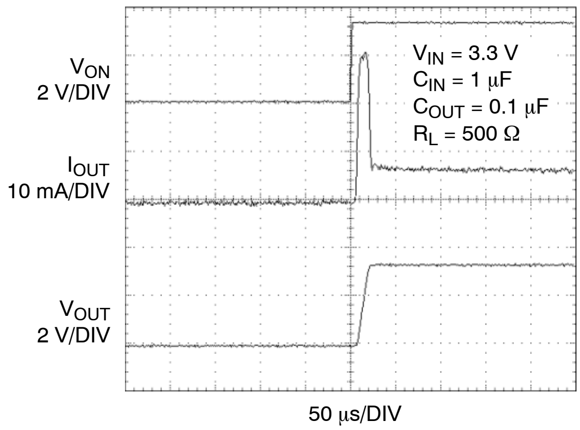


Figure 18. FPF1006 T_{ON} Response

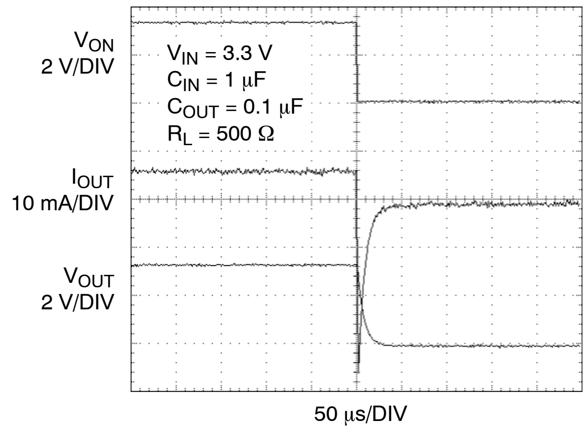


Figure 19. FPF1006 T_{OFF} Response

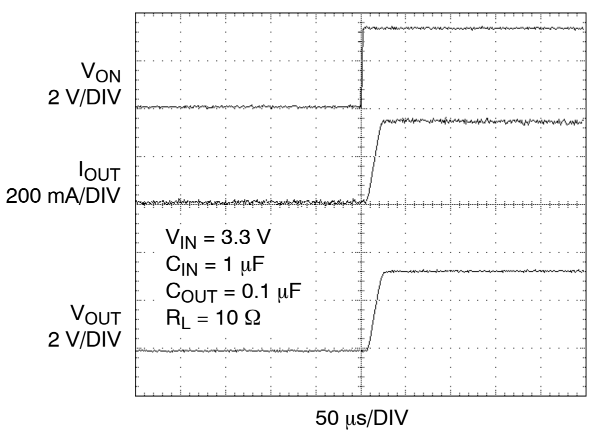


Figure 20. FPF1006 T_{ON} Response

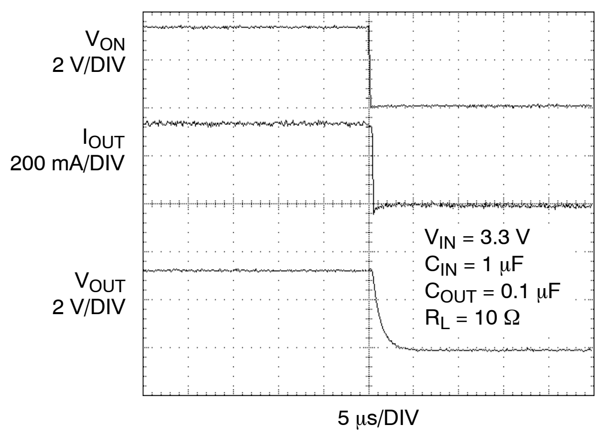


Figure 21. FPF1006 T_{OFF} Response

DESCRIPTION OF OPERATION

The FPF1005 & FPF1006 are low $R_{DS(ON)}$ P−Channel load switches with controlled turn−on. The core of each device is a 55 mΩ P−Channel MOSFET and a controller capable of functioning over a wide input operating range of 1.2−5.5 V. The ON pin, an active HI TTL compatible input, controls the state of the switch. The FPF1006 contains a 120 Ω on−chip load resistor for quick output discharge when the switch is turned off.

However, V_{OUT} pin of FPF1006 should not be connected directly to the battery source due to the discharge mechanism of the load switch.

APPLICATION INFORMATION

Typical Application

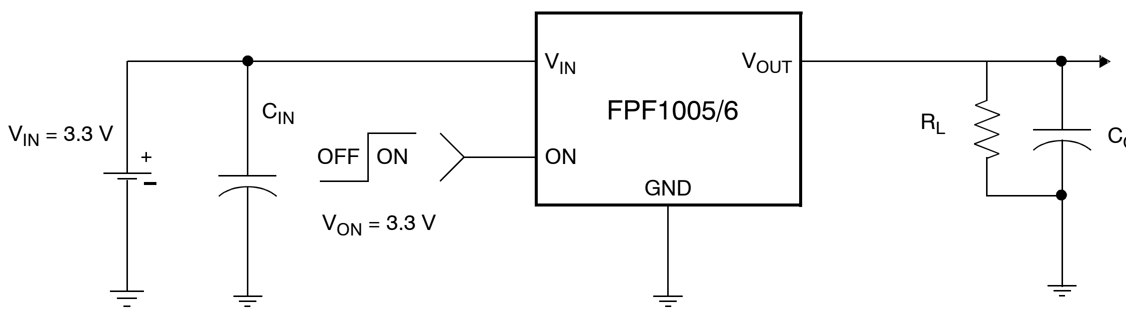


Figure 22. Typical Application

Input Capacitor

To limit the voltage drop on the input supply caused by transient in−rush currents when the switch turns−on into a discharged load capacitor or a short−circuit, a capacitor needs to be placed between V_{IN} and GND. A 1 μF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during higher current application.

Output Capacitor

A 0.1 μF capacitor, C_{OUT}, should be placed between V_{OUT} and GND. This capacitor will prevent parasitic board inductance from forcing V_{OUT} below GND when the switch turns−off. Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_{OUT} is highly recommended. A C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductance may have on normal and short−circuit operation. Using wide traces or large copper planes for all pins (V_{IN}, V_{OUT}, ON and GND) will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Evaluation Board Layout

FPF1005/6 Demo board has the components and circuitry to demonstrate the load switch functions. Thermal performance of the load switch can be improved significantly by connecting the middle pad (pin 7) to the GND area of the PCB.

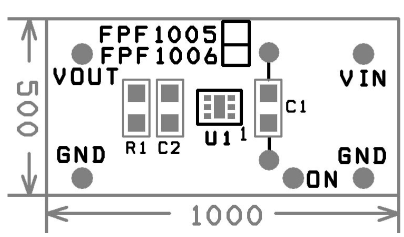


Figure 23. Demo Board Silk Screen Top and Component Assembly Drawing

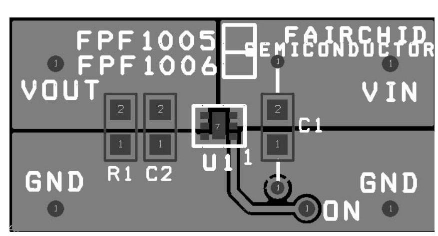


Figure 24. Demo Board Top and Surface Mount Top Layers View (Pin 7 is Connected to GND)

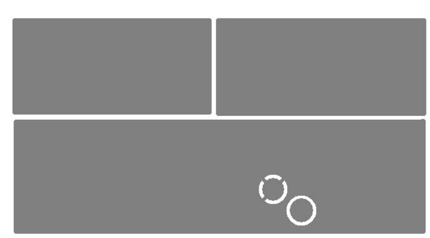
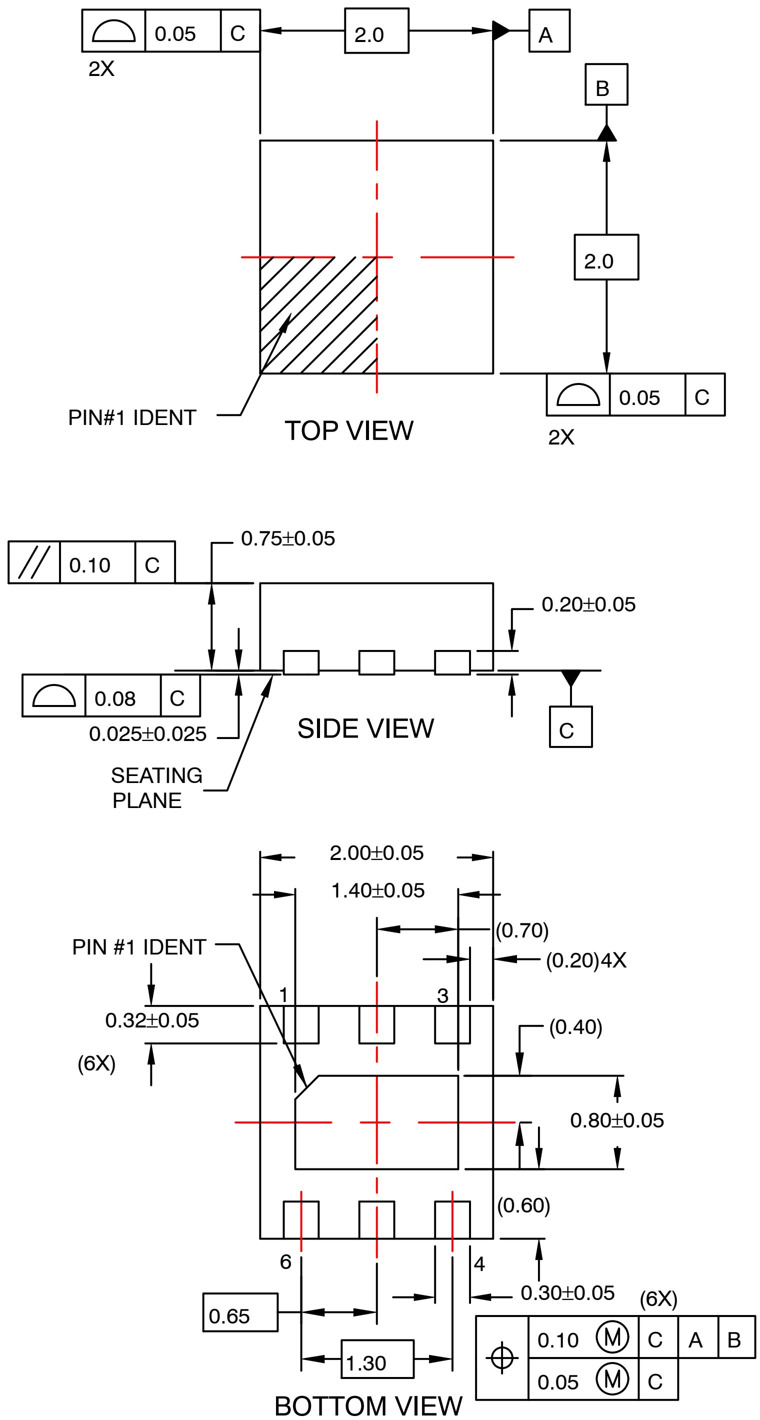


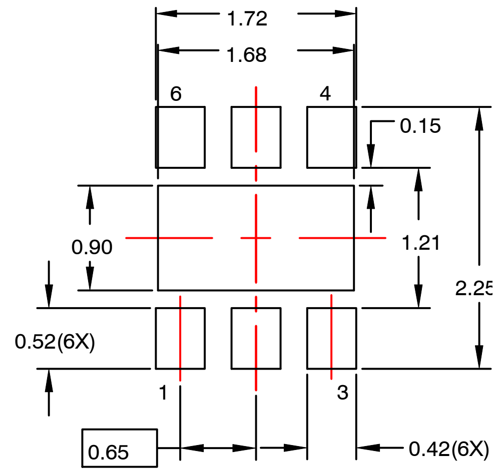
Figure 25. Demo Board Bottom Layer View

IntelliMAX is a trademark of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries.

WDFN6 2x2, 0.65P
CASE 511CY
ISSUE O

DATE 31 JUL 2016





RECOMMENDED
LAND PATTERN

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO−229 REGISTRATION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

DOCUMENT NUMBER:	**98AON13613G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN6 2X2, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales

◊