MJB44H11 (NPN), NJVMJB44H11 (NPN), MJB45H11 (PNP), NJVMJB45H11 (PNP)

Complementary Power Transistors

D²PAK for Surface Mount

Complementary power transistors are for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

Features

- Low Collector−Emitter Saturation Voltage − $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs
- Epoxy Meets UL 94 V−0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
  Machine Model, C > 400 V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Packages are Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	80	Vdc
Emitter−Base Voltage	V_{EB}	5	Vdc
Collector Current − Continuous − Peak	I_C	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 50 0.4	 W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	75	°C/W

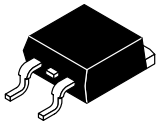
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ON Semiconductor®

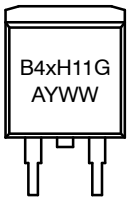
http://onsemi.com

SILICON POWER TRANSISTORS 10 AMPERES, 80 VOLTS, 50 WATTS

MARKING DIAGRAM



D²PAK CASE 418B STYLE 1



x = 4 or 5
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MJB44H11G	D²PAK (Pb−Free)	50 Units/Rail
MJB44H11T4G	D²PAK (Pb−Free)	800/Tape & Reel
NJVMJB44H11T4G	D²PAK (Pb−Free)	800/Tape & Reel
MJB45H11G	D²PAK (Pb−Free)	50 Units/Rail
MJB45H11T4G	D²PAK (Pb−Free)	800/Tape & Reel
NJVMJB45H11T4G	D²PAK (Pb−Free)	800/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)	$V_{CEO(sus)}$	80	–	–	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)	I_{CES}	–	–	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)	I_{EBO}	–	–	50	μA
ON CHARACTERISTICS					
Collector−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	–	1.0	Vdc
Base−Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)	h_{FE}	60	–	–	–
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)		40	–	–	
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz) MJB44H11, NJVMJB44H11 MJB45H11, NJVMJB45H11	C_{cb}	 – –	 130 230	 – –	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz) MJB44H11, NJVMJB44H11 MJB45H11, NJVMJB45H11	f_T	 – –	 50 40	 – –	MHz
SWITCHING TIMES					
Delay and Rise Times(I_C = 5 Adc, I_{B1} = 0.5 Adc) MJB44H11, NJVMJB44H11 MJB45H11, NJVMJB45H11	$t_d + t_r$	 – –	 300 135	 – –	ns
Storage Time(I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc) MJB44H11, NJVMJB44H11 MJB45H11, NJVMJB45H11	t_s	 – –	 500 500	 – –	ns
Fall Time(I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc) MJB44H11, NJVMJB44H11 MJB45H11, NJVMJB45H11	t_f	 – –	 140 100	 – –	ns

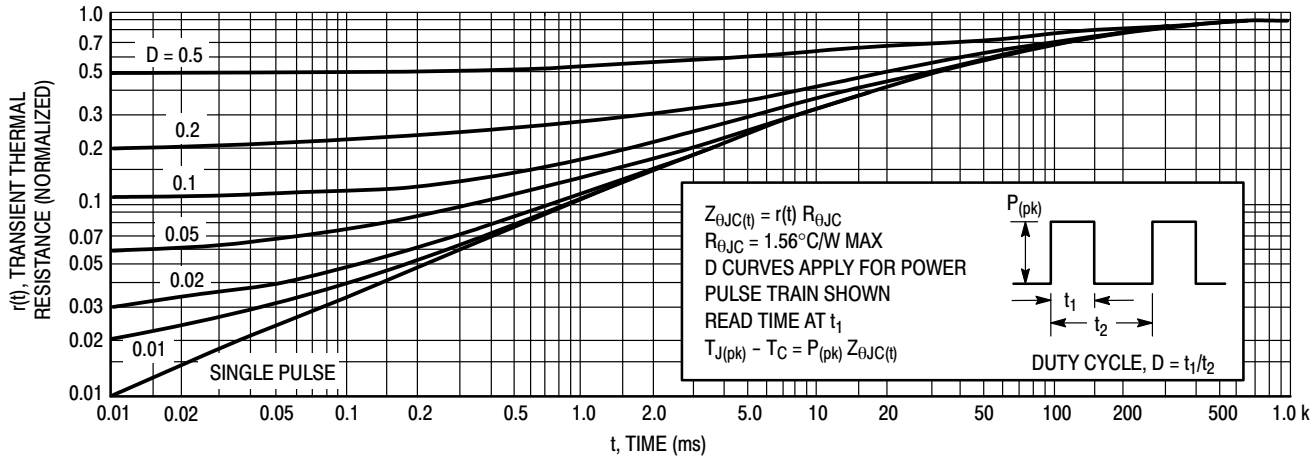


Figure 1. Thermal Response

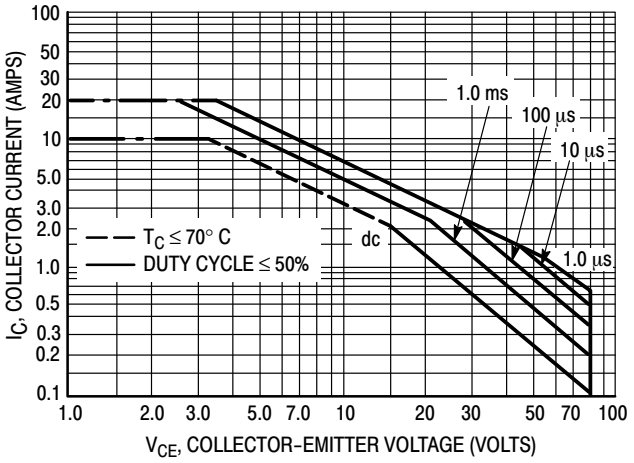


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

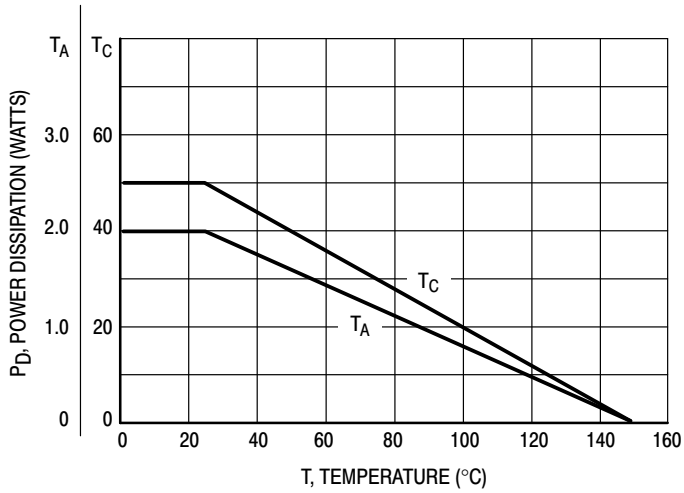


Figure 3. Power Derating

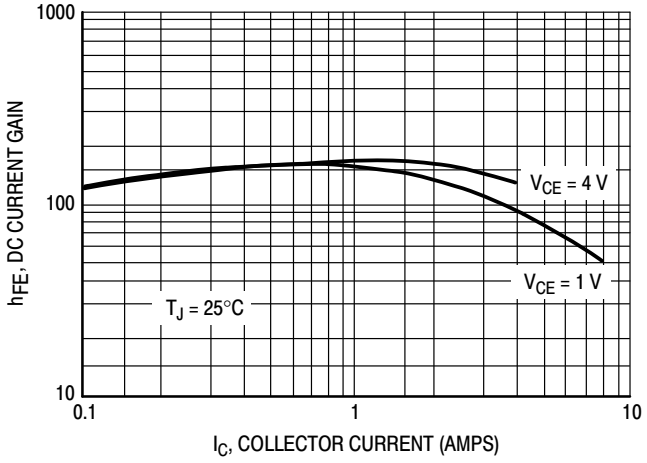


Figure 4. MJB44H11 DC Current Gain

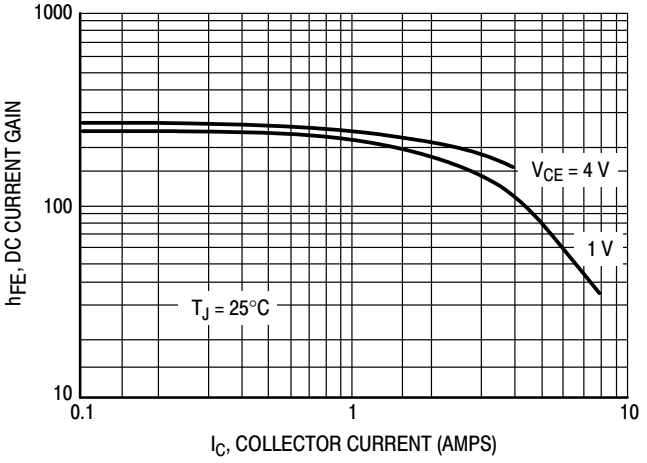


Figure 5. MJB45H11 DC Current Gain

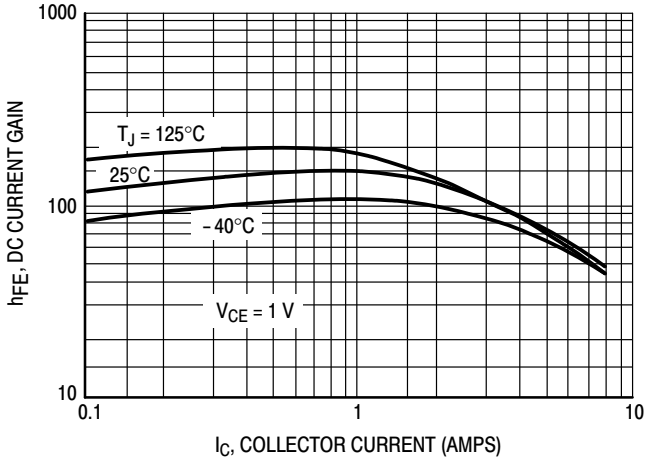


Figure 6. MJB44H11 Current Gain versus Temperature

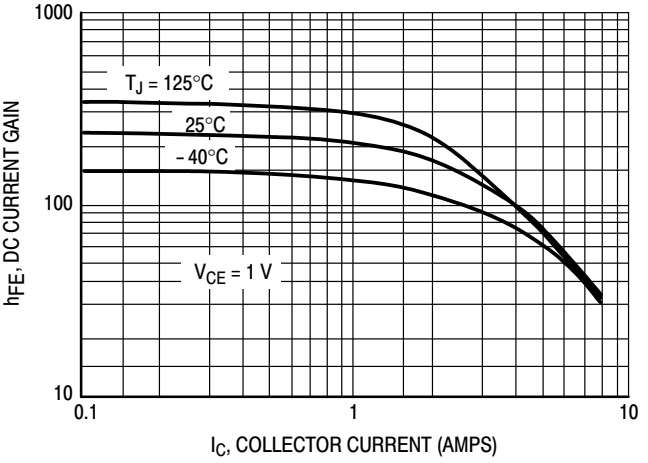


Figure 7. MJB45H11 Current Gain versus Temperature

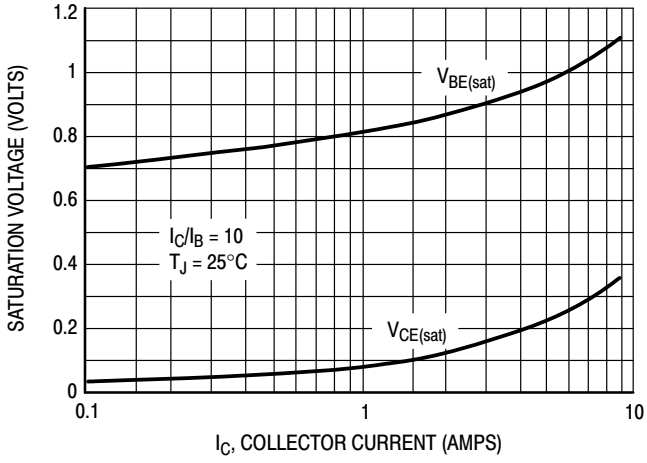


Figure 8. MJB44H11 On−Voltages

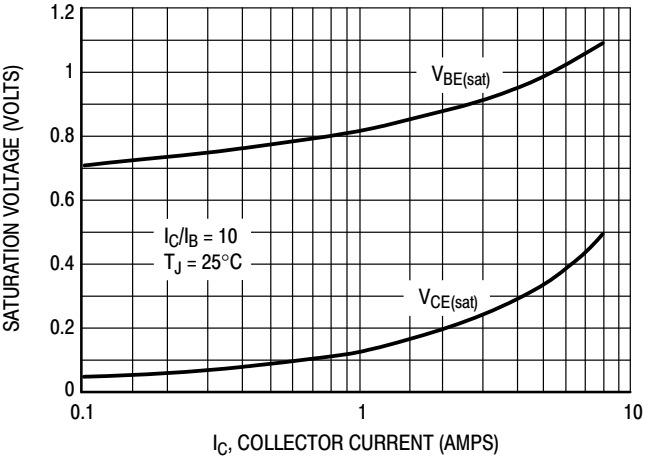
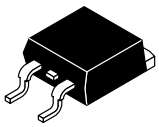


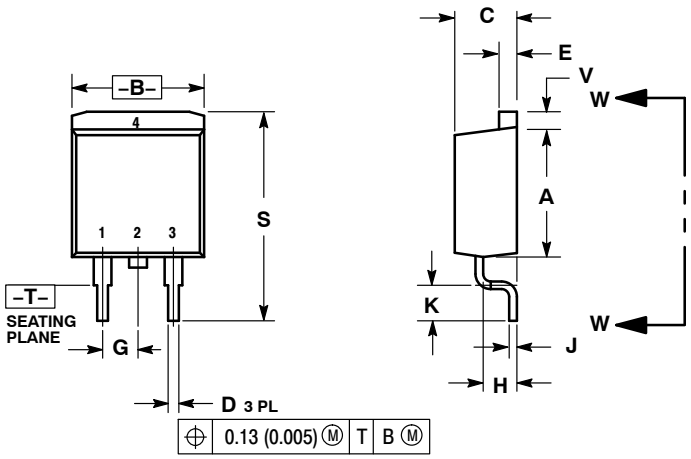
Figure 9. MJB45H11 On−Voltages



SCALE 1:1

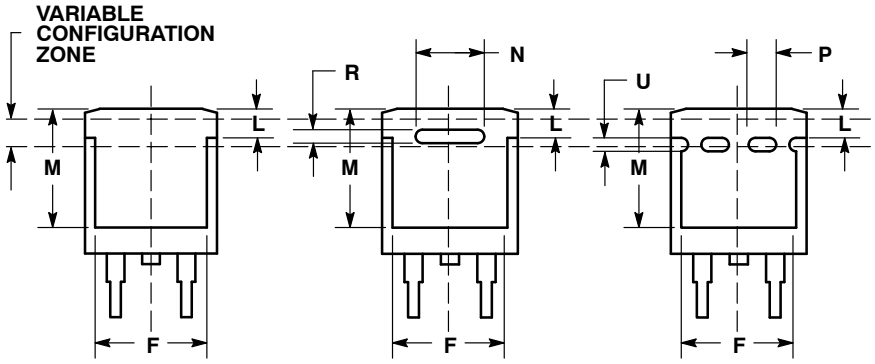
D²PAK 3
CASE 418B–04
ISSUE L

DATE 17 FEB 2015



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

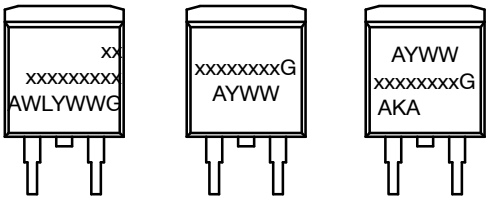
STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

GENERIC MARKING DIAGRAM*

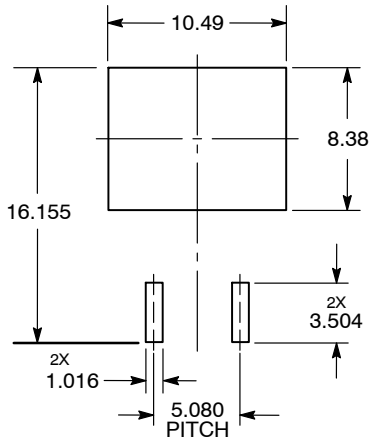


IC **Standard** **Rectifier**

xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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