

# NB100LVEP221

## 2.5V/3.3V 2:1:20 Differential HSTL/ECL/PECL Clock Driver

### Description

The NB100LVEP221 is a low skew 2:1:20 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The two clock inputs are differential ECL/PECL; CLK1/CLK1 can also receive HSTL signal levels. The LVPECL input signals can be either differential configuration or single-ended (if the V<sub>BB</sub> output is used).

The LVEP221 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure tightest skew, both sides of differential outputs should be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The NB100LVEP221, as with most other ECL devices, can be operated from a positive V<sub>CC</sub> supply in LVPECL mode. This allows the LVEP221 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on PECL terminations, designers should refer to Application Note AND8020/D.

The V<sub>BB</sub> pin, an internally generated voltage supply, is available to this device only. For single-ended LVPECL input conditions, the unused differential input is connected to V<sub>BB</sub> as a switching reference voltage. V<sub>BB</sub> may also rebias AC coupled inputs. When used, decouple V<sub>BB</sub> and V<sub>CC</sub> via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V<sub>BB</sub> should be left open.

Single-ended CLK input operation is limited to a V<sub>CC</sub> ≥ 3.0 V in LVPECL mode, or V<sub>EE</sub> ≤ -3.0 V in NECL mode.

### Features

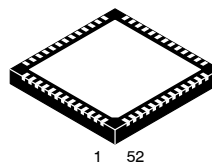
- 15 ps Typical Output-to-Output Skew
- 40 ps Typical Device-to-Device Skew
- Jitter Less than 2 ps RMS
- Maximum Frequency > 1.0 GHz Typical
- Thermally Enhanced 52-Lead QFN Package
- V<sub>BB</sub> Output
- 540 ps Typical Propagation Delay
- LVPECL and HSTL Mode Operating Range:  
V<sub>CC</sub> = 2.375 V to 3.8 V with V<sub>EE</sub> = 0 V
- NECL Mode Operating Range:  
V<sub>CC</sub> = 0 V with V<sub>EE</sub> = -2.375 V to -3.8 V
- Q Output will Default Low with Inputs Open or at V<sub>EE</sub>
- Pin Compatible with Motorola MC100EP221
- These Devices are Pb-Free and are RoHS Compliant



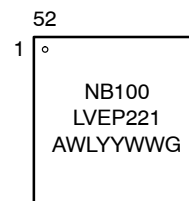
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### MARKING DIAGRAM\*



QFN52  
MN SUFFIX  
CASE 485M



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*For additional marking information, refer to Application Note AND8020/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# NB100LVEP221

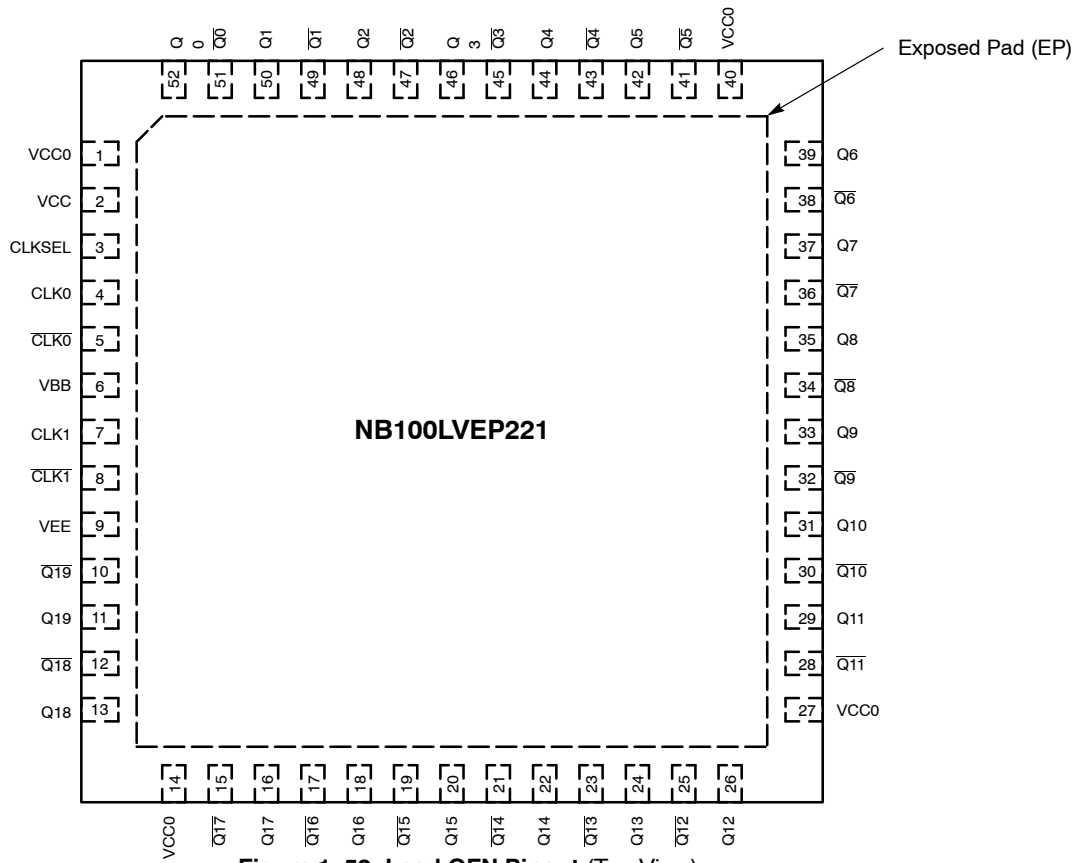


Figure 1. 52-Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK0*, $\overline{\text{CLK0}}$ **	ECL/PECL Differential Inputs
CLK1*, $\overline{\text{CLK1}}$ **	ECL/PECL or HSTL Differential Inputs
Q0:19, $\overline{\text{Q0}}$ : $\overline{\text{Q19}}$	ECL/PECL Differential Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub> /V <sub>CC0</sub>	Positive Supply
V <sub>EE</sub> ***	Negative Supply

\* Pins will default LOW when left open.

\*\* Pins will default HIGH when left open.

\*\*\* The thermally conductive exposed pad on the bottom of the package is electrically connected to V<sub>EE</sub> internally.

Table 2. FUNCTION TABLE

CLK_SEL	Active Input
L	CLK0, $\overline{\text{CLK0}}$
H	CLK1, $\overline{\text{CLK1}}$

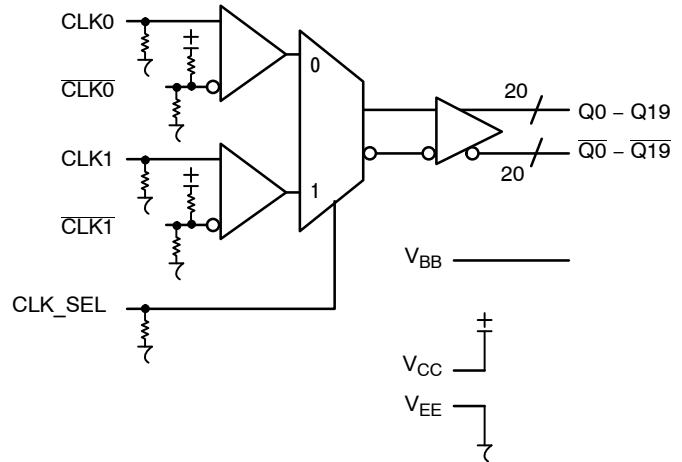


Figure 2. Logic Diagram

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**Table 3. ATTRIBUTES**

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model	> 2 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb-Free Pkg
QFN52		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		533 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, refer to Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
	NECL Mode Input Voltage	V <sub>CC</sub> = 0 V	V <sub>I</sub> ≥ V <sub>EE</sub>	-6	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) (Note )	0 lfpm	QFN52	25	°C/W
		500 lfpm	QFN52	19.6	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case) (Note )	2S2P	QFN52	21	°C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free		265	°C
				265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 5. LVPECL DC CHARACTERISTICS**  $V_{CC} = 2.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{OL}$	Output LOW Voltage (Note 3)	555	680	900	555	680	900	555	680	900	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
$V_{IL}$	Input LOW Voltage (Single-Ended) (Note 4)	555		900	555		900	555		900	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) CLK0/CLK0 CLK1/CLK1	1.2 0.3		2.5 1.6	1.2 0.3		2.5 1.6	1.2 0.3		2.5 1.6	V V
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary + 0.125 V to -1.3 V.
3. All outputs loaded with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .
4. Do not use  $V_{BB}$  at  $V_{CC} < 3.0\text{ V}$ .
5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 6. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 7)	1355	1480	1700	1355	1480	1700	1355	1480	1700	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
$V_{BB}$	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) CLK0/CLK0 CLK1/CLK1	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	1.2 0.3		3.3 1.6	V V
$I_{IH}$	Input HIGH Current			150			150			150	μA
$I_{IL}$	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary + 0.925 V to -0.5 V.
7. All outputs loaded with 50 Ω to  $V_{CC} - 2.0\text{ V}$ .
8. Single-ended input operation is limited  $V_{CC} \geq 3.0\text{ V}$  in LVPECL mode.
9.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 7. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.375\text{ V to } -3.8\text{ V}$  (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	100	125	150	104	130	156	116	145	174	mA
$V_{OH}$	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 11)	-1945	-1820	-1600	-1945	-1820	-1600	-1945	-1820	-1600	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
$V_{BB}$	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)  CLK0/ $\overline{\text{CLK0}}$ CLK1/ $\overline{\text{CLK1}}$	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	$V_{EE} + 1.2$ $V_{EE} + 0.3$		0.0 -0.9	V V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Input and output parameters vary 1:1 with  $V_{CC}$ .

11. All outputs loaded with  $50\ \Omega$  to  $V_{CC}-2.0\text{ V}$ .

12. Single-ended input operation is limited  $V_{EE} \leq -3.0\text{V}$  in NECL mode.

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. HSTL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage CLK1/ $\overline{\text{CLK1}}$	$V_x+100$		1600	$V_x+100$		1600	$V_x+100$		1600	mV
$V_{IL}$	Input LOW Voltage CLK1/ $\overline{\text{CLK1}}$	-300		$V_x-100$	-300		$V_x-100$	-300		$V_x-100$	mV
$V_X$	Differential Configuration Cross Point Voltage	680		900	680		900	680		900	mV
$I_{IH}$	Input HIGH Current	-150		150	-150		150	-150		150	$\mu\text{A}$
$I_{IL}$	Input LOW Current CLK1 CLK1	-150 -250			-150 -250			-150 -250			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

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**Table 9. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -2.375\text{ to }-3.8\text{ V}$  or  $V_{CC} = 2.375\text{ to }3.8\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$V_{Opp}$	Differential Output Voltage (Figure 3)	$f_{out} < 50\text{ MHz}$	550	700		600	700		600	700		mV
		$f_{out} < 0.8\text{ GHz}$	550	700		550	700		500	700		mV
		$f_{out} < 1.0\text{ GHz}$	500	700		500	700		400	600		mV
$t_{PLH}/t_{PHL}$	Propagation Delay (Differential Configuration) CLK0-Qx CLK1-Qx		540	600		540	660		540	750		ps
			590	640		590	710		590	800		ps
$t_{skew}$	Within-Device Skew (Note 15)		15	50		15	50		15	50		ps
	Device-to-Device Skew (Note 16)		40	200		40	200		40	200		ps
$t_{JITTER}$	Random Clock Jitter (RMS) (Figure 3)		1	2		1	2		1	2		ps
$V_{PP}$	Input Swing (Differential Configuration) (Note 17) (Figure 4)	CLK0	400	800	1200	400	800	1200	400	800	1200	mV
		CLK1 HSTL	300	800	1000	300	800	1000	300	800	1000	mV
DCO	Output Duty Cycle	49.5	50	50.5	49.5	50	50.5	49.5	50	50.5		%
$t_r/t_f$	Output Rise/Fall Time (20%–80%)	100	200	300	100	200	300	150	250	350		ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

14. Measured with 750 mV source (LVPECL) or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50  $\Omega$  to  $V_{CC}-2\text{ V}$ .

15. Skew is measured between outputs under identical transitions and conditions on any one device.

16. Device-to-Device skew for identical transitions, outputs and  $V_{CC}$  levels.

17.  $V_{PP}$  is the differential configuration input voltage swing required to maintain AC characteristics.

# NB100LVEP221

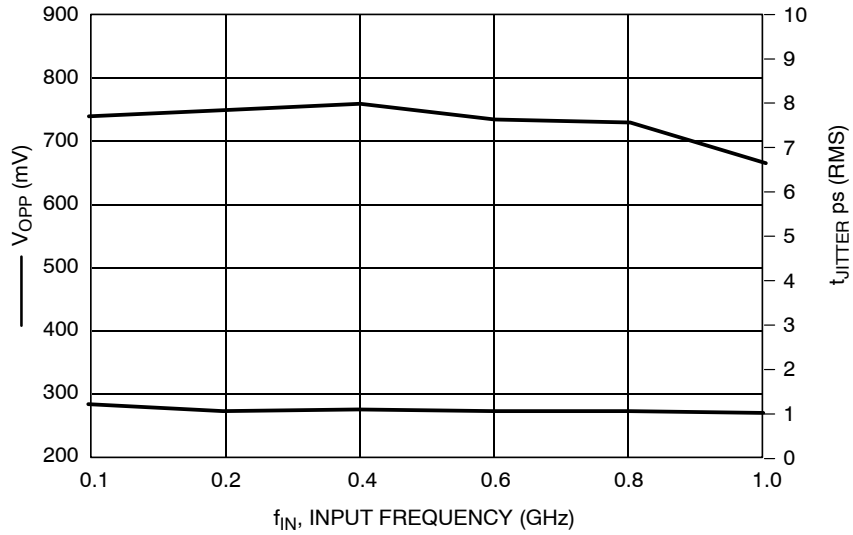


Figure 3. Output Voltage ( $V_{OPP}$ )/Jitter versus Input Frequency ( $V_{CC} - V_{EE} = 3.3 \text{ V} @ 25^\circ\text{C}$ )

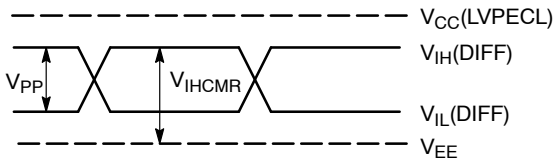


Figure 4. LVPECL Differential Input Levels

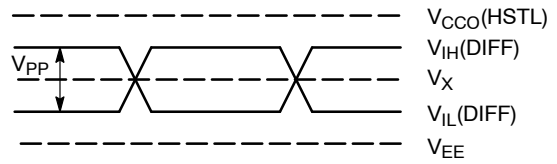


Figure 5. HSTL Differential Input Levels

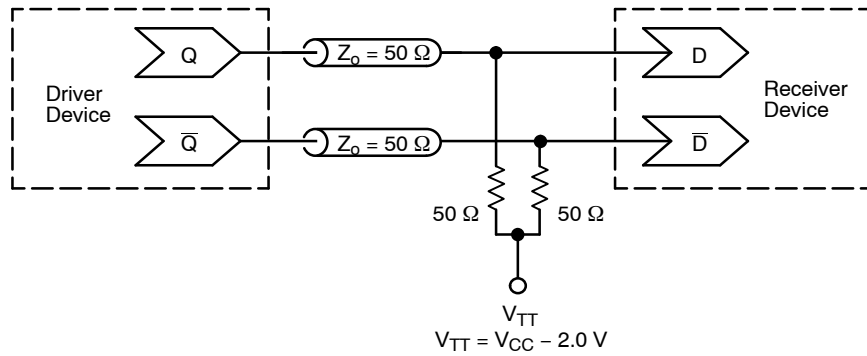


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

# NB100LVEP221

## ORDERING INFORMATION

Device	Package	Shipping†
NB100LVEP221MNRG	QFN52 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices



# MECHANICAL CASE OUTLINE

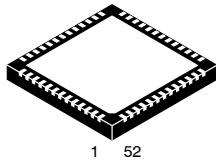
## PACKAGE DIMENSIONS

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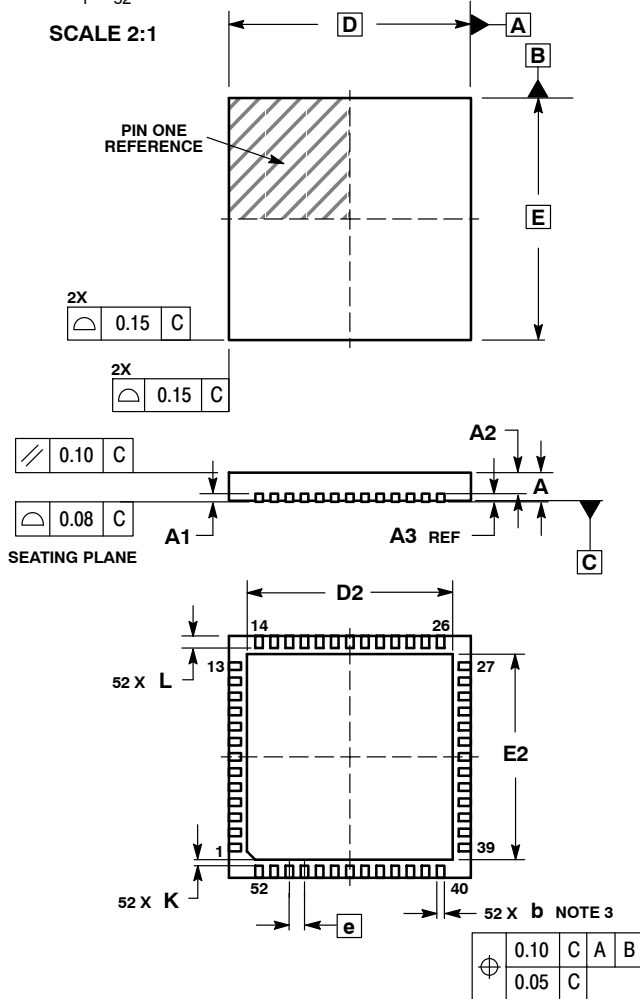


**QFN52 8x8, 0.5P**  
CASE 485M-01  
ISSUE C

DATE 16 FEB 2010



SCALE 2:1

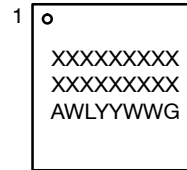


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

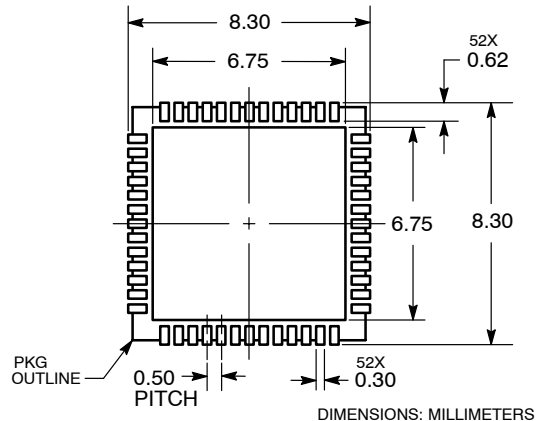
MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

GENERIC MARKING DIAGRAM



- XXXXXXXXXX = Device Code
- A = Assembly Site
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

RECOMMENDED SOLDERING FOOTPRINT



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<b>DESCRIPTION:</b>	<b>52 PIN QFN, 8X8, 0.5P</b>	<b>PAGE 1 OF 1</b>

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