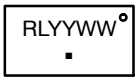
Low Phase-Noise Two-Channel Clock Fanout Buffer

NB3RL02

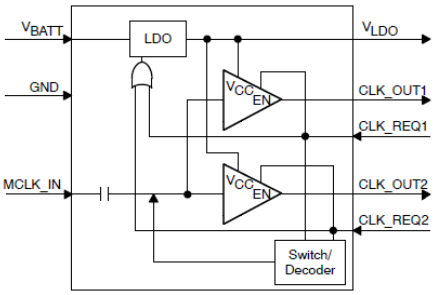
WLCSP8
CASE 499BQ

MARKING DIAGRAM



RL = Specific Device Code
YY = Year
WW = Work Week
▪ = Pb−Free Package

LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

The NB3RL02 is a low−skew, low jitter 1:2 clock fan−out buffer, ideal for use in portable end−equipment, such as mobile phones. With integrated LDO and output control circuitry.

The MCLK_IN pin has an AC coupling capacitor and will directly accept a square or sine wave clock input, such as a temperature compensated crystal oscillator (TCXO). The minimum acceptable input amplitude of the sine wave is 300 mV peak−to−peak.

The two clock outputs are enabled by control inputs CLK_REQ1 and CLK_REQ2.

The NB3RL02 has an integrated Low−Drop−Out (LDO) voltage regulator which accepts input voltages from 2.3 V to 5.5 V and outputs 1.8 V at I_{out} = 50 mA. This 1.8 V supply is externally available to provide regulated power to peripheral devices, such as a TCXO.

The adaptive clock output buffers offer controlled slew−rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

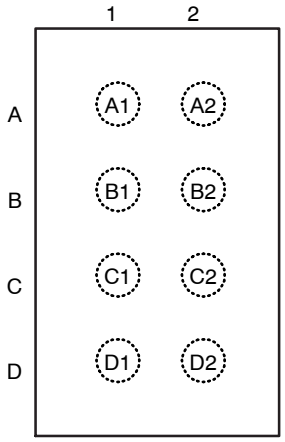
The NB3RL02 is offered in a 0.4 mm pitch wafer−level−chip−scale (WLCS) package and is optimized for very low standby current consumption.

Features

- Low Additive Noise:
  - −149 dBc/Hz at 10 kHz Offset Phase Noise
  - 0.37 ps (rms) Output Jitter
- Limited Output Slew Rate for EMI Reduction (1 ns to 5 ns/Rise/Fall Time for 10−50 pF Loads)
- Regulated 1.8 V Output Supply Available for External Clock Source, ie. TCX0
- Operation to 80 MHz
- Ultra−Small Package:
  - 8−ball: 0.4 mm Pitch WLCS
- ESD Performance Exceeds JESD 22
  - 2000 V Human−Body Model (A114−A)
  - 200 V Machine Model (A115−A)
  - 1000 V Charged−Device Model (JESD22−C101−A Level III)
- These are Pb−Free Devices

Applications

- Cellular Phones
- Global Positioning Systems (GPS)



(Package – Flip Chip)
Die Pads Face Down on PCB

Figure 1. Pinout (Top View)

Table 1. PIN DESCRIPTION

Ball No.	Name	I/O	Description
A1	VBATT	I	Input to internal LDO
A2	CLK_OUT1	O	Clock output 1
B1	VLDO	O	1.8 V supply for NB3RL02 and external TCXO
B2	CLK_REQ1	I	Clock request from peripheral 1
C1	MCLK_IN	I	Master clock input
C2	CLK_REQ2	I	Clock request from peripheral 2
D1	GND	–	Ground
D2	CLK_OUT2	O	Clock output 2

Table 2. FUNCTION TABLE

Inputs			Outputs		
CLK_REQ1	**CLK_REQ2**	**MCLK_IN**	**CLK_OUT1**	**CLK_OUT2**	**VLDO**
L	L	X	L	L	0 V
L	H	CLK	L	CLK	1.8 V
H	L	CLK	CLK	L	1.8 V
H	H	CLK	CLK	CLK	1.8 V

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Min	Max	Unit
V_{BATT}	V_{BATT} Voltage Range (Note 1)		−0.3	7	V
	Voltage range (Note 2)	CLK_REQ_1/2, MCLK_IN	−0.3	V_{BATT} + 0.3	V
		V_{LDO}, CLK_OUT_1/2 (Note 1)	−0.3	V_{BATT} + 0.3	
I_{IK}	Input clamp current at V_{BATT}, CLK_REQ_1/2, and MCLK_IN	V_I < 0		−50	mA
I_O	Continuous output current	CLK_OUT1/2		±20	mA
	Continuous current through GND, V_{BATT}, V_{LDO}	Continuous current through GND, V_{BATT}, V_{LDO}		±50	mA
	ESD Rating	Human−Body Model		2000	V
		Charged−Device Model		1000	
		Machine Model		200	
T_J	Operating virtual junction temperature		−40	150	°C
T_A	Operating ambient temperature range		−40	85	°C
T_{stg}	Storage temperature range		−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input negative−voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. All voltage values are with respect to network ground terminal.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 3)

Symbol	Parameter		Min	Max	Unit
V_{BATT}	Input voltage	V_{BATT}	2.3	5.5	V
V_I	Input voltage Amplitude	MCLK_IN, CLK_REQ1/2	0	1.89	V
V_O	Output voltage	CLK_OUT1/2	0	1.8	V
V_{IH}	High−level input voltage	CLK_REQ1/2	1.3	1.89	V
V_{IL}	Low−level input voltage	CLK_REQ1/2	0	0.5	V
I_{OH}	High−level output current, DC current		−8		mA
I_{OL}	Low−level output current, DC current			8	mA

3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Table 5. ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
LDO							
V_{OUT}	LDO output voltage	I_{OUT} = 50 mA		1.71	1.8	1.89	V
C_{LDO}	External load capacitance			1		10	μF
$I_{OUT(SC)}$	Short circuit output current	R_L = 0 Ω			100		mA
$I_{OUT(PK)}$	Peak output current	V_{BATT} = 2.3 V, V_{LDO} = V_{OUT} − 5%			55	100	mA
PSR	Power supply rejection	V_{BATT} = 2.3V, I_{OUT} = 2 mA	f_{IN} = 217 Hz and 1 kHz	60			dB
			f_{IN} = 3.25 MHz	40			
t_{su}	LDO start−up time	V_{BATT} = 2.3 V , C_{LDO} = 1 μF, CLK_REQ_n to V_{LDO} = 1.71 V			0.2		ms
		V_{BATT} = 5.5 V , C_{LDO} = 10 μF, CLK_REQ_n to V_{LDO} = 1.71 V				1	ms
POWER CONSUMPTION							
I_{SB}	Standby current	Device in standby (all VCLK_REQ_n = 0 V)			0.2	1	μA
I_{CCS}	Static current consumption	Device active but not switching, V_{CLK_REQn} = H			0.4	1	mA
I_{OB}	Output buffer average current	f_{IN} = 26 MHz, C_{LOAD} = 50 pF f_{IN} = 52 MHz, C_{LOAD} = 50 pF			4.2 6.0		mA
C_{PD}	Output power dissipation capacitance	f_{IN} = 26 MHz				44	pF
MCLK_IN INPUT							
I_I	MCLK_IN, CLK_REQ_1/2 leakage current	V_I = V_{LDO} or GND				1	μA
C_I	MCLK_IN capacitance	f_{IN} = 26 MHz			3.75		pF
R_I	MCLK_IN impedance	f_{IN} = 26 MHz			5		kΩ
f_{IN}	MCLK_IN frequency range			9	26/52	80	MHz
MCLK_IN LVCMOS SOURCE							
	Phase noise	f_{IN} = 26 MHz/52 MHz, tr/tf ≤ 1 ns	1 kHz offset		−140/−133		dBc/Hz
			10 kHz offset		−149/−144		
			100 kHz offset		−153/−146		
			1 MHz offset		−151/−151		
	Additive jitter	f_{IN} = 26 MHz, V_{PP} = 0.8 V, f_{IN} = 52 MHz, V_{PP} = 0.8 V, BW = 10 kHz – 5 MHz			0.37 0.24		ps (rms)
t_{DL}	MCLK_IN to CLK_OUT_n propagation delay				10		ns
DC_L	Output duty cycle	f_{IN} = 26 MHz, DC_{IN} = 50% f_{IN} = 52 MHz, DC_{IN} = 50%		45 45	50 50	55 55	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 5. ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
MCLK_IN SINUSOIDAL SOURCE							
V_{MA}	Input amplitude			0.3		1.8	V
	Phase noise	f_{IN} = 26 Mhz/52 MHz, V_{MA} = 1.8 V_{PP}	1 kHz offset		−138/−137		dBc/Hz
			10 kHz offset		−146/−147		
			100 kHz offset		−151/−149		
			1 MHz offset		−149/−154		
		f_{IN} = 26 Mhz/52 MHz, V_{MA} = 0.8 V_{PP}	1 kHz offset		−138/−135		
			10 kHz offset		−146/−144		
			100 kHz offset		−150/−145		
			1 MHz offset		−148/−149		
	Additive jitter	f_{IN} = 26 MHz, V_{MA} = 1.8 V_{PP}, f_{IN} = 52 MHz, V_{MA} = 1.8 V_{PP}, BW = 10 kHz – 5 MHz			0.37 0.16		ps (rms)
t_{DS}	MCLK_IN to CLK_OUT_1/2 propagation delay				12		ns
DC	Output duty cycle	f_{IN} = 26 MHz, V_{MA} > 1.8 V_{PP} f_{IN} = 52 MHz, V_{MA} > 1.8 V_{PP}		45 45	50 50	55 55	%
CLK_OUT_N OUTPUTS							
t_r	20% to 80% rise time	C_L = 10 pF to 50 pF		1		5	ns
t_f	20% to 80% fall time	C_L = 10 pF to 50 pF		1		5	ns
t_{sk}	Channel−to−channel skew	C_L = 10 pF to 50 pF, (C_{L1} = C_{L2}) up to 52 MHz		−0.5		0.5	ns
V_{OH}	High−level output voltage	I_{OH} = −100 μA, reference to V_{LDO}		−0.1			V
		I_{OH} = −8 mA		1.2			
V_{OL}	Low−level output voltage	I_{OL} = 20 μA				0.2	V
		I_{OL} = 8 mA				0.55	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

APPLICATION INFORMATION

Typical Application

A typical mobile application for the NB3RL02 is shown in Figure 2. An external low noise TCXO clock source is powered by the NB3RL02's 1.8 V regulated LDO and is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral can independently request an active clock by asserting a clock request line (CLK_REQ1 or CLK_REQ2).

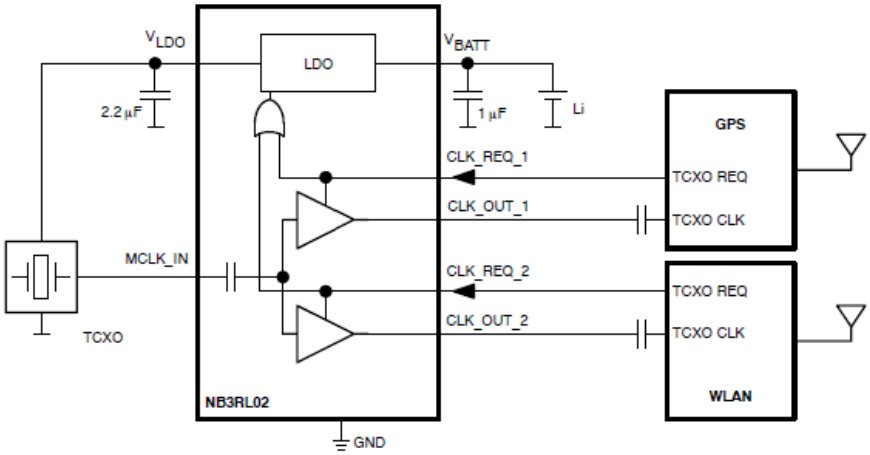


Figure 2. Mobile Application

When both clock request lines are logic LOW, the NB3RL02 enters a current-saving shutdown mode. In this mode, the LDO output goes to 0 V and turns off the TCXO. Also, the unpowered CLK_OUT1 and CLK_OUT2 outputs are pulled to GND.

When the NB3RL02 receives a HIGH from either peripheral CLK_REQn, the 1.8 V LDO output is enabled and will power the TCXO. The output of the TCXO can be a square wave, sine wave, or clipped sine wave and is converted to a buffered square wave.

Input Clock to Output Square Wave Generator

Figure 3 shows the MCLK_IN input having an internal AC coupling capacitor. This allows either a square or sine wave signal to be directly connected from a TCXO. Therefore, an external series capacitor is not required.

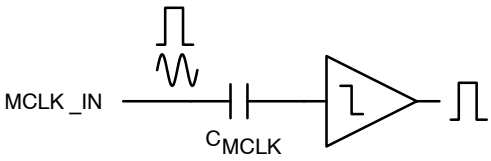


Figure 3. Input Stage

The clock frequency band of the NB3RL02 is 9 MHz to 80 MHz with all performance metrics specified at 26 Mhz and 52 MHz.

Typical input sinusoidal signal amplitude is 0.8 V_{PP} for specified performance, but amplitudes as low as 0.3 V_{PP} are acceptable, but with reduced phase noise and jitter performance.

CLK_OUT1 and CLK_OUT2 Outputs

The CLK_OUT1 and CLK_OUT2 outputs drive 1.8 V LVCMOS levels with rise/fall times within 1 ns to 5 ns with load capacitors between 10 pF and 50 pF. These relatively slow edge rates will minimize EMI radiation into the system. When not requested, each output is set to Low to avoid false clocking of the load device.

LDO

The integrated low noise 1.8 V LDO provides power internal to the NB3RL02 as well as a power source for an external clock such as a TCX0. The input range of the LDO allows the device to be powered directly from a single cell Li battery. The LDO is enabled when either of the CLK_REQn signals is High.

When disabled, the device turns off the LDO and enters a low power shutdown mode consuming less than 1 μA from the battery.

The LDO requires an output decoupling capacitor in the range of 1 μF to 10 μF for compensation and high frequency PSR. An input bypass capacitor of 1 μF or larger is recommended.

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping†
NB3RL02FCT2G	−40°C to 85°C	WLCSP8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

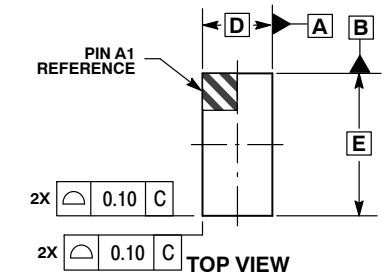
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

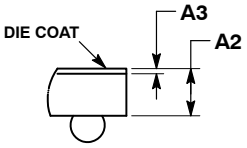
WLCSP8, 1.57x0.77
CASE 499BQ
ISSUE A

SCALE 4:1

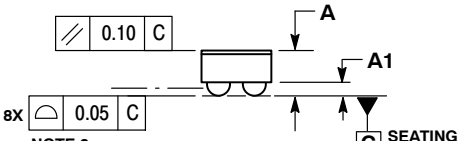
DATE 01 SEP 2015



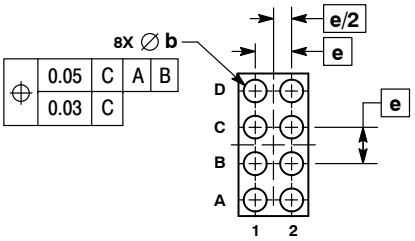
TOP VIEW



DETAIL A



SIDE VIEW

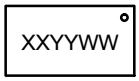


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.50
A1	0.13	0.17
A2	0.30 REF	
A3	0.025 BSC	
b	0.21	0.25
D	0.77 BSC	
E	1.57 BSC	
e	0.40 BSC	

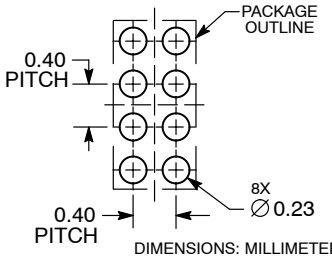
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP8, 1.57X0.77**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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