1.5 A Ultra-Small Controlled Load Switch with Auto-Discharge Path

NCP333

Description

The NCP333 are low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC's on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail.

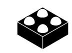
Proposed in a wide input voltage range from 1.2 V to 5.5 V, and a very small 0.76 x 0.76 mm WLCSP4, 0.4 pitch.

Features

- 1.2 V – 5.5 V Operating Range
- 55 mΩ P MOSFET at 3.3 V
- DC Current up to 1.5 A
- Output Auto−Discharge
- Active High EN Pin
- WLCSP4 0.76 x 0.76 mm
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

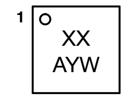
Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices



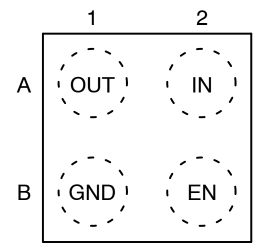
WLCSP4
CASE 567FJ

MARKING DIAGRAM



XX	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

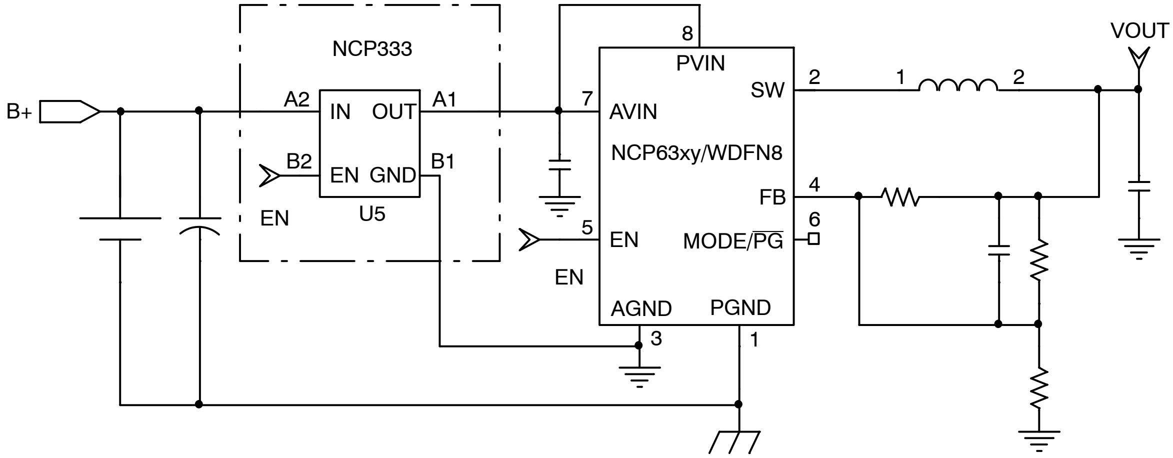


Figure 1. Typical Application Circuit

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2	POWER	Load−switch input voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	B1	POWER	Ground connection.
EN	B2	INPUT	Enable input, logic high turns on power switch.
OUT	A1	OUTPUT	Load−switch output; connect a 0.1 μF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

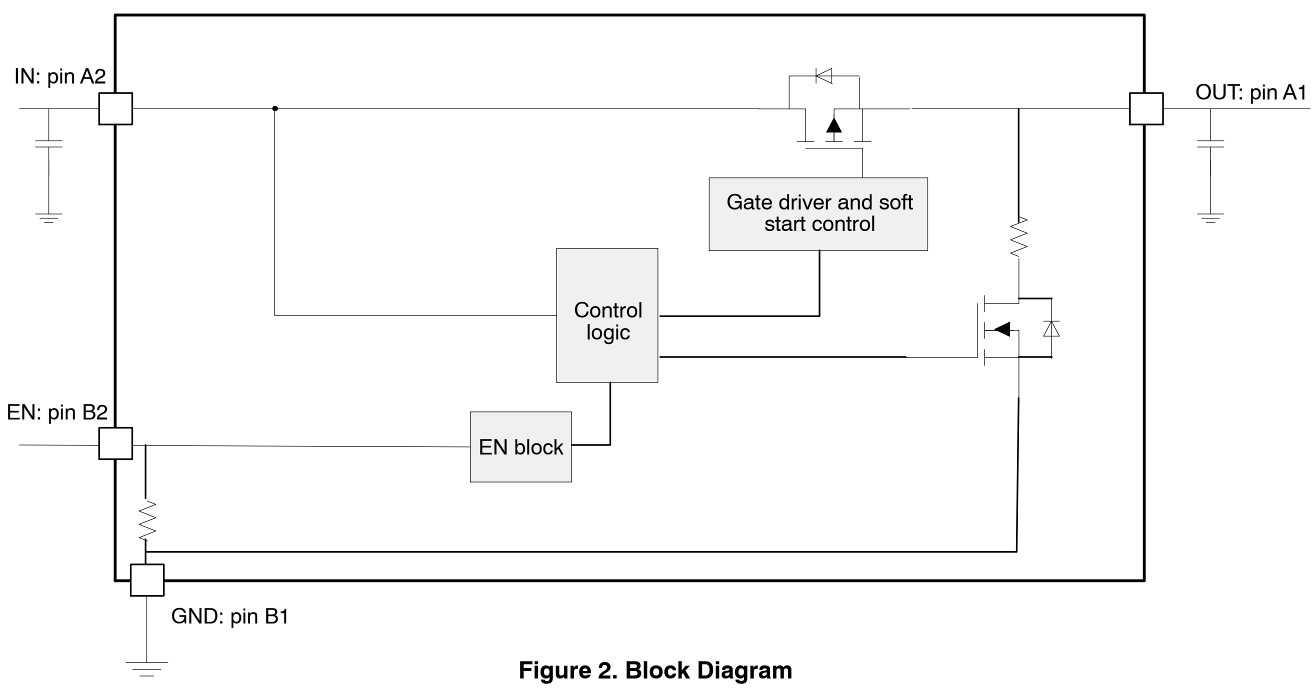


Figure 2. Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins	V_{EN}, V_{IN}, V_{OUT}	−0.3 to + 7.0	V
From IN to OUT Pins: Input/Output	V_{IN}, V_{OUT}	0 to + 7.0	V
Human Body Model (HBM) ESD Rating are (Notes 1, 2)	ESD HBM	4000	V
Machine Model (MM) ESD Rating are (Notes 1, 2)	ESD MM	200	V
Maximum Junction Temperature	T_J	−40 to +125	°C
Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.2		5.5	V
V_{EN}	Enable Voltage			0		5.5	V
T_A	Ambient Temperature Range			−40	25	+85	°C
C_{IN}	Decoupling input capacitor			0.1			μF
C_{OUT}	Decoupling output capacitor			0.1			μF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 5)			150		°C/W
I_{OUT}	Maximum DC current					1.5	A
I_{peak}	Maximum Peak current	1 ms				2	A
P_D	Power Dissipation Rating (Note 6)	$T_A \leq 25°C$	WLCSP package		0.4		W
		$T_A = 85°C$	WLCSP package		0.16		W

1. According to JEDEC standard JESD22−A108.
2. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115 for all pins.
3. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020.
5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

Table 4. ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.2 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{IN} = 3.3 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
R_{DSON}	Static drain-source on-state resistance, (Note 7)	Vin = 5.5 V, I_{OUT} = 200 mA	T_A = 25°C		45	55	mΩ
		Vin = 3.3 V, I_{OUT} = 200 mA	T_A = 25°C		55	74	
		Vin = 1.8 V, I_{OUT} = 200 mA	T_A = 25°C		90	125	
			T_A = 85°C			135	
		Vin = 1.2 V, I_{OUT} = 200 mA	T_A = 25°C		300	400	
Rdis	Output discharge path	Vin = 3.3 V	EN = low		70	110	Ω
T_R	Output rise time (Note 8)	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω		95		μs
T_F	Output fall time (Note 8)	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 5 Ω		11		μs
			C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω		40		
			C_{LOAD} = 1 μF, R_{LOAD} = 100 Ω		94		
T_{on}	Turn on (Note 8)	V_{IN} = 3.6 V	C_{LOAD} = 1 μF, R_{LOAD} = 25 Ω		195		μs
T_{en}	Enable time	V_{IN} = 3.6 V	From EN low to high to Vout = 10% of fully on		100		μs
V_{IH}	High-level input voltage			0.9			V
V_{IL}	Low-level input voltage					0.5	V
EN_{pd}	EN pull down resistor				5		MΩ
QUIESCENT CURRENT							
Iq	Current consumption	Vin = 4.2 V, EN = low, No load				1	μA
		Vin = 4.2 V, EN = high, No load				1	μA

7. Guaranteed by design and characterization
8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

TIMINGS

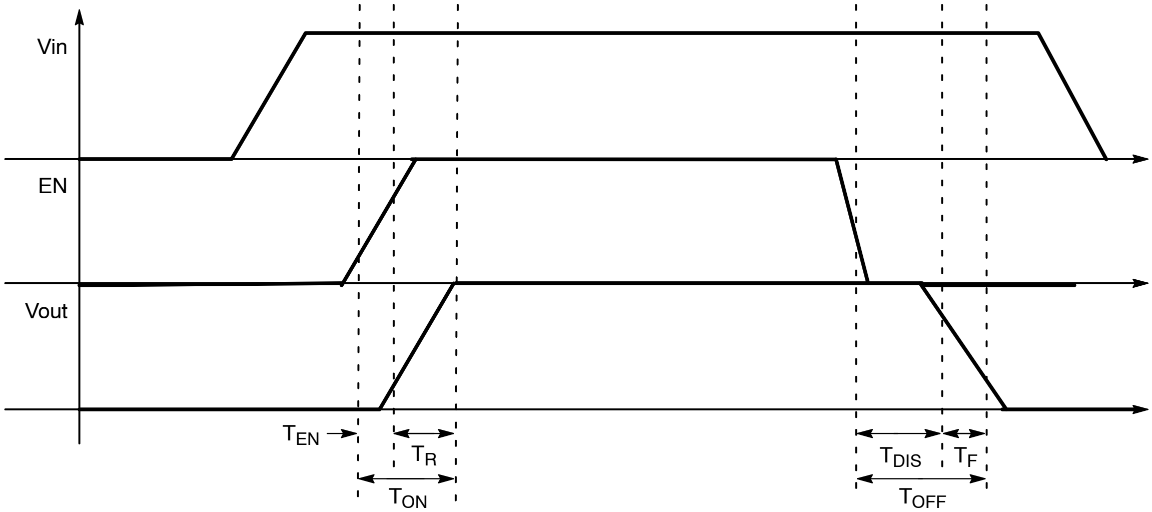


Figure 3. Enable, Rise and Fall Time

TYPICAL CHARACTERISTICS

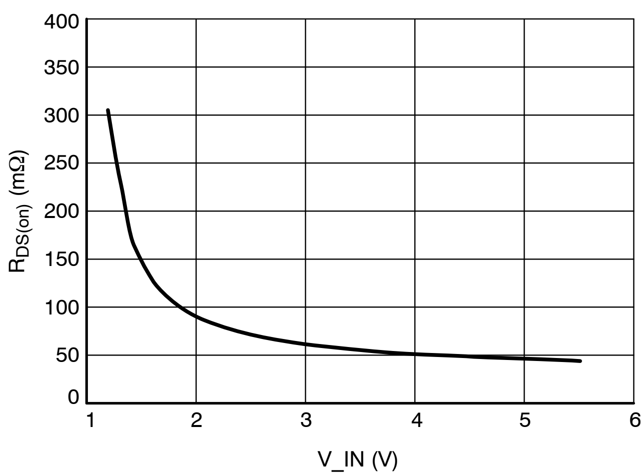


Figure 4. $R_{DS(on)}$ (mΩ) vs. V_{IN} (V)
(I_{LOAD} = 100 mA & Temp 25°C)

TYPICAL CHARACTERISTICS

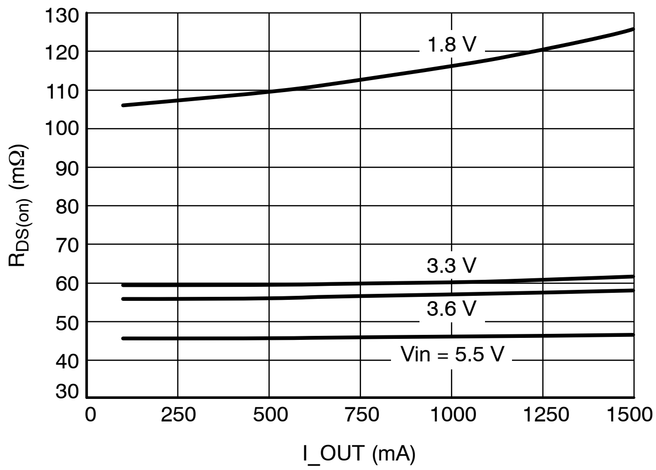


Figure 5. $R_{DS(on)}$ (mΩ) vs. I_{LOAD} (mA)

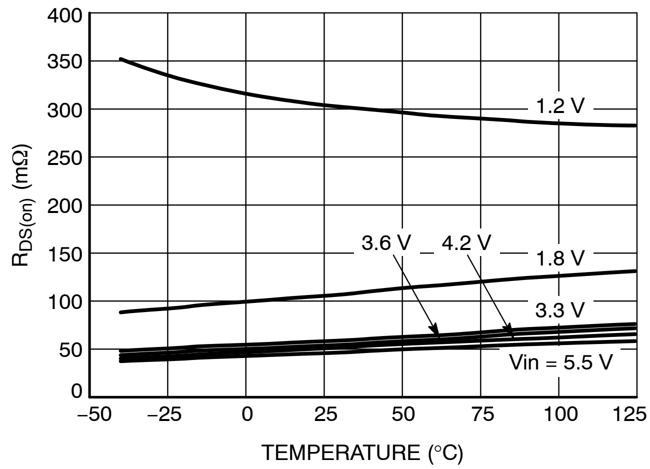


Figure 6. $R_{DS(on)}$ (mΩ) vs. Temperature (°C) at I_{LOAD} 100 mA

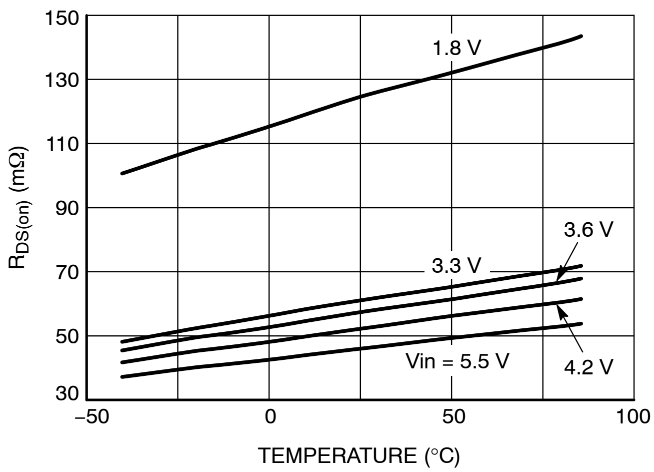


Figure 7. $R_{DS(on)}$ (mΩ) vs. Temperature (°C) at I_{LOAD} 1500 mA

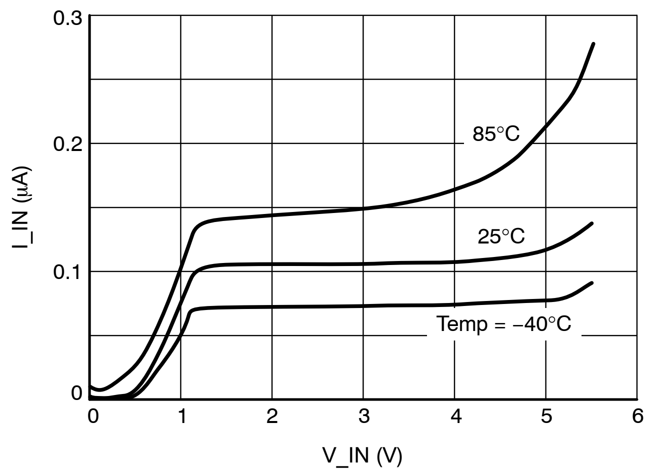


Figure 8. Standbycurrent vs. Temperature (°C) No Load

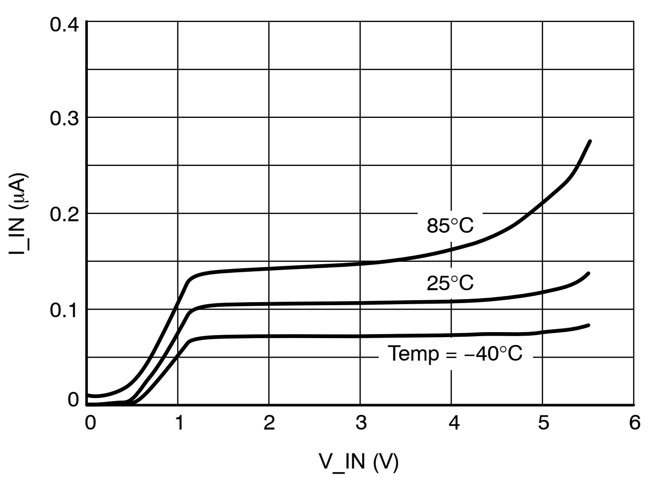


Figure 9. Standbycurrent vs. Temperature (°C) Output Shorted to GND

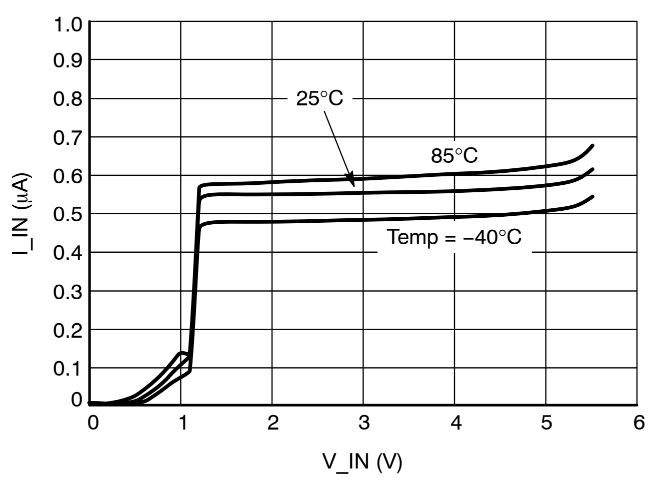


Figure 10. Quiescent Current vs. Temperature (°C)

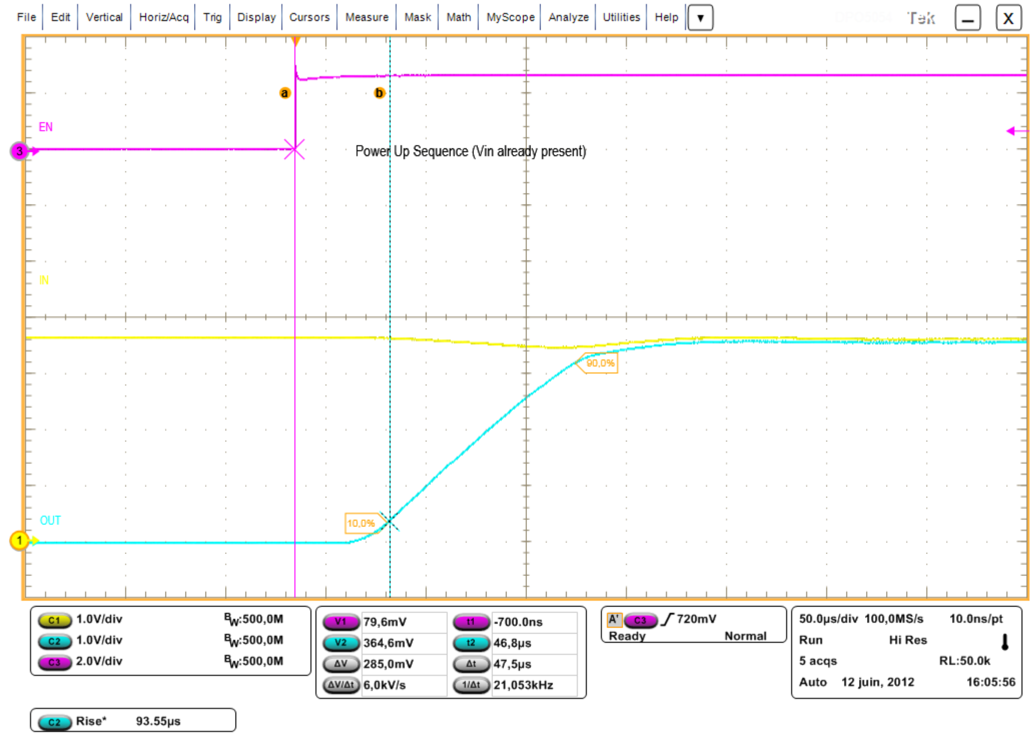


Figure 11. Enable Time and Rise Time

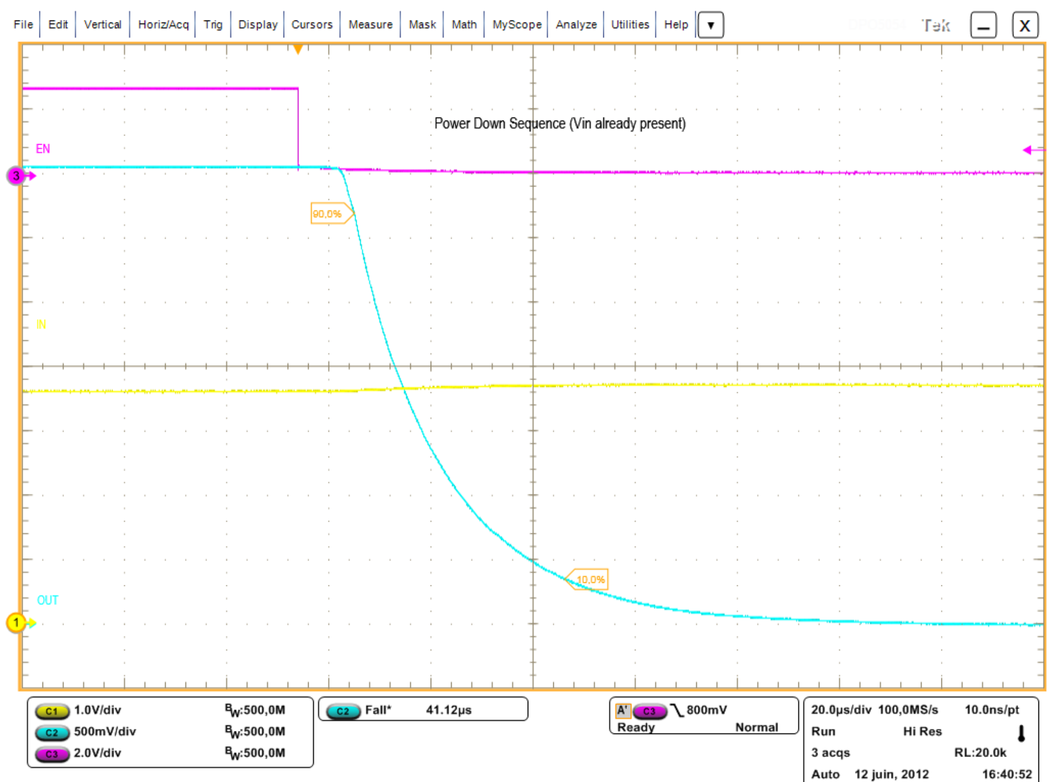


Figure 12. Disable Time and Fall Time

FUNCTIONAL DESCRIPTION

Overview

The NCP333 are a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.2 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.2 V and EN forced to high level.

Auto Discharge

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level, and Vin > 1.2 V.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at 70 Ω.

Soft Start

Each part has a gate soft start control (tr) in order to limit voltage ring when part is enable on a load.

Cin and Cout Capacitors

IN and OUT, 0.1 μF, at least, capacitors must be placed as close as possible the part for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

- $P_D = R_{DS(on)} \times (I_{OUT})^2$
  P_D = Power dissipation (W)
  $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
  I_{OUT} = Output current (A)
- $T_J = P_D \times R_{\theta JA} + T_A$
  T_J = Junction temperature (°C)
  $R_{\theta JA}$ = Package thermal resistance (°C/W)
  T_A = Ambient temperature (°C)

PCB Recommendations

The NCP333 integrates an up to 1.5 A rated PMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

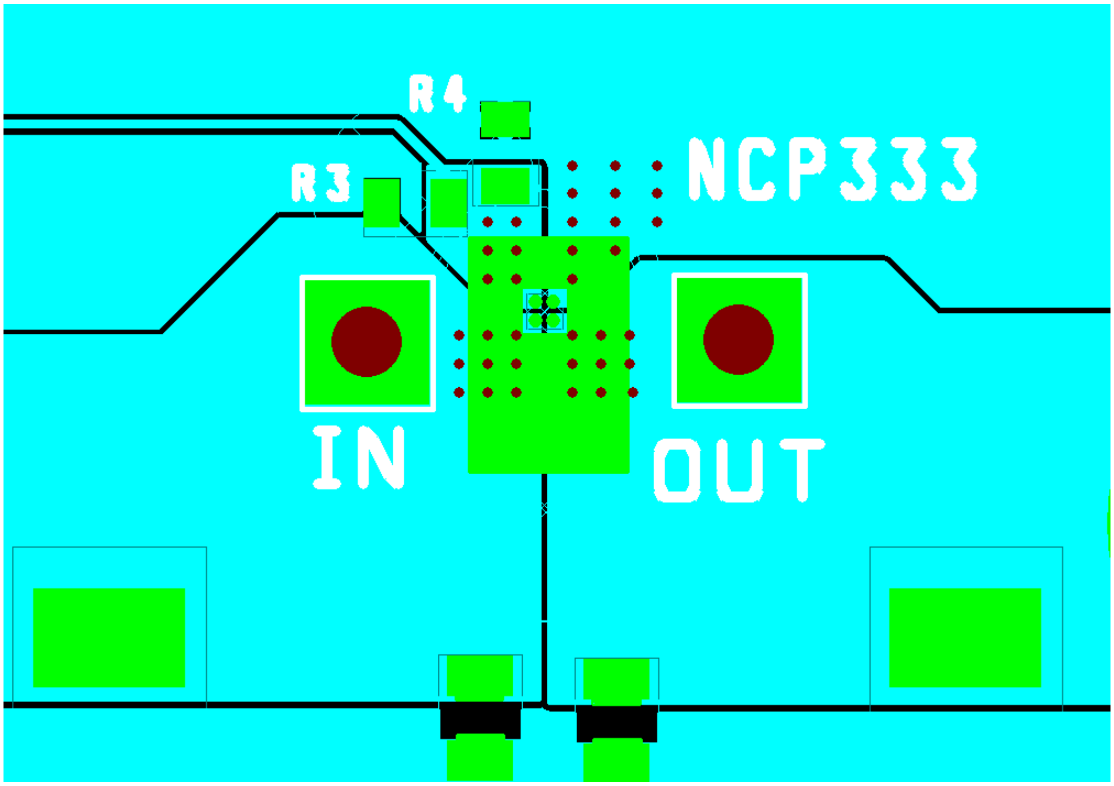


Figure 13. Routing Example: 2 oz, 4 Layers with Vias across 2 Internal Inners

Example of application definition.

$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DS(on)} \times I^2$

T_J: junction temperature.

T_A: ambient temperature.

$R_{\theta JA}$ = Thermal resistance between IC and air, through PCB.

$R_{DS(on)}$: intrinsic resistance of the IC Mosfet.

I: load DC current.

Taking into account of R_ obtain with:

- 1 oz, 2 layers: 150°C/W.

  At 1.5 A, 25°C ambient temperature, $R_{DS(on)}$ 45 mΩ @ Vin 5 V, the junction temperature will be:

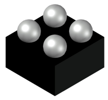
$T_J = T_A + R_{\theta JA} \times P_D = 25 + 150 \times 0.045 \times 1.5^2 = 40°C/W$

ORDERING INFORMATION

Device	Marking	Option	Package*	Shipping†
NCP333FCT2G	AE	Autodischarge	WLCSP 0.76 x 0.76 mm	3000 Tape / Reel
NCP333FCT2GA	AE	Autodischarge	WLCSP 0.76 x 0.76 mm	3000 Tape / Reel

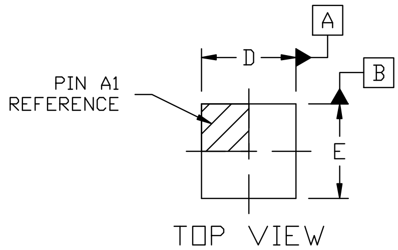
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*UBM = 205 μm



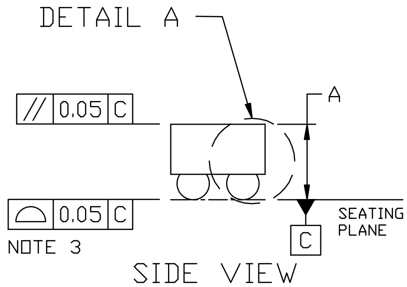
WLCSP4 0.76x0.76x0.605
CASE 567FJ
ISSUE C

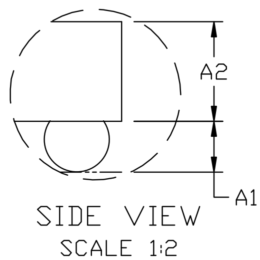
DATE 27 MAR 2023



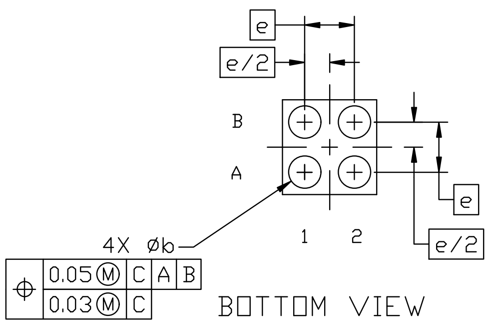
NOTES:

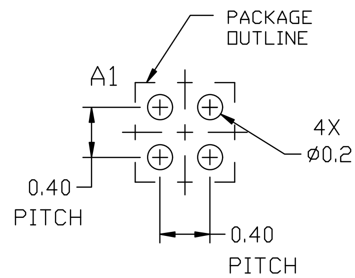
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.





DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.555	0.605	0.655
A1	0.180	0.205	0.230
A2	0.375	0.400	0.425
b	0.236	0.261	0.286
D	0.73	0.76	0.79
E	0.73	0.76	0.79
e	0.40 BSC		

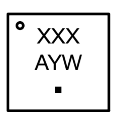




RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON79919E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WLCSP4 0.76x0.76x0.605**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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For additional information, please contact your local Sales Representative at
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