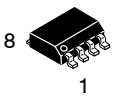
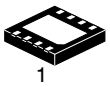
System Basis Chip with Integrated LIN and Voltage Regulator

NCV7428



SOIC−8
D SUFFIX



DFNW8
MW SUFFIX

Description

NCV7428 is a System Basis Chip (SBC) integrating functions typically found in automotive Electronic Control Units (ECUs). NCV7428 provides and monitors the low−voltage power supply for the application microcontroller and other loads and includes a LIN transceiver.

Features

- Control Logic
  - Ensures Safe Power−up Sequence and the Correct Reaction to Different Supply Conditions
  - Controls Mode Transitions Including the Power Management and Bus Wakeup Treatment
  - Generates Reset
- 3.3 V or 5 V V_{OUT} Supply Depending on the Version from a Low−drop Voltage Regulator
  - Can Deliver up to 70 mA with Accuracy of ±2%
  - Supplies Typically the ECU's Microcontroller
  - Undervoltage Detector with a Reset Output to the Supplied Microcontroller
- LIN Transceiver
  - LIN2.x and J2602 Compliant
  - TxD Dominant Timeout Protection
  - Transceiver Mode Controlled by Dedicated Input Pin
- Protection and Monitoring Functions
  - Thermal Shutdown Protection
  - Load Dump Protection (45 V)
  - LIN Bus Pin Protected Against Transients in an Automotive Environment
  - ESD Protection Level for LIN and V_S > ±8 kV
- Wettable Flank Package for Enhanced Optical Inspection

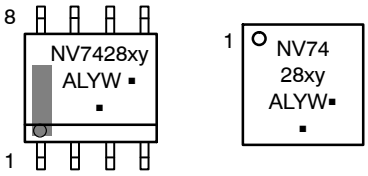
Quality

- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive
- Industrial Networks

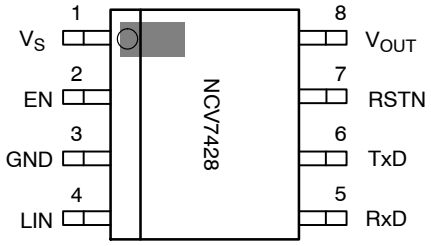
MARKING DIAGRAMS



NV7428 = Specific Device Code
x = − : Normal slope
L : Low slope
y = 3 : 3.3 V V_{OUT}
5 : 5.0 V V_{OUT}
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 17 of this data sheet.

BLOCK DIAGRAM

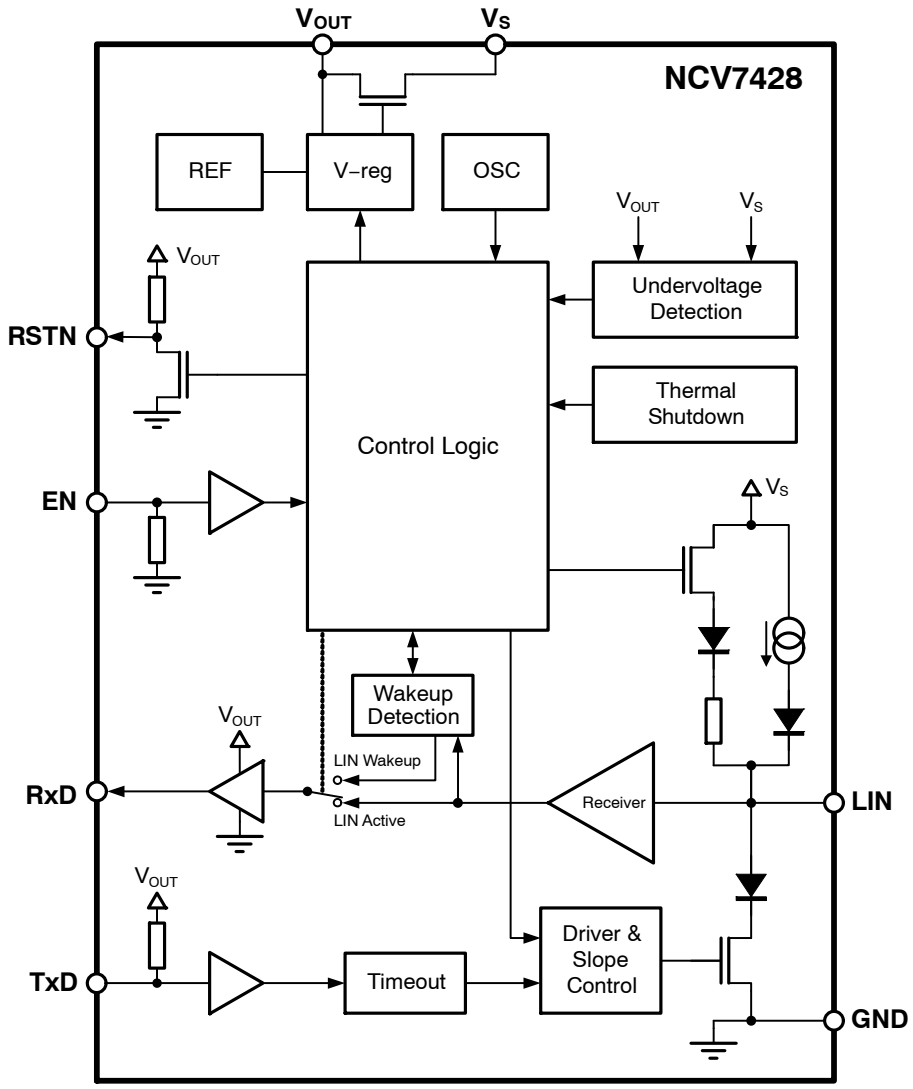


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Function
1	V_S	Battery supply input	Principle power supply of the device
2	EN	LV LIN enable input; internal pull−down	Input of the LIN block enable signal
3	GND	Ground connection	Ground connection
4	LIN	LIN bus interface	LIN bus line
5	RxD	LV digital output; push−pull	Output of data received on LIN bus
6	TxD	LV digital input; internal pull−up	Input of the data to be transmitted from LIN bus
7	RSTN	LV digital output; open drain; internal pull−up	System reset
8	V_{OUT}	LV supply output	Output of the 5 V or 3.3 V/70 mA low−drop regulator (for the MCU)
EP	EP	Exposed Pad	Connect to GND or leave floating

NOTE: (LV = Low Voltage; HV = High Voltage)

APPLICATION INFORMATION

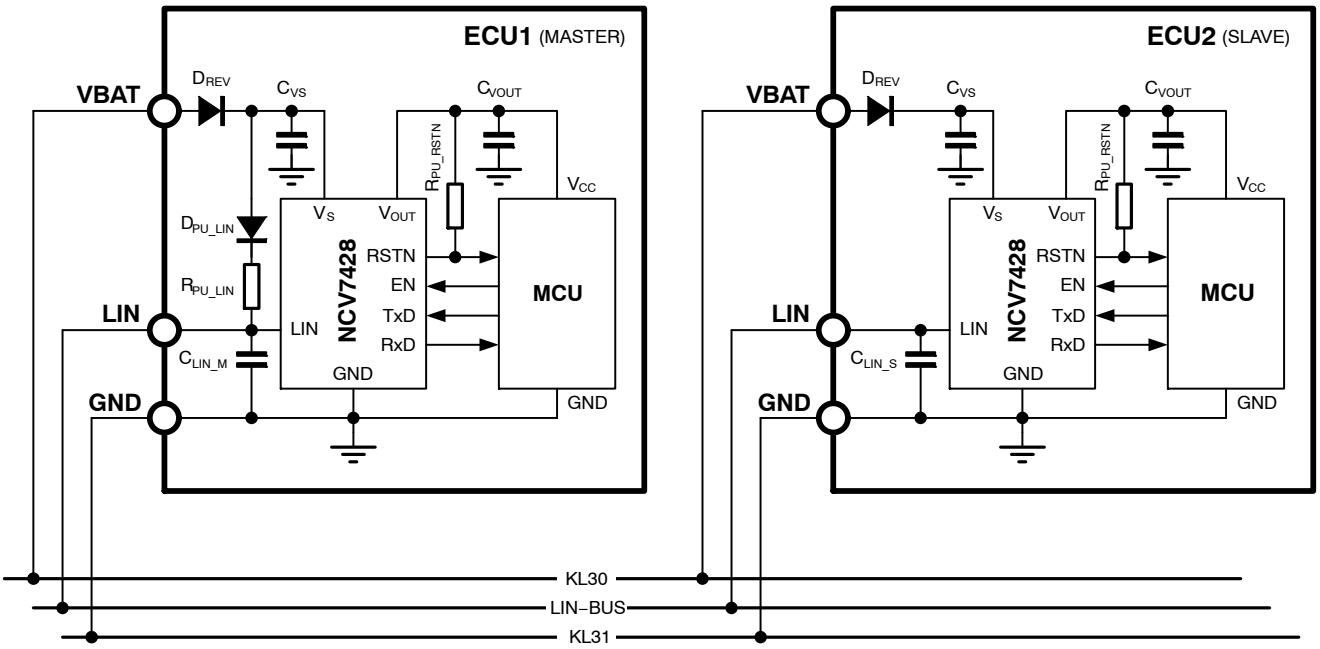


Figure 2. Example Application Diagram

External Components

Overview of external components from application schematic in Figure 2 is given in Table 2 together with their recommended or required values.

Table 2. EXTERNAL COMPONENTS OVERVIEW

Component Name	Description	Value	Note
D_{REV}	Reverse polarity protection diode	parameters application−specific; e.g. 0.5 A / 50 V	required values and types depend on the V_{OUT} load and the application needs
C_{VS}	Filtering capacitor for the battery input	recommended >100 nF ceramic	
C_{VOUT}	Voltage regulator output filtering and stabilization capacitor	> 1.8 μF, ESR < 7 Ω	
D_{PU_LIN}	Master node Pull−up diode on LIN line		required only for master LIN node
R_{PU_LIN}	Master node Pull−up resistor on LIN line	1 kΩ nominal, ≥500 mW	
C_{LIN_M}	Filtering capacitor on LIN line (Master node)	typically 1 nF	optional; is function of the entire LIN network
C_{LIN_S}	Filtering capacitor on LIN line (Slave node)	typically 100 pF − 220 pF	optional; is function of the entire LIN network
R_{PU_RSTN}	Pull−up resistor at RSTN pin	recommended 10 kΩ nominal	optional; depends on application needs

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_S	Maximum DC voltage at V_S pin	−0.3	45	V
V_{OUT}	Maximum voltage at V_{OUT} pin	−0.3	6	V
V_{LIN}	Maximum voltage at LIN bus pin	−45	45	V
$V_{Dig\_IO\_inputs}$	Maximum voltage at digital input pins (TxD, EN)	−0.3	45	V
$V_{Dig\_IO\_outputs}$	Maximum voltage at digital output pins (RxD, RSTN)	−0.3	V_{OUT}+0.3	V
T_J	Junction temperature range	−40	+170	°C
T_{STG}	Storage temperature range	−55	+150	°C
V_{ESD}	System ESD at pins VS, LIN as per IEC 61000−4−2: 330 Ω / 150 pF (Verified by external test house)	≥ ±14		kV
	Human body model at pins VS, LIN stressed towards GND with 1500 Ω / 100 pF	≥ ±8		kV
	Human body model at all pins as per JESD22−A114 / AEC−Q100−002	≥ ±4		kV
	Charge device model at all pins as per JESD22−C101 / AEC−Q100−011	≥ ±500		V
	Machine model; (200 pF; 0.75 μH; 10 Ω) as per JESD22−A115 / AEC−Q100−003	±200		V
MSL	Moisture Sensitivity Level SOIC DFN	2 1		−
T_{SLD}	Lead temperature Soldering − Reflow (SMD styles only), Pb−Free (Note 1)	260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 4. OPERATING RANGES

Symbol	Parameter	Min	Max	Units
V_S	VS operating voltage for parametric operation (Note 2)	5.5	28	V
	VS operating voltage for limited operation (Note 2)	4	28	V
I_{VOUT}	Current delivered by the V_{OUT} regulator	70	−	mA
V_{LIN}	Operating voltage at LIN bus pin	0	V_S	V
$V_{Dig\_IO\_inputs}$	Operating voltage at digital input pins (TxD, EN)	0	5.5	V
$V_{Dig\_IO\_outputs}$	Operating voltage at digital output pins (RxD, RSTN)	0	V_{OUT}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Below 5.5 V at V_S pin in normal mode, the bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit. Above 28 V at V_S pin, LIN communication is operational (LIN pin toggling) but parameters cannot be guaranteed. For higher battery voltage operation above 28 V, LIN pull−up resistor must be selected large enough to avoid clamping of LIN pin by voltage drop over external pull−up resistor and LIN pin min current limitation.

Table 5. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 (Note 3) Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 4) Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 5)	 $R_{\theta JA}$ $R_{\theta JA}$	 125 75	 °C/W °C/W
Thermal Characteristics, DFN−8 (Note 3) Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 4) Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 5)	 $R_{\theta JA}$ $R_{\theta JA}$	 133 55	 °C/W °C/W

3. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
4. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
5. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage for the signal layer and 4 thermal vias connected between exposed pad and first inner Cu layer.

Definitions

The characteristics defined in this section are guaranteed within the operating ranges listed in Table 4, unless stated otherwise. All voltages are referenced to GND (Pin 3). Positive currents flow into the respective pin.

Table 6. DC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_S to LIN); unless otherwise specified. Typical values are given at V_S = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY MONITORING						
V_{S_PORH}	V_S threshold for the power−up of the circuit	V_S rising	3.3	–	4	V
V_{S_PORL}	V_S threshold for the Shutdown of the circuit	V_S falling	2.2	–	3	V
$V_{OUT\_RES\_5}$	V_{OUT} monitoring threshold NV7428−5	V_{OUT} falling	4.55	–	4.75	V
$V_{OUT\_RES\_33}$	V_{OUT} monitoring threshold NV7428−3	V_{OUT} falling	2.97	–	3.135	V
$V_{OUT\_RES\_hys5}$	V_{OUT} monitoring threshold hysteresis for NV7428−5		–	0.1	–	V
$V_{OUT\_RES\_hys33}$	V_{OUT} monitoring threshold hysteresis for NV7428−3		–	0.06	–	V
CURRENT CONSUMPTION						
$I_{VS\_LIN\_Active\_rec}$	V_S supply current	LIN Active, LIN bus recessive	–	–	1.8	mA
$I_{VS\_LIN\_Wakeup}$	V_S supply current (Note 8)	Standby mode; LIN Wakeup, LIN bus recessive; I_{VOUT} = 0 mA V_S = 13.5 V, T_J < 105°C	–	25	33	μA
I_{VS_Sleep}	V_S supply current (Note 8)	Sleep mode; LIN Wakeup, LIN bus recessive; V_{OUT} off, V_{OUT} < 0.5 V V_S = 13.5 V, T_J < 105°C	–	12	18	μA
V_{OUT} REGULATOR						
V_{OUT_5}	V_{OUT} regulator output voltage (Note 6)	V_{OUT} regulator active, 0 < I_{VOUT} < 70 mA, Static regulation, V_S = 5.5 V to 28 V	4.9	5	5.1	V
V_{OUT_33}	V_{OUT} regulator output voltage (Note 6)	V_{OUT} regulator active, 0 < I_{VOUT} < 70 mA, Static regulation, V_S = 4.5 V to 28 V	3.234	3.3	3.366	V
$V_{OUT\_5\_EMC}$	V_{OUT} regulator output voltage under EMC (Note 8)	DPI EMC test applied to LIN pin. No bus capacitor. SOIC8 package; (Note 7)	4.85	5	5.15	V
$V_{OUT\_33\_EMC}$	V_{OUT} regulator output voltage under EMC (Note 8)	DPI EMC test applied to LIN pin. No bus capacitor. SOIC8 package; (Note 7)	3.201	3.3	3.399	V
I_{LIM_VOUT}	V_{OUT} current limitation	V_{OUT} regulator active; current flowing to V_{OUT} load	70	120	350	mA
V_{DROP_VOUT}	Drop−out voltage between V_S and V_{OUT}	5.5 V < V_S < 40 V; I_{VOUT} = 70 mA	–	–	0.55	V
I_{SINK_VOUT}	V_{OUT} sink current	V_{OUT} regulator active, current flowing into the V_{OUT} pin	100	240	400	μA
C_{VOUT}	V_{OUT} regulator filtering capacitance (Note 9)	Equivalent series resistance < 7 Ω	1.8	10	–	μF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. In case LIN bus capacitor of at least 82 pF is not used $V_{OUT\_5\_EMC}$ and $V_{OUT\_33\_EMC}$ needs to be taken into account.
7. Tested according to: LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008. Verified by external test house.
8. Values based on design and characterization. Not tested in production.
9. In parallel with this capacitor any other capacitor can be placed with no limit to ESR and capacitance value
10. The voltage drop in Normal mode between LIN and V_S pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 6. DC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_S to LIN); unless otherwise specified. Typical values are given at V_S = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
$V_{LIN\_dom\_LoSup}$	LIN dominant output voltage	TxD = Low; V_S = 7.3 V	–	–	1.2	V
$V_{LIN\_dom\_HiSup}$	LIN dominant output voltage	TxD = Low; V_S = 18 V	–	–	2.0	V
V_{LIN_REC}	LIN recessive output voltage	TxD = High; I_{LIN} = 10 μA (Note 10)	V_S – 1.5	–	V_S	V
I_{LIN_lim}	Short circuit current limitation	V_{LIN} = V_S = 18 V	40	–	200	mA
R_{slave}	Internal Pull−up Resistance	LIN Normal or Receive−only mode	20	33	47	kΩ
C_{LIN}	Capacitance at pin LIN (Note 8)		–	20	30	pF
LIN Receiver						
V_{bus_dom}	Bus voltage for Dominant state		–	–	0.4	V_S
V_{bus_rec}	Bus voltage for Recessive state		0.6	–		V_S
V_{rec_dom}	Receiver threshold	LIN bus going from Recessive to Dominant	0.4	–	0.6	V_S
V_{rec_rec}	Receiver threshold	LIN bus going from Dominant to Recessive	0.4	–	0.6	V_S
V_{rec_cnt}	Receiver center voltage	(V_{rec_dom} + V_{rec_rec})/2	0.475	–	0.525	V_S
V_{rec_hys}	Receiver hysteresis	V_{rec_rec} − V_{rec_dom}	0.05	–	0.175	V_S
$I_{LIN\_off\_dom}$	LIN output current, Bus in dominant state	LIN Active Mode, Driver Off; V_S = 12 V, V_{LIN} = 0 V	−1	–	–	mA
$I_{LIN\_off\_dom\_wake}$	LIN output current, Bus in dominant state	LIN Wakeup Mode; V_S = 12 V, V_{LIN} = 0 V	−20	−15	−2	μA
$I_{LIN\_off\_rec}$	LIN output current, Bus in recessive state	Driver Off; V_S < 18 V; V_S < V_{LIN} < 18 V	–	–	1	μA
$I_{LIN\_no\_GND}$	LIN current with missing GND	V_S = GND = 12 V; 0 < V_{LIN} < 18 V	−1	–	1	mA
$I_{LIN\_no\_VBB}$	LIN current with missing V_S	V_S = GND = 0 V; 0 < V_{LIN} < 18 V	–	–	5	μA
PIN EN						
V_{IL_EN}	Low−level input voltage		−0.3	–	0.8	V
V_{IH_EN}	High−level input voltage		2	–	5.5	V
$R_{pulldown\_EN}$	Pull−down resistance to GND		55	100	185	kΩ
PIN TxD						
V_{IL_TxD}	Low−level input voltage		−0.3	–	0.8	V
V_{IH_TxD}	High−level input voltage		2	–	5.5	V
R_{pullup_TxD}	Pull−up resistance to V_{OUT}		55	100	185	kΩ
I_{leak_TxD}	Leakage current	V_{TxD} = V_{OUT} = 5.5 V	−1	0	1	μA
PIN RSTN						
I_{OL_RSTN}	Low−level output driving current	V_S = 4 V to 28 V; V_{RSTN} = 0.4 V	4	–	30	mA
V_{OL_RSTN}	Low−level output voltage	V_S = 2 V to 4 V; V_{OUT} = 0 V to 5.5 V; I_{RSTN} = 100 μA	–	–	0.1	V_{OUT}
		V_S < 2 V; V_{OUT} = 1 V to 5.5 V; I_{RSTN} = 100 μA	–	–	0.1	V_{OUT}
R_{pullup_RSTN}	Pull−up resistance to V_{OUT}		55	100	185	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. In case LIN bus capacitor of at least 82 pF is not used $V_{OUT\_5\_EMC}$ and $V_{OUT\_33\_EMC}$ needs to be taken into account.
7. Tested according to: LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008. Verified by external test house.
8. Values based on design and characterization. Not tested in production.
9. In parallel with this capacitor any other capacitor can be placed with no limit to ESR and capacitance value
10. The voltage drop in Normal mode between LIN and V_S pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 6. DC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; Bus Load = 500 Ω (V_S to LIN); unless otherwise specified. Typical values are given at V_S = 12 V and T_J = 25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PIN RSTN						
$V_{S\_DigOut\_Low}$	V_S level guaranteeing Low level at RSTN pin	Shutdown mode; Low level guaranteed for $V_S > V_{S\_DigOut\_Low}$	–	–	2	V
PIN RxD						
I_{OL_RXD}	Low−level output driving current	V_{RxD} = 0.4 V	0.4	–	–	mA
I_{OH_RXD}	High−level output driving current	$V_{RXD} = V_{OUT}$ − 0.4 V	–	–	−0.16	mA
THERMAL SHUTDOWN						
T_{J_SD}	Junction temperature for thermal Shutdown		160	180	200	°C
$T_{J\_SD\_hys}$	Thermal Shutdown hysteresis		–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. In case LIN bus capacitor of at least 82 pF is not used $V_{OUT\_5\_EMC}$ and $V_{OUT\_33\_EMC}$ needs to be taken into account.
7. Tested according to: LIN Conformance Test Specification Package for LIN 2.1, October 10th, 2008. Verified by external test house.
8. Values based on design and characterization. Not tested in production.
9. In parallel with this capacitor any other capacitor can be placed with no limit to ESR and capacitance value
10. The voltage drop in Normal mode between LIN and V_S pin is the sum of the diode drop and the drop at serial pull−up resistor. The drop at the switch is negligible. See Figure 1.

Table 7. AC CHARACTERISTICS (V_S = 5.5 V to 28 V; T_J = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	Normal slope $TH_{REC(max)}$ = 0.744 x V_S $TH_{DOM(max)}$ = 0.581 x V_S t_{BIT} = 50 μs V_S = 7 V to 18 V	0.396	–	0.5	–
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	Normal slope $TH_{REC(min)}$ = 0.422 x V_S $TH_{DOM(min)}$ = 0.284 x V_S t_{BIT} = 50 μs V_S = 7.6 V to 18 V	0.5	–	0.581	–
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x t_{BIT})	Normal and Low slope $TH_{REC(max)}$ = 0.778 x V_S $TH_{DOM(max)}$ = 0.616 x V_S t_{BIT} = 96 μs V_S = 7 V to 18 V	0.417	–	0.5	–
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x t_{BIT})	Normal and Low slope $TH_{REC(min)}$ = 0.389 x V_S $TH_{DOM(min)}$ = 0.251 x V_S t_{BIT} = 96 μs V_S = 7.6 V to 18 V	0.5	–	0.590	–
t_{fallNS}	LIN falling edge normal slope	Normal Mode; V_S = 12 V	–	–	22.5	μs
t_{riseNS}	LIN rising edge normal slope	Normal Mode; V_S = 12 V	–	–	22.5	μs
t_{symNS}	LIN slope symmetry normal slope	Normal Mode; V_S = 12 V	−4	0	4	μs
t_{fallLS}	LIN falling edge low slope (Note 12)	Normal Mode; V_S = 12 V	–	–	45	μs
t_{riseLS}	LIN rising edge low slope (Note 12)	Normal Mode; V_S = 12 V	–	–	45	μs
$t_{tx\_prop\_down}$	Propagation Delay of TxD to LIN. TxD high to low	(Note 11)	–	–	10	μs
$t_{tx\_prop\_up}$	Propagation Delay of TxD to LIN. TxD low to high	(Note 11)	–	–	10	μs
$t_{TxD\_timeout}$	TxD dominant timeout	TxD = Low; LIN dominant timeout enabled	9	13	24	ms
LIN RECEIVER						
$t_{rec\_prop\_down}$	Propagation delay of receiver falling edge		0.1	–	6	μs
$t_{rec\_prop\_up}$	Propagation delay of receiver rising edge		0.1	–	6	μs
t_{rec_sym}	Propagation delay symmetry	$t_{rec\_prop\_down}$ − $t_{rec\_prop\_up}$	−2	–	2	μs
t_{LIN_wake}	Dominant duration for wakeup	LIN in wakeup mode	30	80	150	μs
MODE TRANSITIONS AND TIMEOUTS						
t_{sample_txd}	Low power mode entry EN to TxD sampling point delay	Normal mode: Figure 9, Figure 10	13	25	55	μs
t_{mode}	Normal mode or Reset mode transition time	Low power mode: Figure 9, Figure 10	13	25	55	μs
t_{lp_mode}	Low power mode transition time (Standby or Sleep)	Normal mode: Figure 9, Figure 10	27	45	91	μs
t_{reset}	RSTN pulse extension	Figure 6, Figure 7, Figure 8	3	5	10	ms
$t_{VOUT\_RES\_filt}$	Undervoltage detection filter time	Figure 6	13	25	55	μs

11. Values based on design and characterization. Not tested in production.
12. For low slope versions only (NV7428L5 and NV7428L3)

FUNCTIONAL DESCRIPTION

VS Supply Input

V_S pin of NCV7428 is typically connected to the car battery through a reverse−protection diode and can be exposed to all relevant automotive disturbances (ISO7637 pulses, system ESD ...). V_S supplies mainly the integrated LIN transceiver. Filtering capacitors should be connected between V_S and GND.

During power−up of the battery supply, V_S pin must reach V_{S_PORH} level in order for the circuit to become functional – the internal state machine is initiated and the V_{OUT} regulator is activated. The circuit remains functional until V_S falls back below V_{S_PORL} level, when the device enters the Shutdown mode.

VOUT Low−drop Voltage Regulator

The application low−voltage supply is provided by an integrated low−drop voltage regulator delivering a 5 V or 3.3 V output V_{OUT}. It is able to deliver up to 70 mA with given precision and is primarily intended to supply the application microcontroller unit (MCU) and related 5 V or 3.3 V loads (e.g. its own MCU−related digital inputs/ outputs). An external capacitor needs to be connected on V_{OUT} pin in order to ensure the regulator's stability and to filter the disturbances caused by the connected loads.

All low−voltage digital pins are related to V_{OUT}.

LIN Transceiver

NCV7428 integrates on−chip LIN transceiver interface between physical LIN bus and the LIN protocol controller.

This LIN physical layer is compatible to LIN2.x and J2602 specifications.

NCV7428 LIN2.2 compliant physical layer can be combined on the network with all previous LIN physical layers.

NCV7428 LIN transceiver consists of a transmitter, receiver and wakeup detector. The LIN transceiver can be connected to the bus line via LIN pin, and to the digital control through pins TxD and RxD. The functional mode of the LIN transceiver depends on the operating mode and on EN pin state – see Figure 3. The LIN transceiver is supplied directly from the V_S pin.

LIN Operating Modes

In **LIN Active mode** the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud for normal slope mode and 10 kBaud/s for low slope version. The transmit data stream of the LIN protocol is present on the TxD pin and converted by the transmitter into a LIN bus signal with controlled slew rate to minimize EMC emission. The receiver consists of the comparator that has a threshold with hysteresis in respect to the supply voltage and an input filter to remove bus noise. The LIN output is pulled HIGH via an internal pull−up resistor (typ. 30 kΩ). For master applications, it is needed to put an external resistor (typ. 1 kΩ) with a serial diode between LIN and V_S. The mode selection is done by EN = High.

The transmission is only initiated with the TxD falling edge in LIN Active mode. Entering this mode with TxD already Low will not lead to transmitting bus Dominant signal.

When leaving Normal mode (EN pin falling edge), the transmitter is deactivated immediately.

The **LIN Wakeup mode** can be entered if the EN pin is Low. The LIN receiver stays active to be able to detect a remote wake−up via bus. The LIN transmitter is disabled and the slave internal termination resistor of 30 kΩ between LIN and V_S is disconnected in order to minimize current consumption. Only a pull−up current source between Vs and LIN is active. The valid LIN wakeup event causes driving RxD Low until EN pin is pulled High.

A Wakeup pattern that is initiated in LIN Active mode and ends in LIN Wakeup mode is also considered a valid Wakeup event.

The LIN Wakeup mode is also forced if the device enters to the Sleep operating mode.

The **LIN Off mode** provides extreme low current consumption, LIN transceiver is fully deactivated. Pin RxD stays High (as long as V_{OUT} is provided) and logical level on TxD is ignored.

The bus pin is internally pulled to V_S with a current source (thus limiting V_S consumption in case of a permanent LIN short to GND).

This mode is entered when NCV7428 is in Shutdown mode ($V_S < V_{S\_PORL}$) or in Thermal Shutdown mode ($T_J > T_{J\_SD}$).

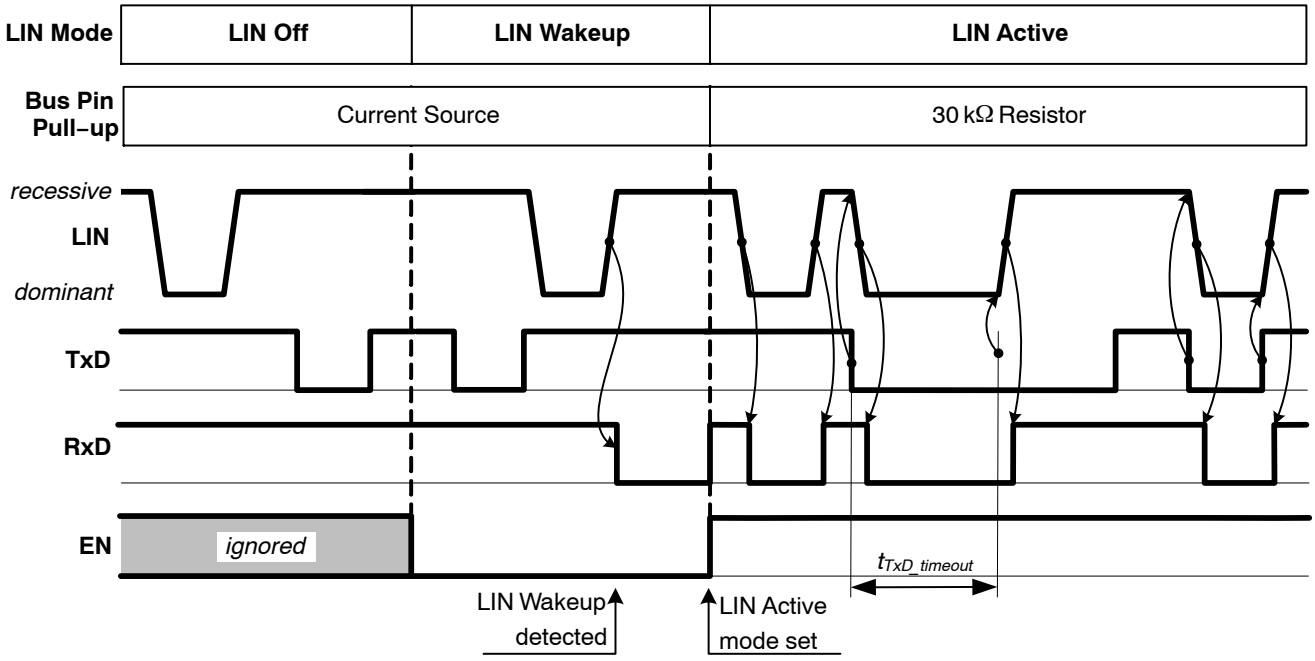


Figure 3. LIN Modes

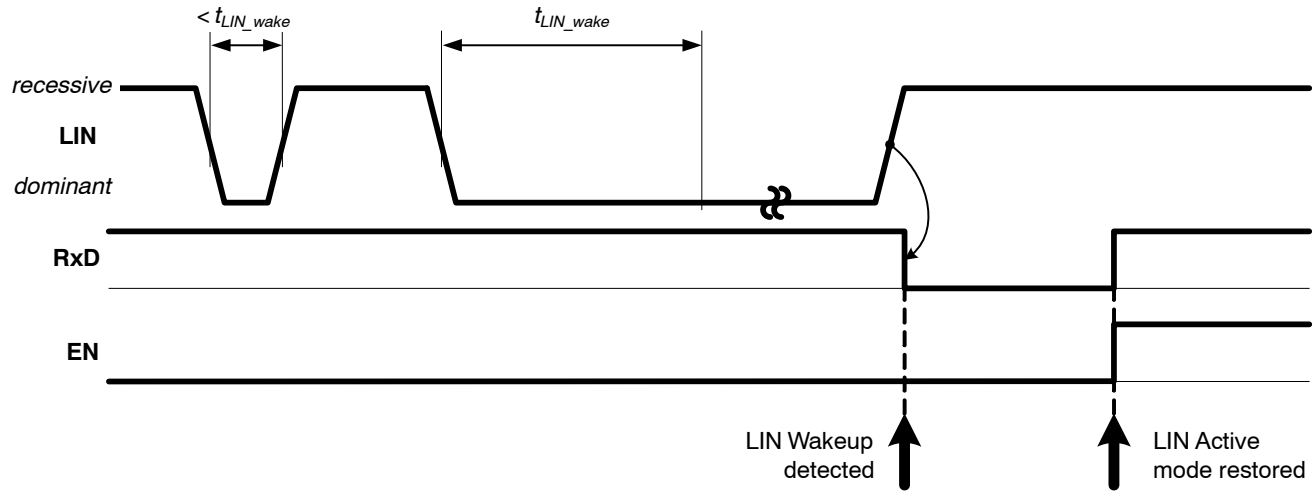


Figure 4. LIN Wakeup Detection

OPERATING MODES

The principal operating modes of NCV7428 are shown in Figure 5 and described in the following paragraphs.

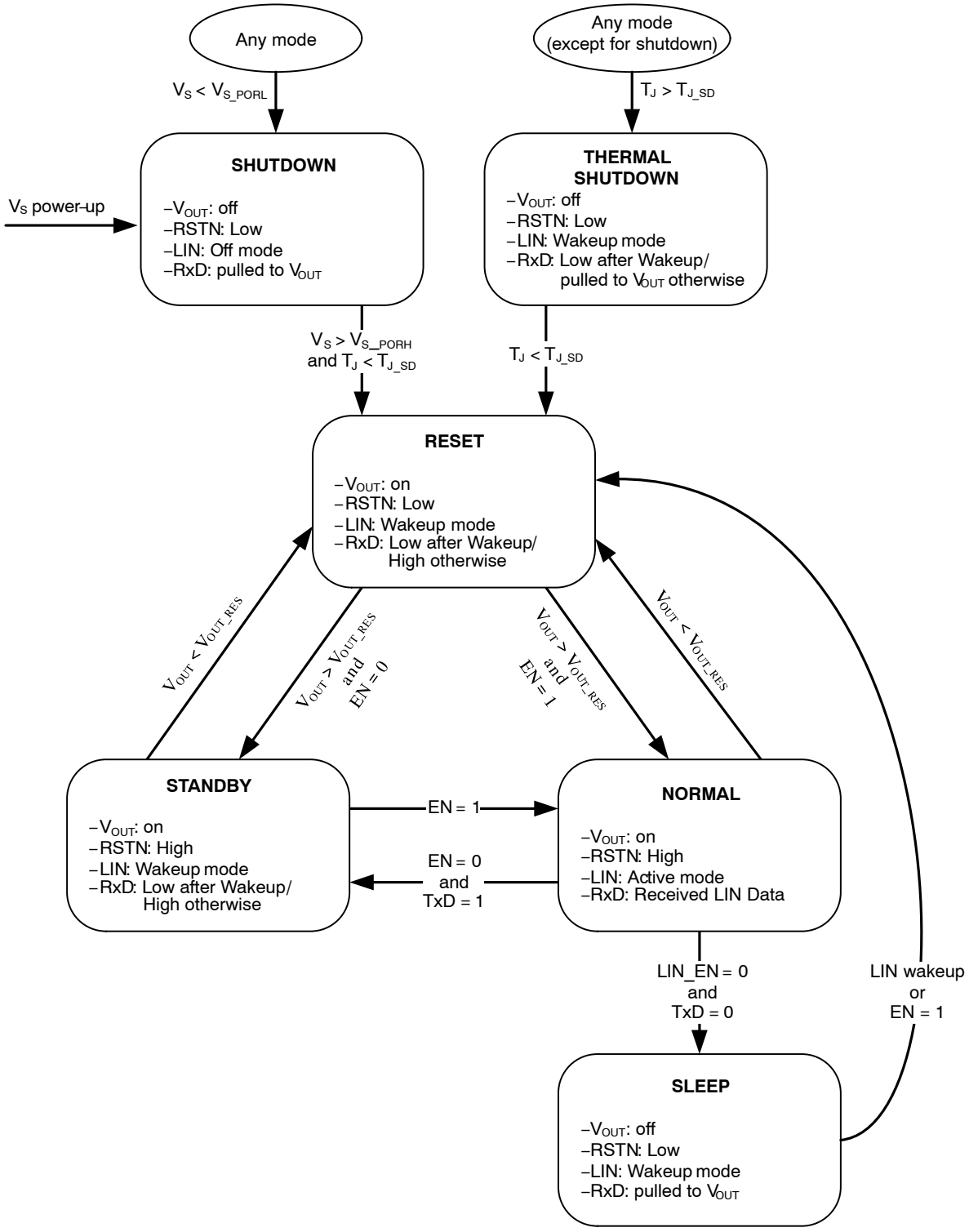


Figure 5. Operating Modes

Shutdown Mode

The Shutdown mode is a passive state, in which all NCV7428 resources are inactive. The Shutdown mode provides a defined starting point for the circuit in case of supply undervoltage, thermal Shutdown or the first supply connection.

On−chip power−supply V_{OUT} is switched off and the LIN pin remains passive so that it does not disturb the communication of other nodes connected to the LIN bus. RxD pin stays pulled to V_{OUT}. No wakeups can be detected.

RSTN pin is forced Low – RSTN Low level is guaranteed for V_S supply above $V_{S\_DigOut\_Low}$.

The Shutdown mode is entered asynchronously whenever the V_S level falls below the power−on−reset level V_{S_PORL}.

The Shutdown mode is left only when the V_S supply exceeds the high power−on−reset level V_{S_PORH} while junction temperature is below T_{J_SD}. When exiting the Shutdown mode, NCV7428 always enters the Reset mode.

RESET Mode

The Reset mode is a transient mode providing a defined RSTN pulse for the application microcontroller.

V_{OUT} supply is kept active. The LIN pin is passive so that it does not disturb the communication of other nodes connected to the bus. RxD pin is High if no wakeup was detected, RxD Low level indicates pending LIN wakeup. Pin RSTN is forced Low.

Reset mode will be entered as a consequence of one of the following events:

- Shutdown mode is exited
- Thermal Shutdown mode is exited
- V_{OUT} voltage falls below V_{OUT_RES} level
- LIN wakeup or EN = High was detected in Sleep mode

Normally, the Reset mode is left when V_{OUT} voltage is above V_{OUT_RES} threshold and defined time t_{reset} elapses. The RSTN pin is internally released to High and the chip then goes to the Normal or Standby mode, depending on EN state.

Normal Mode

Normal mode is entered from Standby mode after a host request – driving EN pin High (Figure 9), or if EN pin is High when leaving Reset mode – t_{reset} time elapsed (Figure 8).

LIN transceiver is in Active mode. V_{OUT} is kept on. Pin RSTN remains High.

Standby Mode

Standby mode is entered from Normal mode after host request – EN pin falling edge followed by TxD pin High. TxD is sampled t_{sample_txd} after EN edge (Figure 9). Standby mode is also entered if EN pin is Low when leaving Reset mode – t_{reset} time elapsed (Figure 7).

LIN transceiver is in Wakeup mode – RxD pin is latched Low after valid Wakeup recognition until Normal mode is requested. V_{OUT} is kept active. Pin RSTN remains High.

Sleep Mode

Sleep mode can be only entered from Normal mode after a host request – EN pin falling edge followed by TxD pin Low. LIN transmitter is blocked immediately after EN pin falling edge, therefor TxD pin and EN pin can be set Low at the same moment. TxD is sampled t_{sample_txd} after EN pin edge (Figure 10).

V_{OUT} regulator is switched off, LIN transceiver is in the Wakeup mode.

If LIN wakeup is detected or EN goes High, Reset mode is entered. LIN wakeup is signaled by RxD, which remains Low until Normal mode is restored (EN is High).

Thermal Shutdown

The device junction temperature is monitored in order to avoid permanent degradation or damage of the chip. Junction temperature exceeding the Shutdown level T_{J_SD} puts the chip into Thermal Shutdown mode.

In Thermal Shutdown mode, V_{OUT} regulator is switched off. LIN transceiver is in Wakeup mode and can detect bus Wakeup. RxD pin stays pulled to V_{OUT} or is driven Low after valid Wakeup recognition. RSTN pin is pulled low. The mode is automatically left only when the junction cools down below the T_{J_SD} threshold.

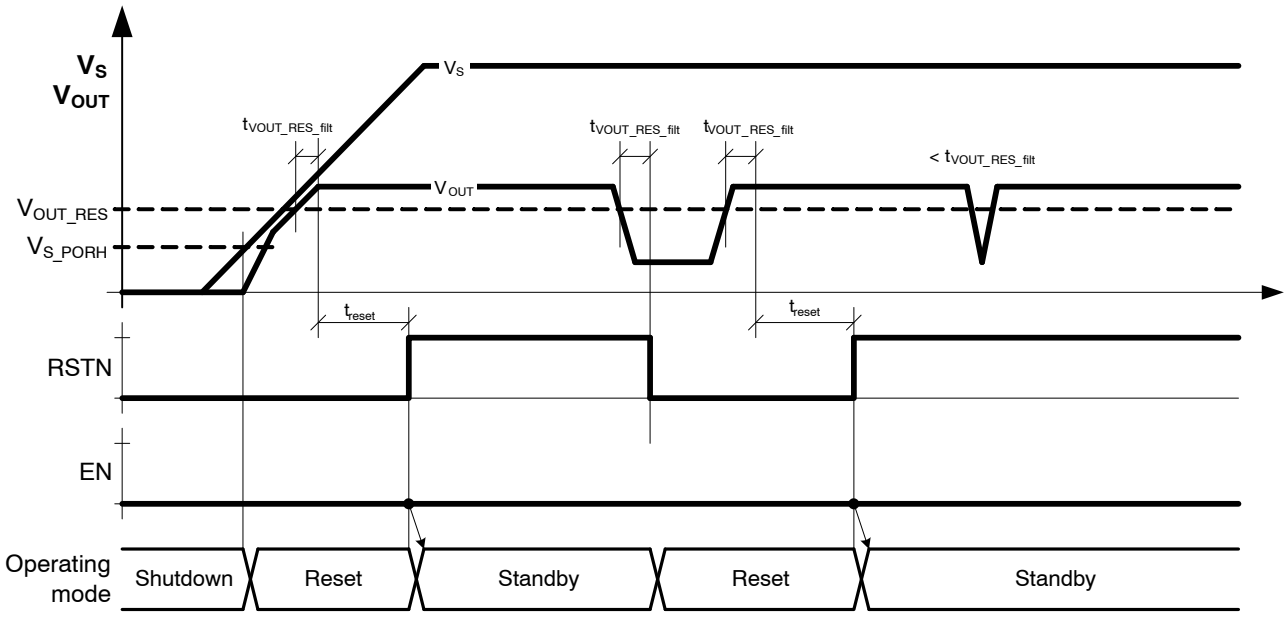


Figure 6. V_{OUT} Regulator Voltage Monitoring

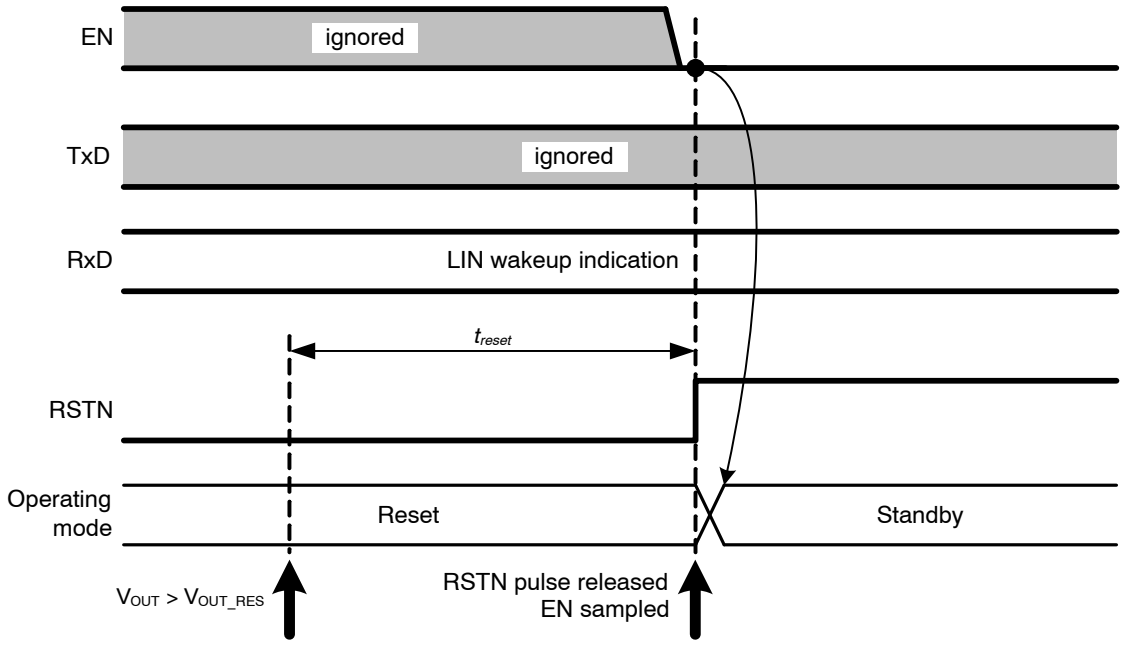


Figure 7. Operating Modes, Transition from Reset to Standby Mode

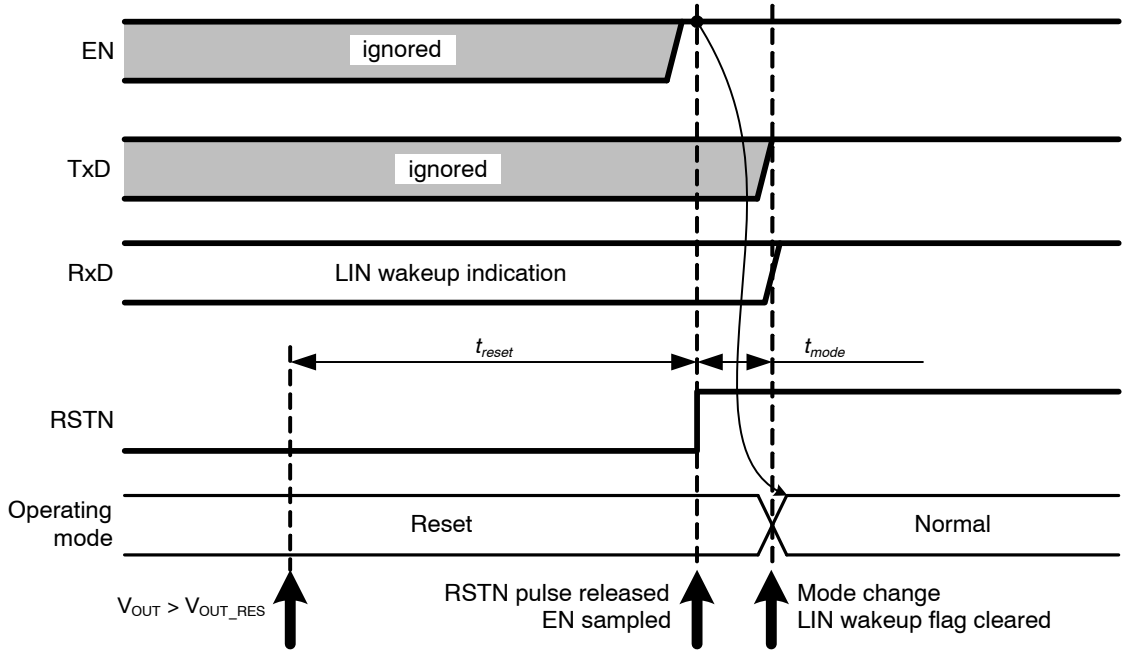


Figure 8. Operating Modes, Transition from Reset to Normal Mode

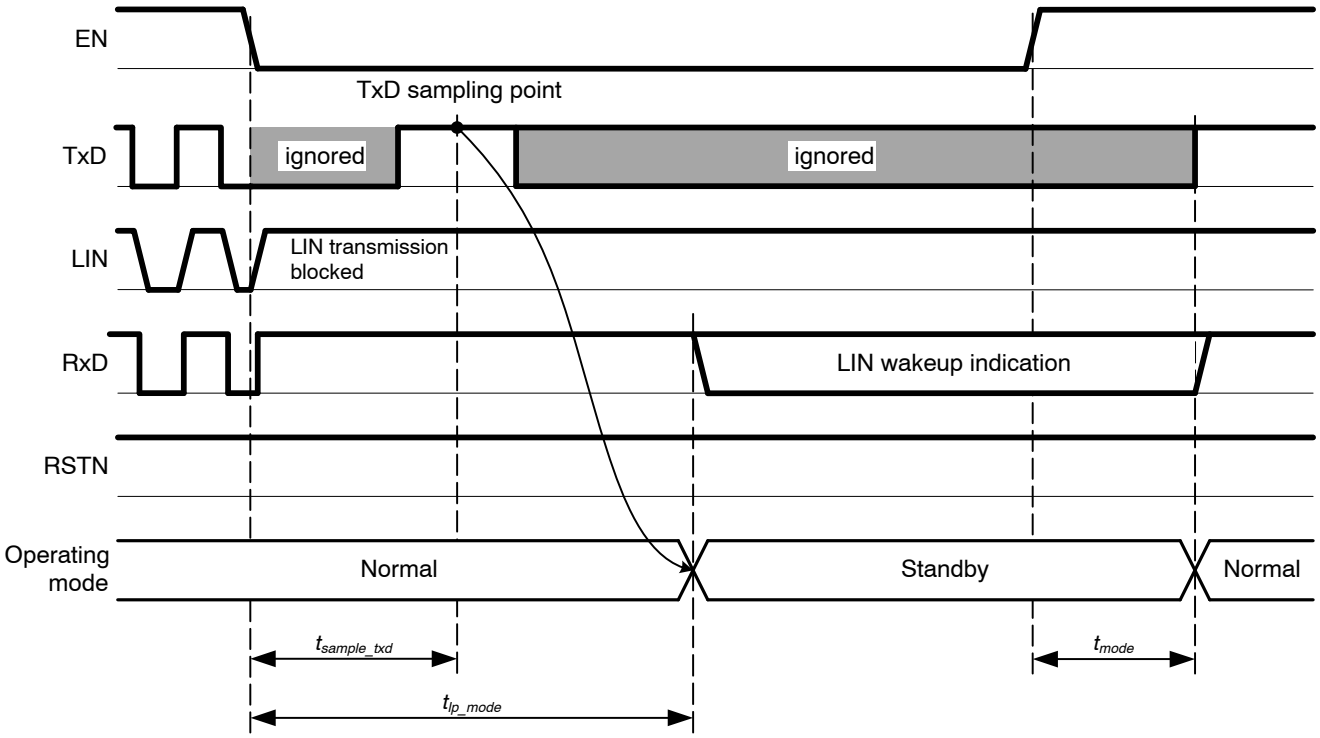


Figure 9. Operating Modes, Transition from Normal to Standby Mode

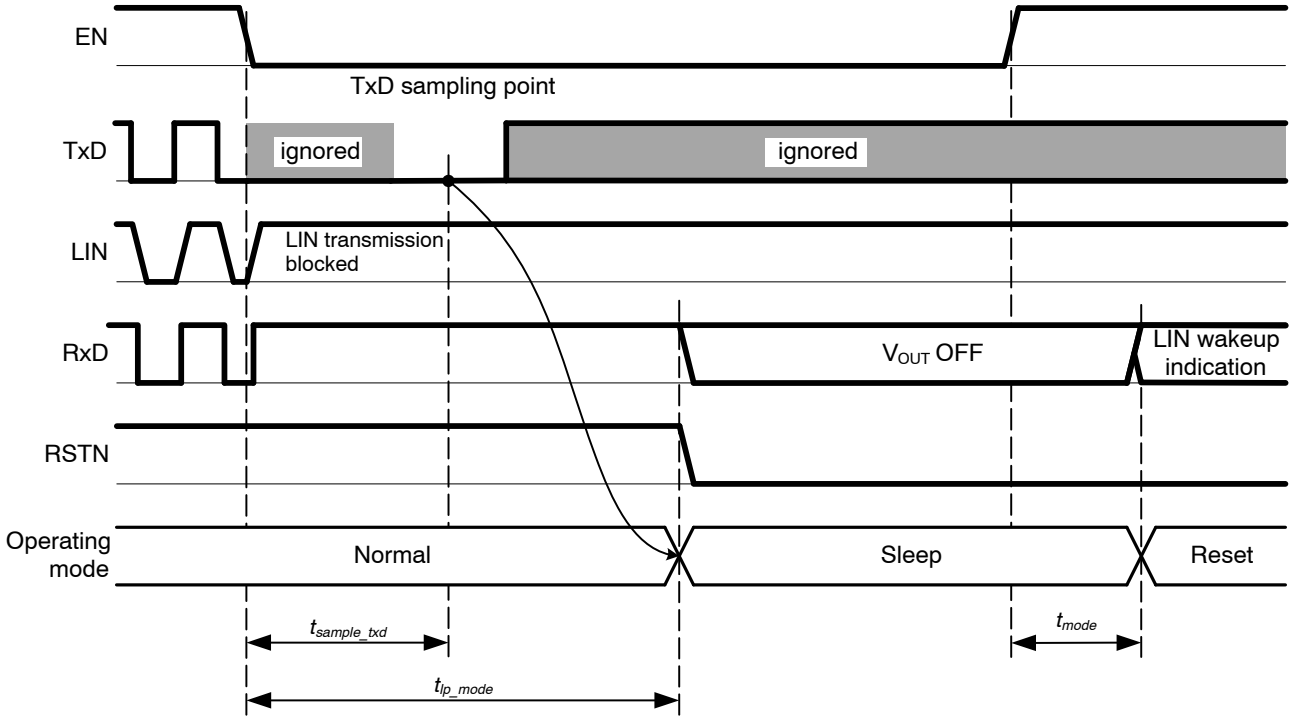


Figure 10. Operating Modes, Transition from Normal to Sleep Mode

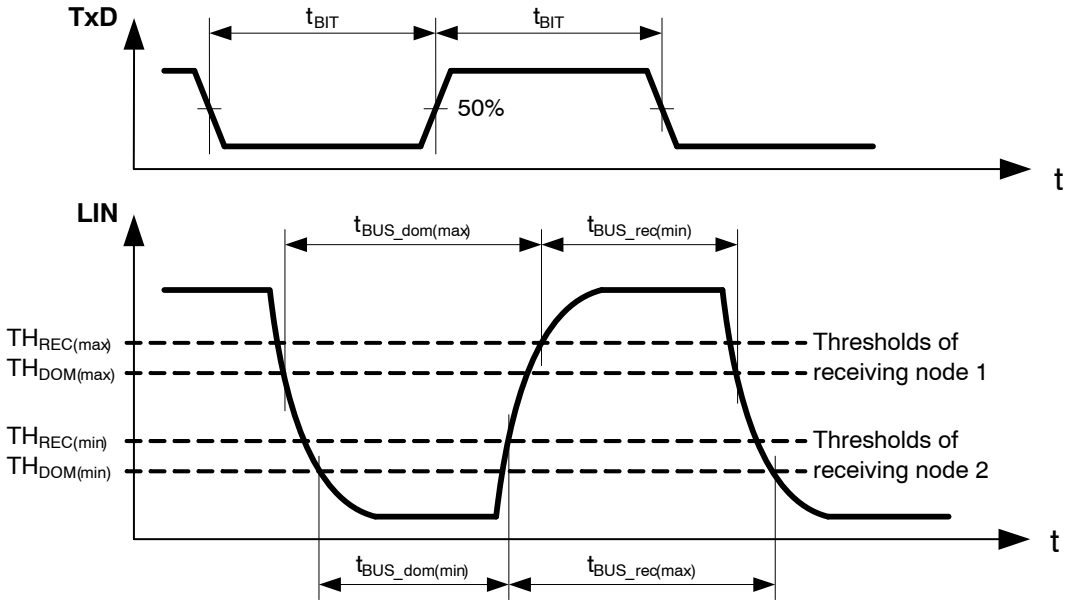


Figure 11. Definition of LIN Duty Cycle Parameters

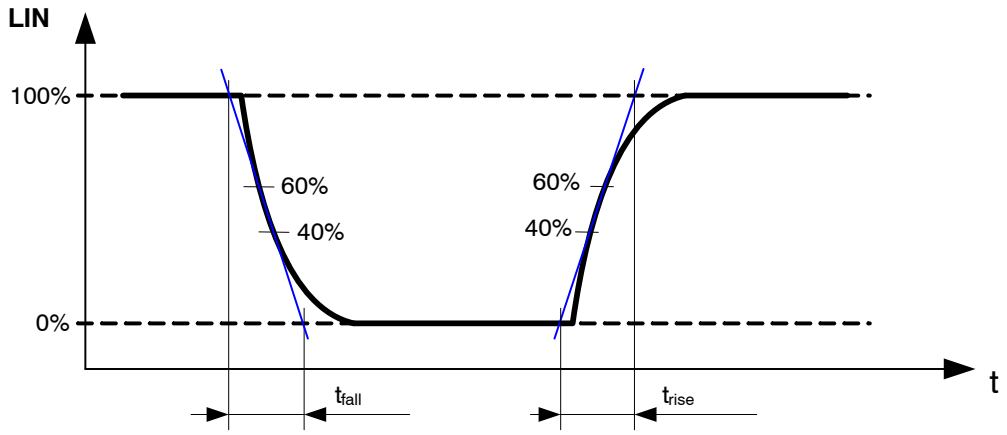


Figure 12. Definition of LIN Edge Parameters

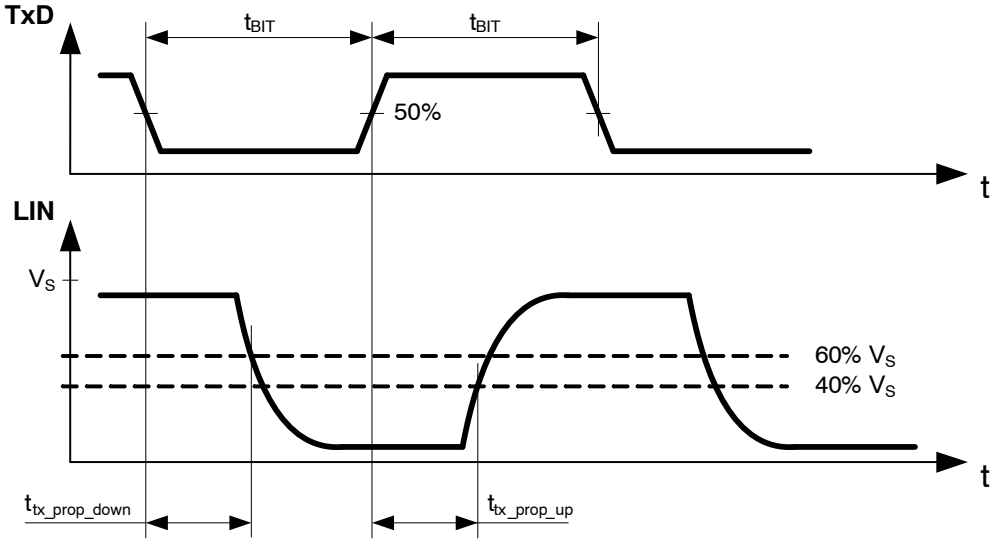


Figure 13. Definition of LIN Transmitter Timing Parameters

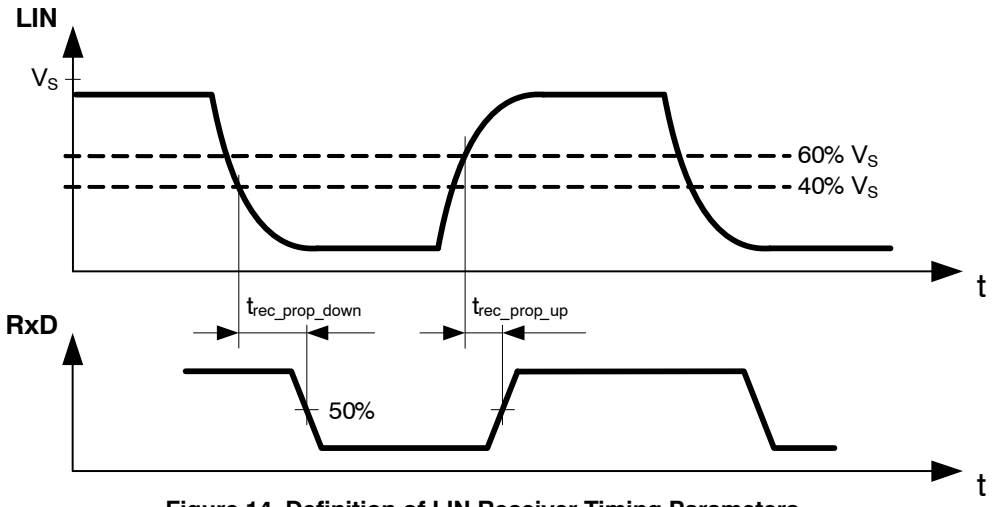


Figure 14. Definition of LIN Receiver Timing Parameters

ORDERING INFORMATION

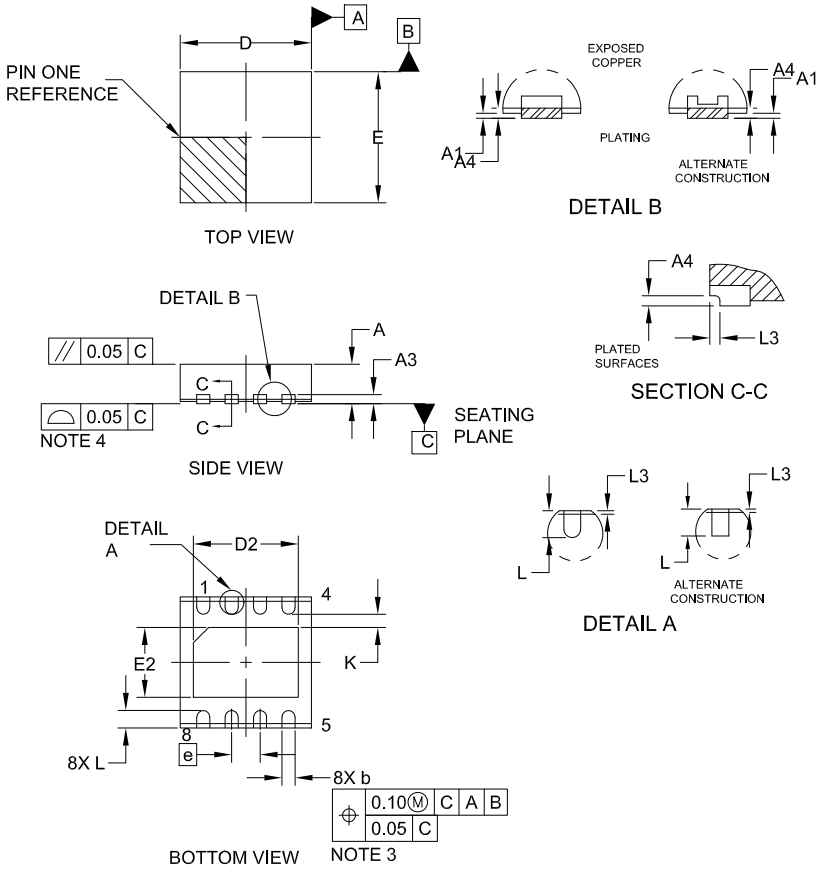
Part Number	Description	Marking	Package	Shipping †
NCV7428D15R2G	LIN transceiver with 5 V regulator	NV7428−5	SOIC−8 (Pb−Free)	3000 / Tape & Reel
NCV7428D13R2G	LIN transceiver with 3.3 V regulator	NV7428−3		
NCV7428D1L5R2G	LIN transceiver with 5 V regulator, low slope LIN	NV7428L5		
NCV7428D1L3R2G	LIN transceiver with 3.3 V regulator, low slope LIN	NV7428L3		
NCV7428MW5R2G	LIN transceiver with 5 V regulator	NV7428−5	DFNW8 Wettable Flanks (Pb−Free)	3000 / Tape & Reel
NCV7428MW3R2G	LIN transceiver with 3.3 V regulator	NV7428−3		
NCV7428MWL5R2G	LIN transceiver with 5 V regulator, low slope LIN	NV7428L5		
NCV7428MWL3R2G	LIN transceiver with 3.3 V regulator, low slope LIN	NV7428L3		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

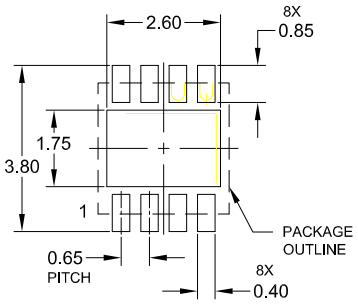
DATE 02 JUL 2021



NOTES:

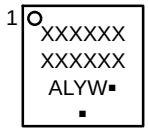
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	—	0.05
A3		0.20 REF	
A4	0.10	---	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW8 3x3, 0.65P**		**PAGE 1 OF 1**

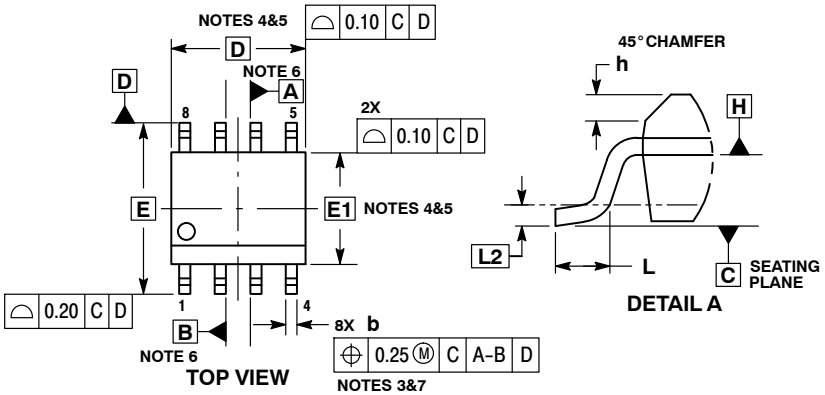
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

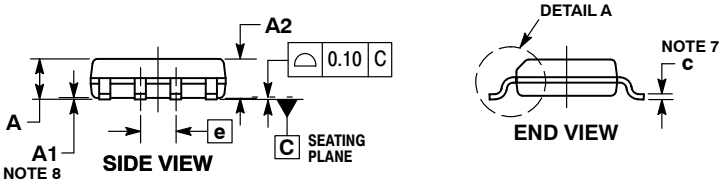
ON Semiconductor®

SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

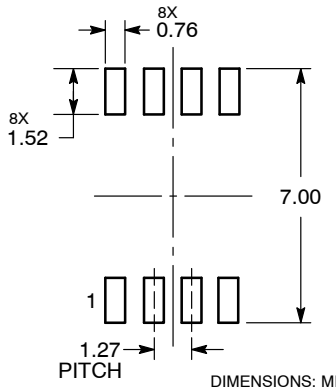




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

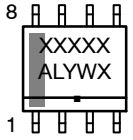
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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