Power MOSFET 120 Amps, 60 Volts N-Channel D²PAK, TO-220

Features

- Low R_{DS(on)}
- High Current Capability
- Avalanche Energy Specified
- AEC Q101 Qualified NVB5426N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Para	Symbol	Value	Unit		
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage - Continuous			V _{GS}	±20	V
Gate-to-Source Voltage - Nonrepetitive (Tp < 10 µs)			V _{GS}	30	V
Continuous Drain	Steady State			120	Α
Current R _{θJC} (Note 1)	State	T _C = 100°C		85	
Power Dissipation R _{θJC} (Note 1)	Steady State	T _C = 25°C	P _D	215	W
Pulsed Drain Current	t _p	= 10 μs	I _{DM}	260	Α
Operating and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			Is	60	Α
Single Pulse Drain-to-Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 50 V_{dc} , V_{GS} = 10 V_{dc} , $I_{L(pk)}$ = 70 A, L = 0.3 mH, R_G = 25 Ω)			E _{AS}	735	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			TL	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{ heta JC}$	0.7	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

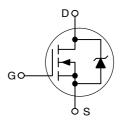


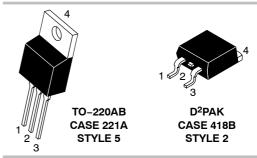
ON Semiconductor®

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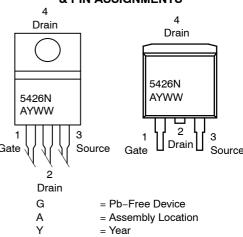
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX (Note 1)
60 V	$6.0~\text{m}\Omega$ @ $10~\text{V}$	120 A

N-Channel





MARKING DIAGRAMS & PIN ASSIGNMENTS



ORDERING INFORMATION

= Work Week

ww

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V,	I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				64		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	T _J = 25°C			1.0	μΑ
		$V_{DS} = 60 \text{ V}$	T _J = 150°C			25	1
Gate-Body Leakage Current	I _{GSS}	V _{DS} = 0 V, V	/ _{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}$	I _D = 250 μA	2.0	3.1	4.0	V
Negative Threshold Temperature Coefficient	V _{GS(th)} /T _J				9.2		mV/°C
Drain-to-Source On Voltage	V _{DS(on)}	V _{GS} = 10 \	V, I _D = 60 A		0.3	0.36	V
		V _{GS} = 10 V, I _D	= 60 A, 150°C		0.6		1
Static Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 60 A			4.9	6.0	mΩ
Forward Transconductance	9 _{FS}	V _{DS} = 15 V, I _D = 20 A			65		S
CHARGES, CAPACITANCES & GATE RESIST	ANCE					-	•
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz			5800		pF
Output Capacitance	C _{oss}				1000		
Transfer Capacitance	C _{rss}				370		1
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V,			150	170	nC
Threshold Gate Charge	Q _{G(TH)}	I _D =	60 A		6.0		1
Gate-to-Source Charge	Q _{GS}				28		
Gate-to-Drain Charge	Q_{GD}				67		
SWITCHING CHARACTERISTICS, V _{GS} = 10 V	(Note 3)				•		•
Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V,	V _{DD} = 48 V,		15		ns
Rise Time	t _r	$I_{D} = 60 A,$	$R_G = 3.0 \Omega$		100		
Turn-Off Delay Time	t _{d(off)}				105		
Fall Time	t _f				95		1
DRAIN-SOURCE DIODE CHARACTERISTICS	;						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V	T _J = 25°C		0.88	1.1	V_{dc}
		I _S = 60 A	T _J = 100°C		0.78		1
Reverse Recovery Time	t _{rr}	$I_S = 60 A_{dc}$	$V_{GS} = 0 V_{dc}$		75		ns
Charge Time	ta	dl _S /dt = 100 A/μs			50		1
Discharge Time	t _b				25		1
Reverse Recovery Stored Charge	Q _{RR}				235		μC

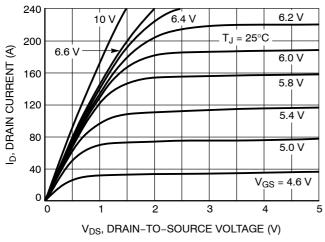
ORDERING INFORMATION

Device	Package	Shipping [†]
NTP5426N	TO-220AB (Pb-Free)	50 Units / Rail
NTB5426NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NVB5426NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



240 $V_{DS} \ge 10 \text{ V}$ 200 ID, DRAIN CURRENT (A) 160 120 T_J = 125°C 80 T_J = 25°C 40 = -55°C 0 3 5 6

V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

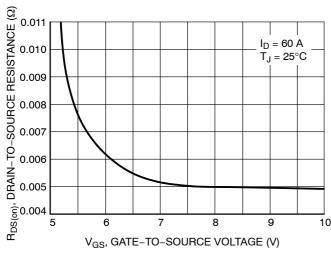


Figure 2. Transfer Characteristics

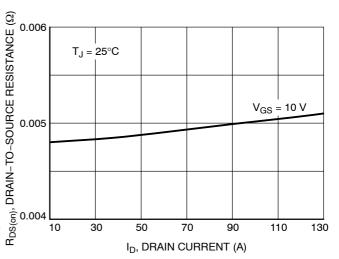


Figure 3. On-Resistance vs. Gate Voltage

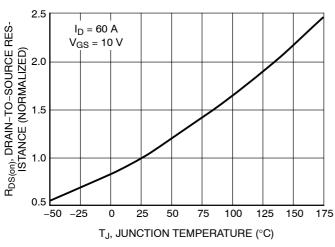


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**

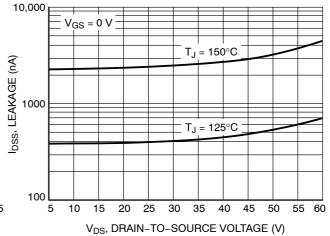


Figure 5. On-Resistance Variation with **Temperature**

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

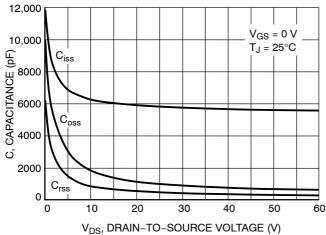


Figure 7. Capacitance Variation

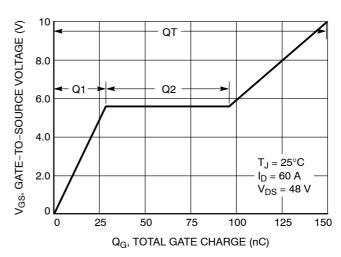


Figure 8. Gate-to-Source Voltage vs. Total Charge

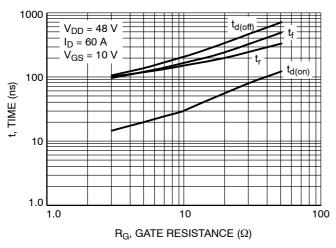


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

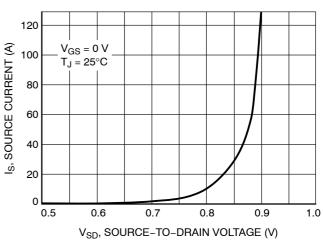


Figure 10. Diode Forward Voltage vs. Current

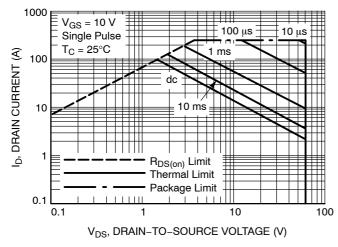


Figure 11. Maximum Rated Forward Biased Safe Operating Area

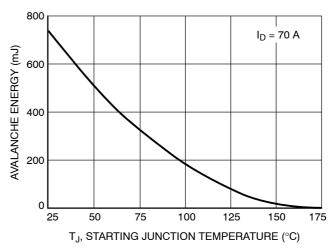


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

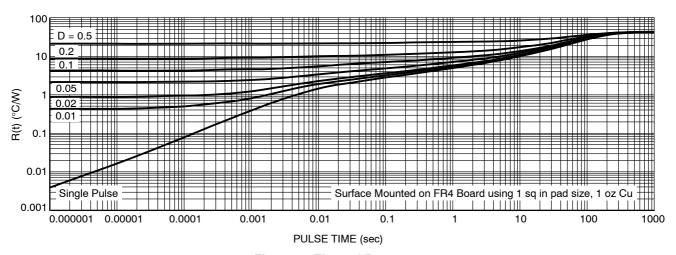


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

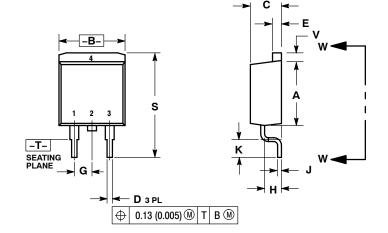




D²PAK 3 CASE 418B-04 **ISSUE L**

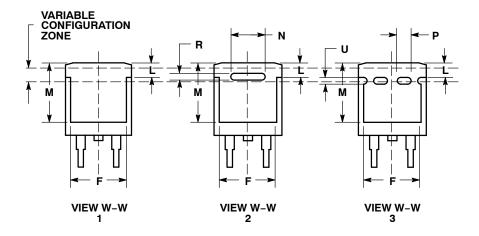
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SCALE 1:1



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
- 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

	INC	HES	MILLIMETERS		
ым	MIN			MAX	
			MIN		
Α	0.340	0.380	8.64	9.65	
В	0.380	0.405	9.65	10.29	
С	0.160	0.190	4.06	4.83	
D	0.020	0.035	0.51	0.89	
E	0.045	0.055	1.14	1.40	
F	0.310	0.350	7.87	8.89	
G	0.100 BSC		2.54 BSC		
Н	0.080	0.110	2.03	2.79	
J	0.018	0.025	0.46	0.64	
K	0.090	0.110	2.29	2.79	
L	0.052	0.072	1.32	1.83	
M	0.280	0.320	7.11	8.13	
N	0.197 REF		5.00 REF		
Р	0.079 REF		2.00 REF		
R	0.039 REF		0.99 REF		
S	0.575	0.625	14.60	15.88	
V	0.045	0.055	1.14	1.40	



STYLE 1: PIN 1. BASE 2. COLLECTOR
3. EMITTER
4. COLLECTOR STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE

STYLE 4:

PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

STYLE 6: PIN 1. NO CONNECT 2. CATHODE 3. ANODE 4. CATHODE

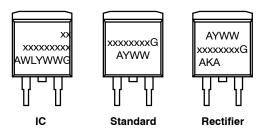
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DATE 17 FEB 2015

GENERIC MARKING DIAGRAM*



xx = Specific Device Code A = Assembly Location

 WL
 = Wafer Lot

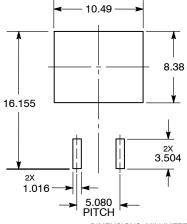
 Y
 = Year

 WW
 = Work Week

 G
 = Pb-Free Package

 AKA
 = Polarity Indicator

SOLDERING FOOTPRINT*



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^{*}This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ■", may or may not be present.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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