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Human Body Model (HBM) vs. IEC 61000-4-2

Overview

Many ESD standards such as the Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), and IEC 61000-4-2 have been developed to test for robustness and ensure ESD protection. Unfortunately, these standards are often misunderstood and sometimes used interchangeably, which can result in tested, “protected” systems that later fail in the consumer’s hands. To ensure better product reliability, it is critical that today’s design engineer understand the significant differences between manufacturing environment and system end user environment ESD testing.

While most designers are familiar with the classic device level manufacturing tests that are applied to integrated circuits, the most common misunderstanding occurs between the HBM and IEC 61000-4-2 standards. These two very different standards are designed for very different purposes. Only the more stringent IEC 61000-4-2 standard allows one to identify and correct ESD vulnerability of electronic products under real-world ESD stress conditions.

The purpose of this paper is to describe the intended purpose and basic differences of the HBM and IEC61000-4-2 standards and testing methodologies.

The Changing ESD Landscape: Increasing ESD Events, Decreasing On-Chip Protection

Three important changes have contributed to the increased ESD vulnerability of today’s electronic devices:

- **Smaller Manufacturing Geometries** - as manufacturing geometries for today's most advanced ICs decrease to 90 nm and less, the voltage and current levels that can cause ESD related failures for these devices also decrease. ESD damage can occur due to excessive voltage, high current levels, or a combination of both. High voltages can cause gate oxide punch-through, while excessive I^2R levels can cause junction failures and metallization traces to melt. As manufacturing geometries decrease, the voltage and current levels that can cause these failures also decrease. This has made it difficult to provide even relatively low levels of on-chip ESD protection.
- **A Reduction in On-Chip Protection** - increased susceptibility to ESD damage has been widely publicized as the Industry Council on ESD Target Specifications recently announced a move to reduce the standard level of on-chip ESD protection, making external ESD protection circuits even more critical for adequate system reliability. The focus of the Industry Council’s efforts is to reduce the level of on-chip ESD protection, primarily aimed at providing adequate levels of ESD protection for manufacturing environments. They are not suggesting reducing system level ESD protection, which they suggest must remain at existing levels.
- **The Changing Application Environment** – the proliferation of laptops, cell phones, MP3 players, digital cameras, and other hand-held mobile devices, used in uncontrolled environments (i.e., no wrist-grounding straps or conductive and grounded table surfaces). In these environments, people touch I/O connector pins while connecting and disconnecting cables. Devices are subjected to constant ESD stress as users plug cameras, games, and other devices into their USB and video ports. A portable device can also build up a charge during normal usage and discharge that energy when connected to another device, such as a computer or a TV. The simple act of walking across a synthetic carpet and touching an exposed port on the outside of a digital TV can result in an ESD discharge greater than 35 kV. ESD discharges can occur directly at the port, or they can be discharged through a cable. This scenario is particularly dangerous to electronics equipment because the entire charge bypasses the connector’s ground shield (if it has one) and is discharged directly into the system’s electrical circuits.

Table 1: Static Voltage Generation Examples (Source: ESD Association)

Examples of Static Voltage Generation At Different Levels of Relative Humidity (RH)		
Means of Generation	10-25% RH	65-90% RH
Walking across carpet	35,000 V	1,500 V
Walking across vinyl tile	12,000 V	250 V
Worker at bench	6,000 V	100 V
Poly bag picked up from bench	20,000 V	1,200 V
Chair with urethane foam	18,000 V	1,500 V

ESD Standards in the Manufacturing Environment

ICs are inherently susceptible to ESD damage. This damage can occur during the process of assembling the ICs into boards and finished systems, packaging, or in the field. There are several current methods for rating ICs for ESD in the manufacturing environment. The most common include:

- **HBM** - this standard is intended to simulate a person becoming charged and discharging from a bare finger to ground through the circuit under test.
- **MM** - intended to simulate a charged manufacturing machine, discharging through the device to ground.
- **CDM** - simulates an integrated circuit becoming charged and discharging to a grounded metal surface.

The purpose of traditional ESD testing of integrated circuits in the manufacturing environment is very different than system level testing. HBM, MM and CDM tests are intended to ensure that integrated circuits survive the manufacturing process. Generally, manufacturers design in only enough protection for their device to survive being assembled into a finished system.

Processes such as packaging, final testing, shipment to a board assembly facility, placement on the circuit board, and the soldering process are performed in controlled ESD environments that limits the level of ESD stress to which the device is exposed. In the manufacturing environment, ICs are only specified to survive 2 kV HBM, although some have been specified as high as 8 kV, while others - particularly newer parts in very small geometry processes - can be 500 V or less.

While HBM is usually sufficient for the controlled ESD environment of the factory floor, it is completely inadequate for system level testing. The levels of ESD strikes, both the voltages and the currents, can be much greater in the end user environment. For this reason, the industry uses a different testing standard for system level ESD testing. This standard is known as the IEC 61000-4-2.

IEC 61000-4-2: The ESD Standard for System Level Testing

The IEC standard is a system level test that replicates a charged person discharging to a system in a system end user environment. The purpose of the system level test is to ensure that finished products can survive normal operation and it is generally assumed that the user of the product will not take any ESD precautions to lower ESD stress to the product.

The IEC 61000-4-2 standard defines four standard levels of ESD protection, using two different testing methodologies. Contact discharge involves discharging an ESD pulse directly from the ESD test gun that is touching the device under test. This is the preferred method of testing. However, the standard provides for an alternate test methodology known as air discharge for cases where contact discharge testing is not possible. In the air discharge test, the ESD test gun is brought close to the device under test until a discharge occurs. The standards are defined so that each level is considered equivalent – a Level 4 contact discharge of 8 kV is considered equivalent to a 15 kV air discharge.

Table 2. IEC 61000-4-2 Test Levels

Contact Discharge		Air Discharge	
Level	Test Voltage kV	Level	Test Voltage kV
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X ^{Note 1}	Special	X ^{Note 1}	Special

Notes

1. "X" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those are specified, special test equipment may be required.

HBM versus IEC 61000-4-2

There are several differences between the HBM and IEC 61000-4-2 standard that are immediately obvious. The most important differences are as follows:

- the amount of current and I^2R power released during a voltage strike
- the rise time of the voltage strike
- the number of voltage strikes repeated in the tests

The Amount of Current and I^2R Power Released During a Voltage Strike

A key difference between these two standards is the peak current level associated with a strike. As shown in Table 3, the peak current discharged during an 8 kV HBM strike is less than the peak current discharged during a 2 kV IEC 61000-4-2 strike and, at 8 kV (a common system level ESD requirement), the peak current for an IEC 61000-4-2 strike is over 22 times higher than what most high performance semiconductors are designed to withstand.

Table 3. Peak current of HBM vs. IEC 61000-4-2 ESD Standards

Applied Voltage (kV)	Peak Current (A) Human Body Model	Peak Current (A) IEC 61000-4-2
2	1.33	7.5
4	2.67	15.0
6	4.00	22.5
8	5.33	30.0
10	6.67	37.5

The difference in current is critical to whether the ASIC will survive the ESD strike. Because high current levels can cause junction failures and metallization traces to melt, it is possible that a chip protected to 8 kV HBM can be destroyed by a 2 kV IEC 61000-4-2 strike. For this reason, it is crucial that system design engineers do not rely on HBM ratings to determine whether a system will survive an ESD strike after it is shipped to end customers.

Rise time of the voltage strike

Another key difference between these standards is the rise time of the voltage strike. The HBM model specifies a rise time of 25 ns. An IEC pulse has a rise time of less than 1 ns and dissipates most of its energy in the first 30 ns. If it takes 25 ns to respond, the device rated using the HBM specification can be destroyed before its protection circuits are even activated (see Figure 1).

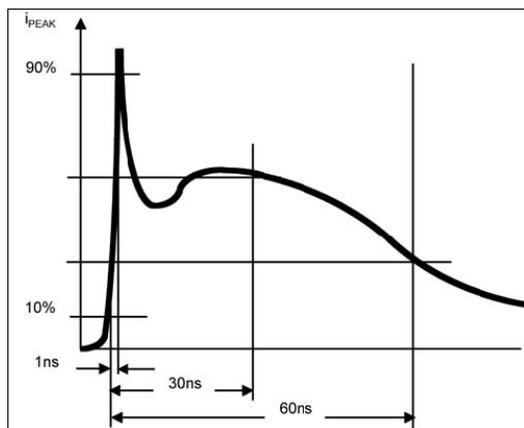


Figure 1. IEC 61000-4-2 ESD Pulse Waveform

This example demonstrates that a protection circuit designed to withstand an HBM pulse may not even turn on before the “protected” chip is destroyed in an IEC 61000-4-2 pulse.

The Number of Voltage Strikes Repeated

Another difference between the HBM and IEC standards is the number of strikes used during testing. The HBM standard requires only a single positive and single negative strike to be tested, whereas the IEC 61000-4-2 test requires 3 positive strikes and 3 negative strikes. It is possible for a device to survive the first strike, but fail on subsequent strikes due to damage sustained during the initial strike. In today’s application environment, systems can be subject to many strikes over their lifetimes, and it is becoming more common for system vendors to test their systems with even more strikes than the minimum of three that are specified in the IEC 61000-4-2 standard.

Beware of Misleading Marketing Specifications

Some semiconductor vendors are now increasing their “integrated ESD” ratings and potentially confusing system designers. Some of these vendors have even dropped saying which standard was used to test their devices, in an effort to mislead customers, implying that their integrated ESD protection eliminates the need for external ESD devices.

It is critical for a system designer to check which standard was used to rate the ESD level of a device. If a device has been tested to the IEC 61000-4-2 standard, it will say so. Devices that do not state the testing standard used, have usually been tested using the HBM or other non-IEC 61000-4-2 standards, and should not be considered to have adequate ESD protection integrated. For example, ON Semiconductor recently tested an HDMI switch from a vendor prominently marketing that they integrated 8 kV of ESD protection. When tested, this device failed and was destroyed by a 6 kV IEC 61000-4-2 standard discharge test.

If the system designer is not aware of this potentially misleading marketing tactic, it can cause costly program slips and redesigns.

Summary

System designers need to be familiar with the differences between various ESD test standards. The ratings that are used for protecting ICs in the manufacturing environment such as HBM and CDM are not equivalent to system level ESD tests such as the IEC 61000-4-2. Each standard has a legitimate purpose, but misapplying these standards can result in design delays and/or product returns. For system level ESD ratings, always use the IEC 61000-4-2 standard.

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