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Demonstration Note for CS5101

Multiple Output, Telecommunications Power Supply with Secondary Side Control for Tight Output Regulation

DEMONSTRATION NOTE

INTRODUCTION

The CS5101 demonstration board is a multiple-output (5.0 V @ 7.0 A; 3.3 V @ 5.0 A), isolated, 50 W power supply that accepts the standard telecommunications input voltage range: 36 V to 72 V. The 3.3 V auxiliary output uses the CS5101, a secondary side post regulator (SSPR) to provide a tightly regulated output over full load to no load conditions.

In this demonstration board, the main output is controlled by the CS3843 current mode PWM controller. The CS5101 regulates the 3.3 V secondary output by adjusting the duty cycle of the auxiliary switch using leading edge modulation. This auxiliary output voltage is independently controlled by a local feedback loop. This method of regulation is similar to that of a magnetic amplifier, however, the CS5101 offers several distinct advantages.

Features

- High Efficiency
- Soft Switching of Auxiliary FET
- Programmable Overcurrent Protection
- Easy and Accurate Overcurrent Protection
- Tight Regulation Over Full Load/Line Range
- Lossless Shut-Down Feature

Table 1. Suggested Equipment for CS5101 Demonstration Board

Description	Specifications
Power Supply	36 V–72 V, 2.0 A Output
Oscilloscope	100 MHz, 2-Channel
Multi Meters	At least two required
Load	Electronic load or power resistors

USING THE CS5101 DEMONSTRATION BOARD

The bench power supply is connected to the input voltage terminals, shown as V_{IN} and PGND in Figure 1. A load is applied to the the output voltage terminals, shown as 5.0 V, 3.3 V and SGND in Figure 1. The loads should be set within the parameters specified in Table 2.

Five test points TP1 through TP5 have been brought out so that waveforms at critical nodes can be easily viewed (see Figure 1). (Please note: when monitoring secondary side waveforms, the ground lead on the oscilloscope AC plug should not be connected to earth ground.)

TP1 is located at the drain of the primary-side FET. A typical waveform at TP1 is shown in Figure 2a. When measuring this point, reference the scope ground to the primary side ground (PGND).

Table 2. Demonstration Board Specifications

Parameter	Description	Specification
V_{IN}	Input voltage range.	36 V to 72 V
V_{OUT1}	Main output voltage.	5.0 V \pm 3.0%
V_{OUT2}	Auxiliary output voltage.	3.3 V \pm 2.0%
I_{OUT1}	Main output current.	1.5 A–7.0 A
I_{OUT2}	Auxiliary output current.	0 A–5.0 A
Isolation	Primary to secondary isolation (min).	500 V
P_{OUT}	Total output power (max).	50 W
	Output power without airflow (max).	40 W
I_{CL}	Current limit threshold (V_{OUT}).	9.0 A
I_{SC}	Short circuit current (V_{OUT2}).	4.4 A

CS5101DEMO/D

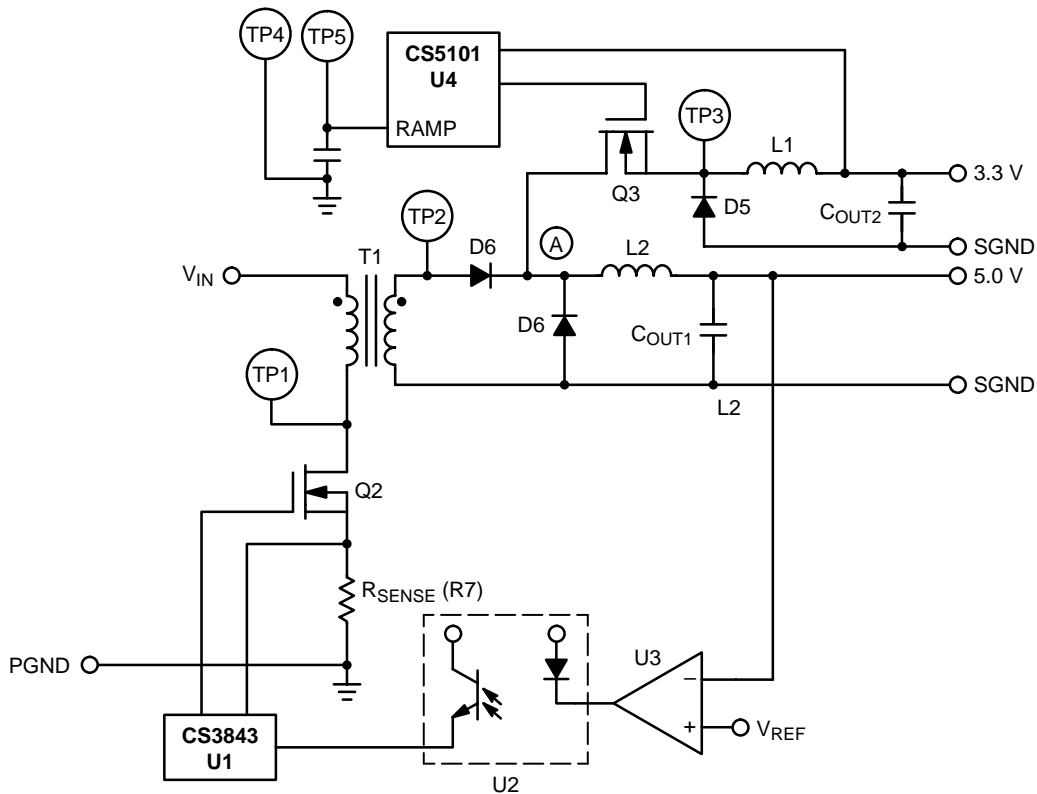


Figure 1. Simplified CS5101 Demonstration Board Schematic

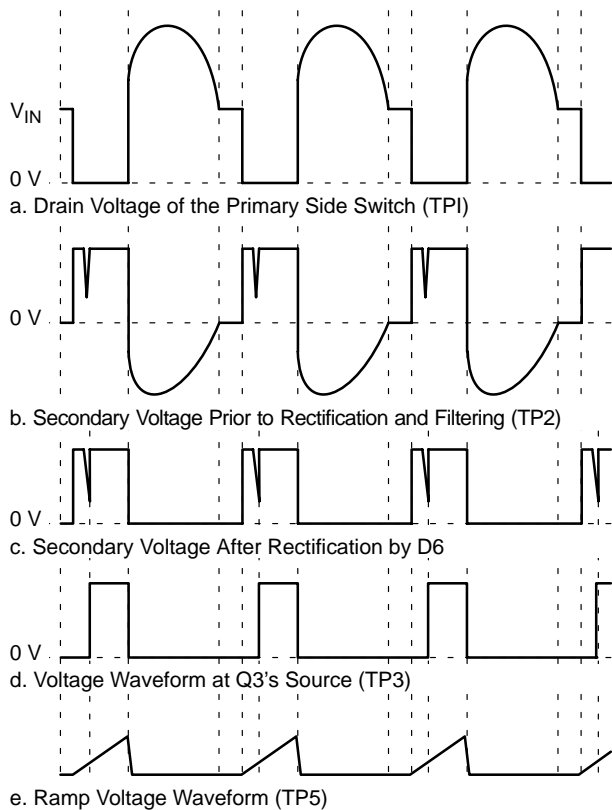


Figure 2. Demonstration Board Test Point Waveforms Under Full Load Conditions

TP2 is located at the top side of the secondary winding. This voltage is similar to TP1, but is scaled down three to one, based on the transformer turns ratio. This waveform is illustrated in Figure 2b. The notch during the on-time portion of the waveform is generated when the CS5101 turns on Q3 and is caused by the transformer leakage inductance, which appears in series with the secondary winding.

TP3 is located at the source of the FET (Q3). The on-time of Q3 is reduced compared to TP2, as shown in Figure 2d. The leading edge of this waveform is in sync with the notch at TP2. The leading edge modulation scheme used in the CS5101 causes a delay in Q3 turn-on to maintain regulation on the 3.3 V output.

TP5 is located at the ramp node used to control the CS5101, which is shown in Figure 2e. When measuring at this point, connect the scope probe ground to TP4.

THEORY OF OPERATION

The main output of this 50 W power supply is 5.0 V at 7.0 A. This output is generated using a forward topology DC to DC converter, which operates using peak current mode control. Primary side regulation is accomplished with the industry standard CS3843. The auxiliary output supplies 3.3 V at 5.0 A. It is regulated by the CS5101, which uses leading edge modulation to control the on-time of Q3.

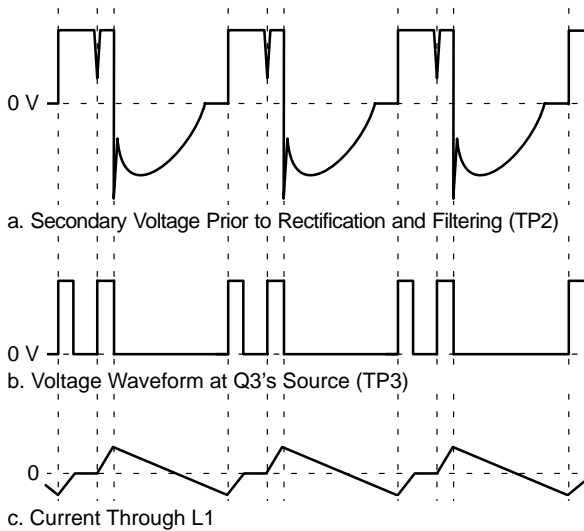


Figure 3. Demonstration Board Test Point Waveforms Under No Load Condition on the 3.3 V Output

Primary Side Control

The error amplifier (U3) feeds the output voltage back to the CS3843 controller through the opto-isolator (U2). The voltage on the secondary side of the transformer, at test point TP2, is rectified by a Schottky pair (D6) and averaged by an LC filter (L2 and C_{OUT1}), to create the main output (Figure 3).

Secondary Side Control

The rectified voltage at the cathode of D6 (Figure 1) is applied to the FET (Q3). Since the average of this rectified waveform is 5.0 V, the CS5101 must reduce the duty cycle of Q3, which is applied to the auxiliary output filter comprised of L1 and C_{OUT2}. This is done by delaying the turn-on of Q3 relative to the rising edge of the waveform shown in Figure 2c. This waveform represents point A in Figure 1.

During the off-time of Q3, its body diode prevents the current through L1 from becoming discontinuous. As the current through L1 decays through zero, the body diode of Q3 conducts negative current. When the voltage at the drain of Q3 rises, it immediately causes the source of Q3 to track. The source will remain elevated until the current in L1 reaches zero, as shown in Figure 3b. The CS5101 controls the width of the second pulse, shown in Figure 3b, to maintain regulation.

Lossless Current Limit

Current limit is implemented without using a current sense resistor. The inductor's DC resistance is used instead (Figure 4). The average voltage across the inductor is determined by the product of its DC resistance and the DC current through the coil. A low-pass filter averages the AC voltage at the switching node. This voltage is compared to the output voltage, which is fed to the CS5101 through R16.

The current limit threshold is set by the offsets of R17 and R15. Under normal operating conditions, the current limit is invoked when the DC voltage drop across the coil equals the sum of these two offsets. Under a short circuit condition, the output current will fold-back, since the offset associated with R17 is negligible and the offset created by R15 remains.

The current limit set-point is determined by:

$$I_{LIM} = \frac{V_{OFFSET}}{R_{L1}}$$

where V_{OFFSET} is the DC offset voltage at the input of the current sense amplifier and R_{L1} is the DC resistance of the coil L1. On the demonstration board, the inductor DC resistance is about 7.0 mΩ

The fold-back value is determined by:

$$I_{FOLD} = \frac{V_{OFFSET}}{R_{L1}} = \frac{\left(\frac{V_{REF} \times R_{16}}{R_{15} + R_{16}}\right)}{R_{L1}} = \frac{\left(\frac{5.0 \text{ V} \times 6.2 \text{ k}\Omega}{1000 \text{ k}\Omega + 6.2 \text{ k}\Omega}\right)}{7.0 \text{ m}\Omega} = 4.4 \text{ A}$$

where V_{REF} is the reference provided from the CS5101.

The output current limit set point is determined by:

$$I_{LIM} = \frac{V_{OFFSET}}{R_{L1}} = \frac{\left(\frac{V_{REF} \times R_{16}}{R_{15} + R_{16}} + \frac{V_{OUT2} \times R_{15}}{R_{15} + R_{16}} - \frac{V_{OUT2} \times R_{17}}{R_{17} + R_{18} + R_{19}}\right)}{R_{L1}} = \frac{\left(\frac{5.0 \text{ V} \times 6.2 \text{ k}\Omega}{1.0 \text{ M}\Omega + 6.2 \text{ k}\Omega} + \frac{3.3 \text{ V} \times 1.0 \text{ M}\Omega}{1.0 \text{ M}\Omega + 6.2 \text{ k}\Omega} - \frac{3.3 \text{ V} \times 390 \text{ k}\Omega}{390 \text{ k}\Omega + 3.0 \text{ k}\Omega + 3.3 \text{ k}\Omega}\right)}{7.0 \text{ m}\Omega} = 9.0 \text{ A}$$

Output current limit for this circuit is set at 9.0 A to guarantee specified maximum output current over the variation of DC resistance in L1.

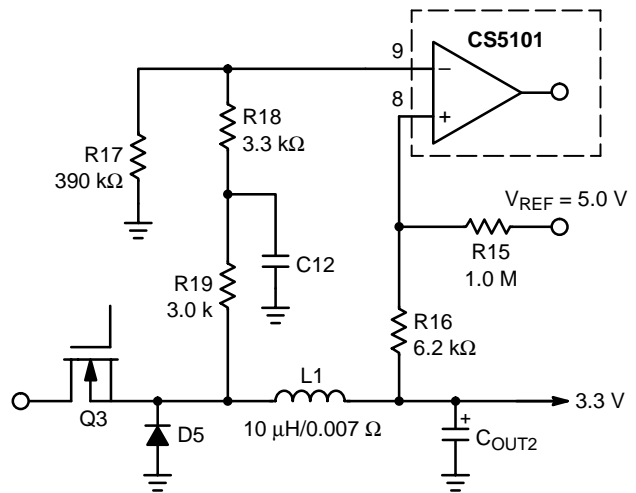


Figure 4. Lossless Current Limit Circuit

Efficiency Considerations

The conversion efficiency for the secondary output in this design is calculated below. The slight loss in efficiency is primarily in the flyback diode (D5).

Power loss in the FET (Q3) occurs during conduction, since the CS5101 ensures lossless turn-off and turn-on. This FET loss is:

$$\begin{aligned} P_{Q3} &= R_{DS(on)} \times I^2 \times DC \\ &= 0.04 \Omega \times 25 A^2 \times 20\% = 0.2 W \end{aligned}$$

where DC is duty cycle which is about 20% for a 3.3 V output and 48 V input.

Power loss in the CS5101 depends on quiescent current, gate drive current, and V_{CC} .

$$\begin{aligned} P_{Q4} &= (I_Q + I_{DR}) \times V_{CC} \\ &= (I_Q + Q_{TOT} \times f_{SW}) \times V_{CC} \\ &= (12 \text{ mA} + 30 \text{ nC} \times 160 \text{ kHz}) \times 18 \text{ V} = 0.302 \text{ W} \end{aligned}$$

Loss in the diode is:

$$\begin{aligned} P_{D5} &= V_F \times I_{OUT} \times (1 - DC) \\ &= 0.55 \text{ V} \times 5.0 \text{ A} \times (100 - 20)\% = 2.2 \text{ W} \end{aligned}$$

Loss in the inductor consists of conduction loss and core loss. Inductor core loss is estimated from data supplied by core vendor.

$$\begin{aligned} P_{L1} &= P_{CORE} + I_{OUT}^2 \times R_{LDC} \\ &= 0.125 \text{ W} + 25 A^2 \times 7.0 \text{ m}\Omega = 0.3 \text{ W} \end{aligned}$$

Total power loss and efficiency, for the 3.3V output, are determined as follows:

$$\begin{aligned} P_T &= P_{Q3} + P_{Q4} + P_D + P_{L1} \\ &= 0.2 \text{ W} + 0.3 \text{ W} + 2.2 \text{ W} + 0.3 \text{ W} = 3.0 \text{ W} \end{aligned}$$

$$\eta = \frac{P_{OUT}}{P_T + P_{OUT}} = \frac{16.5 \text{ W}}{3.0 \text{ W} + 16.5 \text{ W}} = 84.6\%$$

Compensating the CS5101

There are two control loops used in the demonstration circuit. The 5.0 V output is regulated by the TL431 error amplifier (U3) and its associated feedback components. Compensation of this amplifier is handled using a simple RC network (R23 and C18), which is common in current mode control.

The 3.3 V output is controlled by the error amplifier in the CS5101. This amplifier is compensated with a dual pole-zero RC network (R13, C10, C11 and R22, C17), which is common in voltage mode control. The crossover frequency of the CS5101 controller is 5 to 10 times lower than the main loop to ensure proper interaction between the two control loops. The current limit circuit is compensated

with a single pole. It has a lower crossover frequency than the CS5101 voltage feedback loop.

Selection of the compensation components is described in detail in the application note "Secondary Side Post Regulator," document number CS5101AN/D, available through the Literature Distribution Center or via our website at <http://www.onsemi.com>.

CONSIDERATION FOR CRITICAL COMPONENTS IN THIS DESIGN

Magnetics

An un-gapped transformer was chosen to provide maximum primary inductance. The turns ratio was selected so that the duty cycle at low line (36 V) does not exceed 50%. The circuit uses a resonant reset technique, which eliminates the need for an auxiliary catch winding. A single secondary winding generates both the 5.0 V and 3.3 V outputs.

Input Capacitors

Input capacitors are chosen to support maximum ripple current. A 100 V rating for the capacitors was chosen to ensure reliable operation at maximum input voltage (72 V).

Output Capacitors

Output capacitors were selected based primarily on the output ripple voltage specification. Output ripple is determined by the effective series resistance (ESR) of the output capacitors.

FETs

The MOSFET selection is based on a sufficient voltage rating of 200V for Q2 and 55V for Q3. Because Q3 has a low $R_{DS(on)}$ and switches with very low transient loss it does not require a heat sink.

Schottky Diodes

Schottky diodes D5 and D6 are selected for the maximum current and voltage of the circuit. In this design they support 50 V (max) spikes. The snubber circuit formed by R29/C35 reduces these voltage spikes.

Output Chokes

The output chokes were selected to support full output load current with a 30°C temperature rise and to minimize output voltage ripple.

CS5101 Voltage Limiting

The maximum voltage on the CS5101's V_{CC} input is limited to 19 V by D4. This limits the maximum gate to source voltage for Q3 to less than 20 V.

The complete demonstration board schematic is shown in Figure 5, and the Bill of Materials, with part numbers, vendors and contact numbers is contained in Table 3.

CS5101DEMO/D

Table 3. Bill of Materials for the CS5101 Demonstration Board

Qty	Ref Des	Description	Manufacturer	Part Number	Phone	Fax
3	C1, C2, C3	47 μ F, 100 V	Nichicon	UPR2A470MPH	(708) 843-7500	(708) 843-2798
6	C7, C12, C14, C16, C18, C31, C32	0.1 μ F	Panasonic	ECU-S1J104MEA	-	-
1	C4	4700 pF	Panasonic	ECU-S1J472KBA	-	-
2	C11, C36	0.01 μ F	Panasonic	ECU-S1J103KBA	-	-
2	C5, C35	150 pF	Panasonic	ECU-S2A151JCA	-	-
1	C8	68 F	Panasonic	ECU-S2A680JCA	-	-
1	C9	330 pF	Panasonic	ECU-S2A331JCB	-	-
2	C10, C15	0.47 μ F	Panasonic	ECU-S1J474MEB	-	-
2	C13, C17	0.22 μ F	Panasonic	ECU-S1J224MEA	-	-
6	C19-C24	680 μ F/16 V	Nichicon	UPY1C681MPH	(708) 843-7500	(708) 843-2798
1	C33	47 μ F/35 V	Nichicon	UPL1V470MEH	(708) 843-7500	(708) 843-2798
1	C34	1000 pF/200 V	Panasonic	ECQ82102JF	-	-
2	R1, R3	22 k	KOA Speer Electronics	CF-1/4-223-J	(814) 382-5538	(814) 382-8883
1	R2	2.0 k	KOA Speer Electronics	CF-1/4-202-J	(814) 382-5538	(814) 382-8883
1	R4	5.1 Ω	KOA Speer Electronics	CF-1/4-5R1-J	(814) 382-5538	(814) 382-8883
2	R5, R29	100 Ω	KOA Speer Electronics	CF-1/4-101-J	(814) 382-5538	(814) 382-8883
1	R10	33 Ω	KOA Speer Electronics	CF-1/4-330-J	(814) 382-5538	(814) 382-8883
2	R6, R7	0.2 Ω /1.0 W	KOA Speer Electronics	RSS-1-0R2-J	(814) 382-5538	(814) 382-8883
2	R8, R11	5.1 k	KOA Speer Electronics	CF-1/4-512-J	(814) 382-5538	(814) 382-8883
1	R9	510 Ω	KOA Speer Electronics	CF-1/4-511-J	(814) 382-5538	(814) 382-8883
3	R12, R16, R23	6.2 k	KOA Speer Electronics	CF-1/4-622-J	(814) 382-5538	(814) 382-8883
1	R13	300 Ω	KOA Speer Electronics	CF-1/4-301-J	(814) 382-5538	(814) 382-8883
2	R15, R28	1.0 M	KOA Speer Electronics	CS-1/4-105-J	(814) 382-5538	(814) 382-8883
1	R18	3.0 k	KOA Speer Electronics	CF-1/4-302-J	(814) 382-5538	(814) 382-8883
1	R19	3.3 k	KOA Speer Electronics	CF-1/4-332-J	(814) 382-5538	(814) 382-8883
1	R17	380 k	KOA Speer Electronics	CF-1/4-393-J	(814) 382-5538	(814) 382-8883
1	R20	1.3 k, 1.0%	KOA Speer Electronics	MF-55-0-1301-F	(814) 382-5538	(814) 382-8883
9	R12, R24, R25	2.0 k, 1.0%	KOA Speer Electronics	MF-55-0-2001-F	(814) 382-5538	(814) 382-8883
1	R22	200 Ω	KOA Speer Electronics	CF-1/4-201-J	(814) 382-5538	(814) 382-8883
1	R26	10 k	KOA Speer Electronics	CF-1/4-103-J	(814) 382-5538	(814) 382-8883
1	R27	18 Ω	KOA Speer Electronics	CF-1/4-180-J	(814) 382-5538	(814) 382-8883
1	U1	PWM	ON Semiconductor	CS3843AN8	(401) 885-3600	(401) 885-5786
1	U2	Opto-isolator	Motorola	MOC8102	-	-
1	U3	Reference	National Semiconductor	LM431ACZ	-	-
1	U4	SSPR	ON Semiconductor	CS5101N14	(401) 885-3600	(401) 885-5786
1	D1	15 Zener	Central Semiconductor	1N5245	(516) 435-1110	(516) 435-1824
2	D2, D3	Diode	Central Semiconductor	1N4148	(516) 435-1110	(516) 435-1824
1	D1	19 V Zener	Central Semiconductor	1N5249	(516) 435-1110	(516) 435-1824
1	D5	8.0 A/80 V Schottky	International Rectifier	8TQ080	(310) 322-2331	(310) 232-3332
1	D6	16 A/60 V Schottky	International Rectifier	30CTQ080	(310) 322-2331	(310) 232-3332
1	Q1	NPN, 100 V, 1.0 A	Central Semiconductor	TIP29C	(516) 435-1110	(516) 435-1824

CS5101DEMO/D

Table 3. Bill of Materials for the CS5101 Demonstration Board

Qty	Ref Des	Description	Manufacturer	Part Number	Phone	Fax
1	Q2	NMOS, 200 V	International Rectifier	IRF640	(310) 322-2331	(310) 232-3332
1	Q3	NMOS, 55 V	International Rectifier	IRFZ34N	(310) 322-2331	(310) 232-3332
1	L1	10 μ H/5.0 A	Allied Components Int.	CS226	(714) 630-3713	(714) 630-3562
1	L2	10 μ H/ 7.0 A	Allied Components Int.	CS227	(714) 630-3713	(714) 630-3562
1	T1	Power Xformer	Gauss Transformer	GSPT-30EPC-H005	(714) 522-6889	(714) 522-7335
6	J1-J6	Turret Terminal	Millmax	2501-1-00-44-00-00-07-0	-	-
2	H1	Clip-On Heat Sink	Aavid Engineering	576802804000	(603) 528-3400	(603) 528-1478
1	H2	1" Heat Sink	Aavid Engineering	613002802500	(603) 528-3400	(603) 528-1478

CS5101DEMO/D

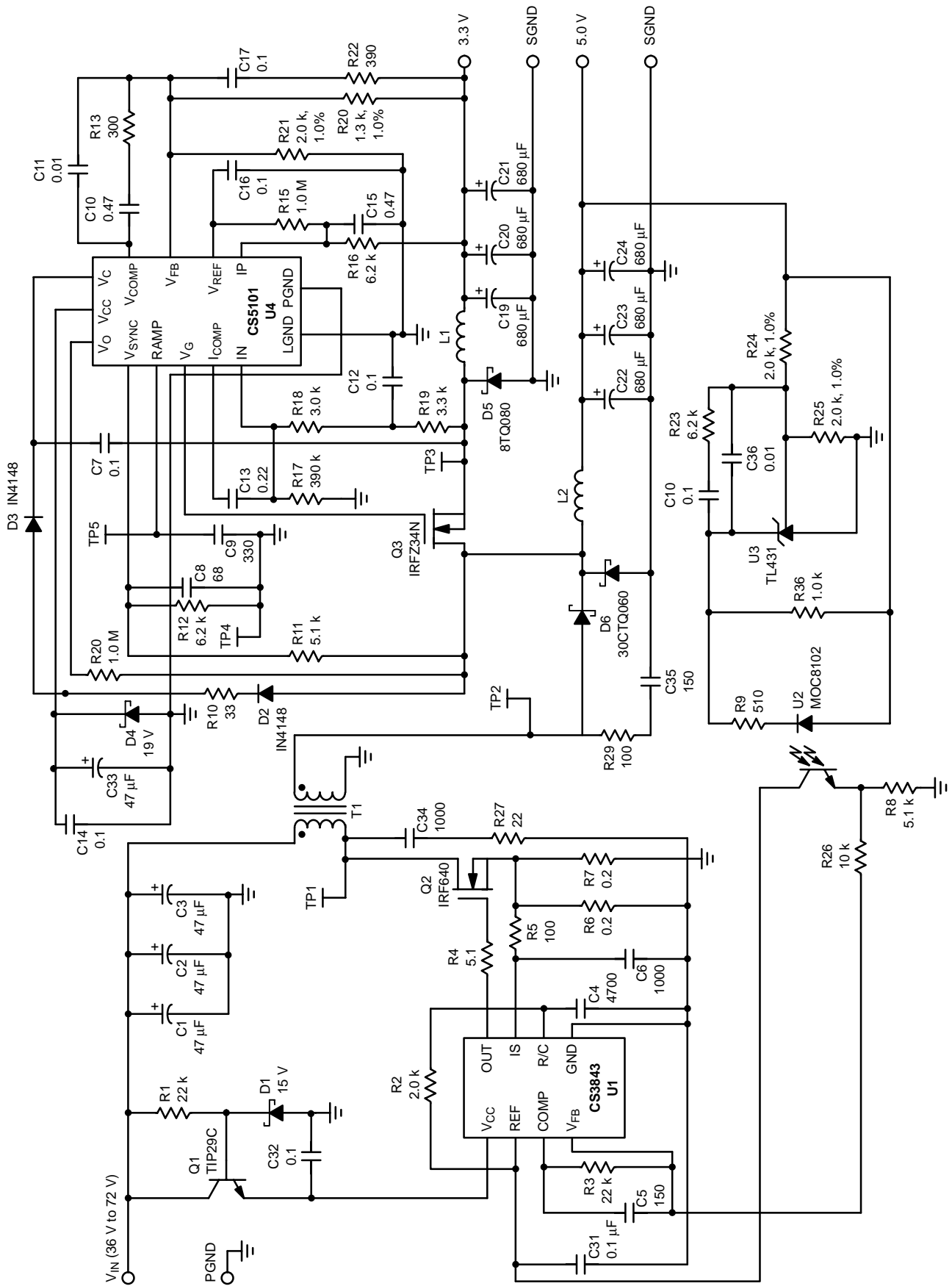



Figure 5. Demonstration Board Schematic

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