



ON Semiconductor®

Introducing XPressArray-II

**The Industry's First 0.15 μm Structured ASIC
Focusing on FPGA Conversions**

Disclaimer: ON Semiconductor is providing this reference design documentation package “AS IS” and the recipient assumes all risk associated with the use and/or commercialization of this design package. No licenses to ON Semiconductor’s or any third party’s Intellectual Property is conveyed by the transfer of this documentation. This reference design documentation package is provided only to assist the customers in evaluation and feasibility assessment of the reference design. It is expected that users may make further refinements to meet specific performance goals.

Introducing XPressArray®-II

The Industry's First 0.15 μm Structured ASIC Focusing on FPGA
Conversions



Overview

More often than not, programmable logic devices represent a significant portion of the cost of new electronic products. Hitting the market window is extremely critical to the success of a product, which is one reason system designers turn to programmable logic devices such as FPGAs. However, taking a product to market with an expensive FPGA may put an end to the product before it has a chance to succeed. As a result, the debate over FPGA versus ASIC implementation has been magnified and has taken center stage for companies in need of cost effective, long-term solutions for their products. The challenge for these companies is in identifying a chip solution that minimizes risk, time-to-market, and cost.

The technological advancements in shrinking process geometries along with a focus on system-on-chip (SoC) applications by most ASIC suppliers have created a significant gap between high density ASICs and high-cost, low-density FPGAs. Companies are forced to choose between two inadequate solutions. One choice is to remain with expensive FPGAs, but the resulting competitive pressures and lower margins make this an ineffective choice for many applications. The second choice is to convert to an ASIC. However, the costs to convert to a standard cell ASIC have become extremely difficult to justify for many mid-density, medium volume applications. Nonrecurring engineering (NRE) costs for converting to a cell-based or standard cell ASIC typically fall in the \$400K to \$1.0M range. These excessive NREs are being driven by reticle costs that are growing exponentially with smaller process geometries. The expensive tooling has pushed out the conversion break-even volumes to 50,000 units annually or more for many products with business models predicated on a low-cost conversion solution.

ASIC vendors have introduced structured ASICs in order to bridge the gap between FPGAs and standard cell ASICs for mid-density applications. Their lower NREs and quicker turn-around times make them an attractive alternative. However, most of the structured ASICs available are targeted towards standard cell replacement rather than FPGA conversions.

The Solution

The evolutionary XPressArray-II structured ASIC continues the trend of the revolutionary XPressArray family as the preferred solution to fill the market gap between high density FPGAs and standard cell ASICs. This innovative, next-generation technology platform is the answer to cost-reduction questions that target expensive FPGAs. It offers a low-cost, high performance 0.15 μm product that is a true drop-in, pin-for-pin replacement for high-performance 1.2 V and 1.5 V FPGAs, and satisfies the need for medium-density prime ASICs. This unique solution surpasses expectations in reducing time-to-market while delivering significant NRE savings compared to a standard cell ASIC and unit cost savings compared to an FPGA.

XPressArray-II continues the new approach to ASIC development and FPGA-to-ASIC conversions pioneered by XPressArray. XPressArray-II is fabricated using a hybrid technology that integrates an established world-class 0.15 μm front-end process with a proven metal finishing technology. Manufacturing with this hybrid technology achieves the goals of high performance and high density, while enabling the additional benefits of ASICs; low cost and low power utilization. The front-end processing steps are common to multiple applications, significantly reducing the tooling costs that are associated with a 0.15 μm technology. Therefore, the NRE for an XPressArray-II product can be up to 70 percent lower than the NRE of alternative solutions, such as a 0.15 μm standard cell. Furthermore, the unit cost can be 90 percent less than the cost of the original FPGA. Less expensive NRE and unit pricing reduces the required breakeven point for ASIC conversions, filling the significant void in many business models that require a low-cost, high-performance application.

XPressArray-II is a flexible, high-performance, feature packed platform that supports densities of up to 4.8M ASIC gates, FPGA compatible delay-locked loops (DLL) and phase-locked loops (PLL), local clock speeds of up to 500 MHz, and system clock speeds of up to 210 MHz based on single-cycle 18x18 bit multiplier performance for DSP applications. Flexible, high-density

memories are critical to many designs and the XPressArray-II platform delivers in the form of FPGA-like 18 kbit initializable dual-port RAM blocks that can be configured to provide up to 6.1 Mbits of block and distributed memory. Flexibility is also a key advantage of the XPressArray-II I/O technology that includes fully configurable signal, core, and I/O power supply pad locations and support for a wide range of I/O standards, including PCI, PCI-X, Mode 1 and Mode 2, GTL, HSTL, SSTL, and LVPECL. The I/O technology also features a double data rate (DDR) memory interface and 1 Gbps low-voltage differential signaling (LVDS). All of these features are available in a platform that supports power dissipation of just 55 nW/MHz/gate, reducing total chip power consumption to less than 20 percent of a standard FPGA.

XPressArray-II is the only 0.15 µm ASIC solution that offers high levels of integration with clock speeds up to 500 MHz at a fraction of the NRE costs associated with standard cell ASICs and unit costs of FPGAs. Examples of XPressArray products are listed below with their associated costs and prototype lead times.

XPressArray	FPGA	ASIC Gates	RAM Bits	I/Os	50K/Yr NRE	Price	Lead Time*
X2P560-FF672	XC2VP7-FF672	250,000	810,000	459	\$85K	\$40.00	3 weeks
X2P880-BF957	XC2V4000-BF957	860,000	2,200,000	699	\$100K	\$105.00	3 weeks
X2P1200-BG1020	EP1S40-BG1020	590,000	3,400,000	831	\$150K	\$240.000	3 weeks

The Market

High-density FPGAs have changed the programmable logic market by allowing users to prototype their applications with higher-performance solutions. The inherent advantages of FPGAs are flexibility, quick manufacturing turns and low-cost prototypes. These advantages are especially valuable within diverse markets such as automotive, communications, computing, and medical equipment where time-to-market and low development cost are critical to the overall success of their products. FPGAs serve these industries well by helping customers expedite their application development. However, once an application is in production, component costs then become extremely important to profitability, competitive positioning and ultimately, the product lifecycle. A business model with an FPGA conversion strategy targeting an XPressArray-II structured ASIC is an optimal approach for these applications.

The advantages inherent in FPGA conversions also apply to the mid-density ASIC market. The XPressArray-II offers comparable performance to that of cell-based ASICs at a fraction of the upfront engineering cost. In addition, XPressArray-II also provides time-to-market advantages and significantly lower costs for initial prime ASICs targeting medium complexity and medium volume 0.15 µm applications.

Summary

Companies no longer have to choose between two inadequate solutions: the high unit cost associated with FPGAs or the expensive NRE, high production volume and lengthy lead times associated with standard cell ASICs. One of the primary objectives for every company is to reduce system costs without affecting time-to-market or performance. For medium-density, high speed 1.5 V ASIC applications, XPressArray-II is the optimal solution. XPressArray-II minimizes risk, extends product lifecycle and enhances its user's profitability.

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative