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# MINIMISE LATCH-UP SENSITIVITIES IN AUTOMOTIVE ICs

**Starting with first-order analysis, and then by applying best layout practices, you can mitigate those pesky latch-up problems.**

Passing latch-up immunity tests can be a challenge for semiconductor vendors when qualifying new IC designs for automotive applications. Intuitively, chip designers may be expected to increase physical separation of critical transistors on the die. In fact, this brings no appreciable benefits and, in some cases, can make matters worse.

Understanding the causes, and how to predict latch-up threshold, allows effective layout techniques and protection structures to be applied. This ultimately creates a "best-practice" approach to meeting latch-up immunity targets.

## UNDERSTANDING LATCH-UP

Latch-up can occur when a parasitic silicon controlled rectifier (SCR) is created between two PNP and NPN bipolar transistor structures *(Fig. 1)*. Under certain conditions, the SCR can enter into a self-sustained, low-impedance state that lies between the anode and cathode. At this juncture, recovery becomes impossible.

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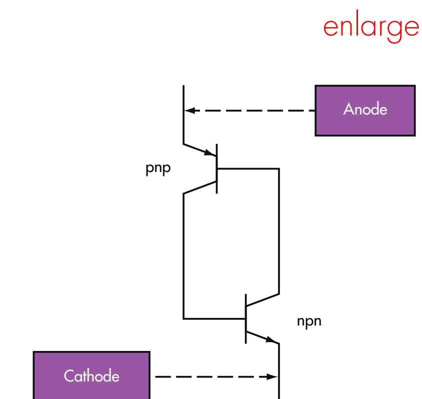


**1. The parasitic SCR is vulnerable to latch-up.**

The onset of latch-up can be analysed in terms of the primary characteristics of an SCR when entering this state. These are the trigger voltage (Vt1), the holding current (IH), and the on-state resistance ($R_{ON}$). When the SCR anode voltage reaches the value of Vt1, there's a sudden and significant reduction in measured voltage accompanied by a surge in current. This is referred to as "snap back."

The circuit can recover from snap back and return to normal operation if the stimulus is removed. On the other hand, if the current continues to increase beyond IH, the device "latches." Once latched, the power supply can support the current flow into the SCR and the device will not return to normal operation until the supply is removed or the device is damaged.

## PREDICTING LATCH-UP THRESHOLD

The hold-up current for the parasitic SCR determines the IC's latch-up threshold. Predicting this threshold is the initial step toward ensuring immunity in the final chip design.

First of all, it's necessary to understand the factors that influence the value of the threshold. In practice, IH is almost completely determined by the values of the two parasitic resistors that set the bias conditions for the respective bipolar transistors.

This being the case, it can be seen that physical separation between the NMOS and PMOS transistors has no practical effect on latch-up immunity. In fact, layout errors have resulted in latch-up occurring between two devices spaced more than 1000μm apart.

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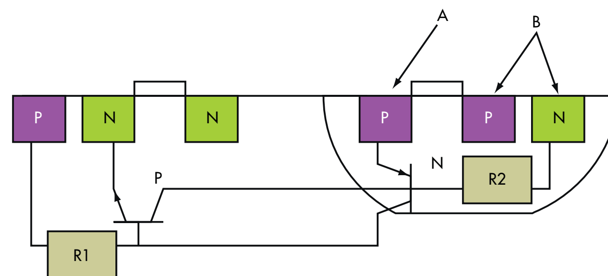


**2. This CMOS cross-section shows the parasitic bipolar transistors (R1 and R2).**

In Figure 2, the parasitic resistors are shown as R1 and R2. The following example describes in detail the sequence of events that lead to latch-up, and shows how the latch-up threshold can be predicted.

Referring to Figure 2:

- Node-A (PMOS drain) is forced to a potential higher than $V_{SUPPLY}$ (Node-B)
- The P-N junction (A-B) will forward bias allowing current to flow through the N-well
- If the external energy source (driving Node-A) is capable of delivering 200mA of current, R2 must be less than 3Ω to prevent the activation of the vertical PNP transistor ($V_{BE}$ = Ifault * R2; 0.6 = 200mA * 3Ω)
- If activated, the flow of current into the substrate via the PNP transistor will drive current through R1 (the exit path)
- If the value of R1 is large enough to develop the required $V_{BE}$ with the available current, the inherent positive feedback will induce latch-up
- By using more realistic values for R1 and R2 (25Ω and 15Ω, respectively, the following latch-up threshold can be predicted:

0.6 = Ith1 * 25
0.6 = Ith2 * 15
Ith1 = 24mA
Ith2 = 40mA

These values for R1 and R2 predict a summed latch-up threshold of 64mA (Ith1 and Ith2 are parallel paths)

- Clearly, if the external fault can deliver 200mA, both R1 and R2 must be less than 6Ω to prevent latch-up.

## PERSISTENT CONDITION

If latch-up occurs, this condition can persist because Node-B (driven by the power supply to the IC) comprises a second PNP transistor. Once the NPN actively pulls current from the N-well, current is supplied from both base regions. Hence, latch-up can persist after the fault current is removed, due to the activity of the second PNP transistor.

In high-voltage structures, such as ICs designed for automotive applications, the drain is typically extended to account for the high $V_{DD}$. This physical extension effectively increases the value of R1 and R2, leading to even greater latch-up sensitivity.

## LATCH-UP TESTING

For devices seeking automotive qualification, the Automotive Electronics Council (AEC) Q-100 document specifies IC latch-up criteria with reference to the JEDEC Standard IC latch-up test. In fact, both of these standards are almost interchangeable.

These specifications identify two categories of testing. Class I is performed at room temperature

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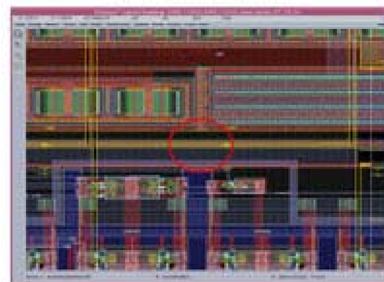
and Class II is defined as at the maximum ambient operating temperature. Class II is typically done at 125°C for AEC Q-100 qualifications unless otherwise defined.

## LAYOUT PRACTICES TO AVOID LATCH-UP

Fortunately, a number of layout techniques are available to eliminate or reduce circuit susceptibility to latch-up. These range from straightforward measures, such as the positioning of supply-voltage pins, to a variety of more complicated measures.

Standard industry layout practices include:

- Every well must have a substrate contact of the appropriate type.
- Every substrate contact should be directly metal-connected to a supply pad.
- Place substrate contacts as close as possible to the source connection of transistors connected to the supply rails (a less conservative rule is to place a substrate contact for every five to 10 transistors or every 25 to 100μm)
- Position n- and p-transistors with packing of n-devices toward $V_{SS}$ and p-devices toward $V_{DD}$.



**3. Certain layout locations can be latch-up-sensitive, such as is the case with the N-well tie (circled in red) in this PMOS device.**

- Connect P+ guard rings to $V_{SS}$ around n-transistors.
- Connect N+ guard rings to $V_{DD}$ around p-transistors.

Guard rings are areas of p+ or n+ diffusion placed inside or around a well or circuit cluster. These are intended to provide a biased diffusion area that collects substrate carriers, thereby decoupling parasitic bipolar structures. There are two types of these structures: minority carrier guard rings and majority carrier guard rings.

Minority carrier guard rings are used to collect injected minority carriers before they're collected by a reverse-biased, well-to-substrate junction. Once collected, they become majority carriers. The current-surge in the well could then result in a voltage drop large enough to turn on a parasitic bipolar, leading to latch-up.

Majority carrier guard rings decouple the parasitic bipolar transistors by minimising the voltage drop created by majority carrier currents. Once again, the current surge in the well could result in a voltage drop that's large enough to turn on a parasitic bipolar, which leads to latch-up.

Butted contacts are relevant for latch-up since they effectively reduce the base-emitter shunting resistance (R2). The ideal layout will depend on whether these emitters (diffusion areas in the N-well) are connected or left floating, and on their relative size by either acting as a real butted contact or a reverse-biased well tie. Ironically, the proper layout is relatively simple, but it's somewhat complicated to determine.

However, design rules for mixed-signal ICs don't allow for butted contacts because of noise considerations. Instead, an extensive guard bar and/or separate power domains may be considered for digital and mixed-signal applications.

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Parasitic bipolar base width has also been analysed to determine its effect on latch-up sensitivity. Although the separation between the p+ emitter and the well mask edge (Xp) has relatively little effect, the separation between the n+ emitter and n-well edge (Xn) is more influential.

There are two competing effects on npn emitter latch-up trigger current: R2 increases with Xn and current gain (ßnpn) lowers for increasing Xn. However, the increase in R2 dominates for small values of Xn, while at large Xn the variation in (ßnpn) becomes the major effect. Therefore, contrary to what would be natural assumptions, wider structures can in fact be more sensitive to latch-up.

An example of a latch-up problematic layout is shown in Figure 3. The red-circled area is the resistive N-well tie for a 20V PMOS device circled in black. The problem is that the exit path for the N-well tie uses small transistors in series from the well to the power supply. This places a moderate impedance in series with the N-well tie, which will forward-bias the base-emitter junction of the parasitic pnp transistor at very low current levels.

## OTHER LATCH-UP CONSIDERATIONS

The use of epitaxial starting material has been a very popular choice to reduce latch-up sensitivity. Essentially, the lightly doped epi layer provides IC-quality silicon, while the heavily doped substrate draws stray currents away from the active device area.

The junction formed by the lightly doped epi layer and the heavily doped substrate provides a built-in field that directs majority carriers into the substrate. Injected minority carriers are also reflected back into the epi layer. The combined effect is to create guard rings that are more effective.

Finally, ESD protection structures can impact latch-up performance. Simple diode junctions may shunt potentially harmful currents, which would increase the latch-up immunity of a given output topology. In contrast, ESD protection structures with bipolar characteristics (like snap-back or SCR structures) can have holding currents that are low enough to be triggered by latch-up stress. Consequently, care must be taken to ensure that ESD structures aren't active during reasonable overstress conditions.

## CONCLUSION

A first-order analysis is able to predict latch-up threshold, something that should be performed for any transistor which makes an off-chip connection. When armed with this basic information, designers are then able to apply best layout practices in order to mitigate latch-up sensitivity.

Physical separation of transistors, alone, isn't sufficient to meet AEC-Q-100 or JEDEC (Joint Electron Devices Engineering Council) latch-up standards, although the selection of starting material will utlimately influence the device's sensitivity to latch-up. In addition, designers are recommended to consider latch-up simultaneously with measures to ensure ESD immunity. ■

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