Implementing HV cell technologies in next-generation SoCs

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The HV standard cell methodologies described in this article allow engineering teams to alleviate the risks associated with designs using higher voltages. The reliability, performance benchmarks and the breadth of features of the proposed design will thus meet expectations, and justify the investment made.

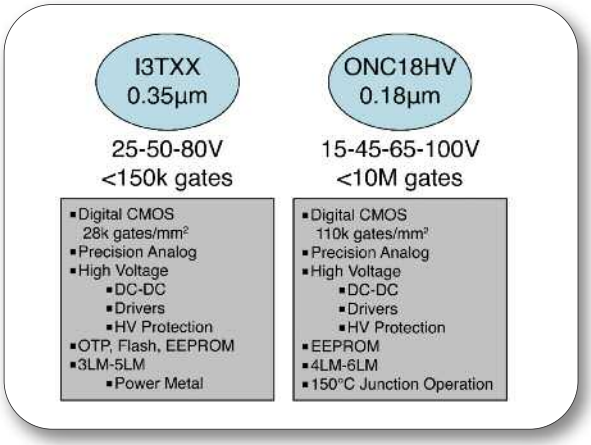

Figure 1: Examples of the HV processes offered by ON Semiconductor

Migration to more detailed semiconductor geometries is key to the progress of modern System-on-Chip (SoC) design. The pace at which new process nodes emerge has not slowed in over forty years, and is unlikely to do so for a long time into the future. This has enabled support of larger quantities of digital content and greater memory capacities, as well as processing changes from analog signals to digital, so that systems can interact with the real world through sensors, etc. This article provides a comprehensive guide to assist those in need of higher voltage operation in these smaller architectures.

High voltage (HV) small-geometry technologies allow more sophisticated signal processing via DSPs and more powerful microcontrollers, as well as support for higher speed interfacing (such as 10/100 Ethernet, CAN 2.0, USB 2.0, and I²C). By utilization of HV process technologies, system designers can integrate high density logic and mixed signal circuitry together with high performance drivers onto single IC devices. However there are sizeable hurdles that need to be overcome if this is to be achieved.

Though HV offers clear advantages in terms of system performance, there are a number of aspects that need to be taken into account before opting to follow this route. Engineering teams looking to make use of application-specific integrated circuits (ASICs) based on a smaller geometry HV semiconductor process should first consider the impact this will have on the effectiveness of their system design.

System reliability and operational lifespan: It is vital that the engineers involved are fully aware of what time period their system will reside within HV domains. From this it will be possible to assess whether utilizing higher voltage levels will be applicable, or whether they will impact too greatly on the long-term operation of the system.

Technology costs: Bipolar CMOS-DMOS (BCD) processes are very expensive to implement, and as a result should not be entered into without careful thought. Proper analysis of the proposed system should be embarked upon beforehand, as potentially there may be more suitable and less expensive solutions for the particular task. It may prove more appropriate to employ a multiple die approach, rather than try to integrate everything on one piece of silicon.

Electrostatic discharge (ESD) issues: Due to the high voltages involved, there is an inherent risk of exposure to ESD – this effectively comes with the territory. Also there is likely to be a need for qualification of the IP in these conditions, to ensure that it does not prove vulnerable to damage.

Heat dissipation: To understand and alleviate the high levels of heat produced by the chip, there is a clear need for thermal modeling for both the die and the package of the device to be undertaken, as well as the use of advanced, thermally-enhanced packaging techniques.

Partitioning of LV/HV sections of the chip: Depending on the voltage levels present on a single silicon substrate, HV isolation may require a substantial amount of area. Proper floor-planning of circuitry in the different voltage domains is critical to minimize wasted space.

Latch-up issues: With big drivers in operation, there can often be a lot of overshoot and ringing in this type of systems, depending on the load. Efforts must be made to protect the thin gate oxides on the chip, so that the operational lifespan is not shortened.

Modeling of safe operating areas (SOA): When creating HV analog circuits, the designer needs to know when transistors are being stressed to the point of breakdown. For this reason, it is vital that the transistor models contain flags that will alert the designer during simulation so that the risks can be mitigated.

Bandwidth issues: Because of the high capacitive loads involved and the fact that thinner gate oxides are needed for higher-frequency HV chip design, there can potentially be speed limitations on the system. It will be necessary to ascertain if these limitations will have an adverse influence on the overall performance.

Temperature issues: When the system is designed for applications in uncompromising environments (such as automotive, heavy industrial, etc) then the effect that temperature could have on system performance also needs to be thoroughly looked into.

Understanding the high voltage requirements of the design: Sometimes the best solution is not a fully-integrated solution, and the HV element should in fact be off-chip. Understanding the HV requirements of the design allows the system architect and their design team to make the right decisions to enable delivery of the best overall solution to the customer. From these considerations it is clear that anyone embarking on a project of this kind should engage with a semiconductor vendor that has amassed experience in HV implementations and is capable of offering innovative process technologies optimized for this purpose. The consequences that could result from not taking this course of action are that the system produced will fall short of its targets, in terms of both performance and longevity.

The third-generation of I3TXX smart-power technology developed by ON Semiconductor is a HV-capable platform using 0.35 µm BCD. It is aimed at the HV mixed signal system designs required for leading edge automotive, military, medical and industrial applications. The platform includes 3.3V gate oxides and a dual-gate 18V capability in some technology variants. Also available are different isolation schemes including P-sinker, deep-well, and deep-trench isolation with up to 62V operation. This technology family is fully enabled with a large selection of foundation IP. It has a junction temperature range of -40°C to 150°C with a lifetime profile of up to 175°C. ON Semiconductor's ONC18 process is a low-cost industry-compatible 0.18 µm CMOS technology currently being enabled for operation up to 100V. This full featured process includes 1.8 V/3.3 V dual gate I/Os, nominal and high value MIM capacitors, resistors, and a construction of six levels of metal. It has a junction temperature range of -55°C to 125°C with a lifetime profile up to 150°C. The ONC18 process is highly suited to the development of low power and highly integrated circuits combining digital and mixed signal functionality, allowing the creation of ASICs with up to 10M logic gates. It can support memory capacities of up to 1.1Mbits of synchronous single port and 512Kbits of dual port SRAM, or 1.1Mbits of high density, low leakage VIA-programmable ROM. EEPROM is available for analog trim or up to 8k Bytes of program or data memory.

By employing an approach based on modular technology platforms such as these, it has been possible to leverage existing IP that was originally meant for lower voltage processes, thus keeping the engineering overhead to a minimum. It means that both HV and low-power functionality can be implemented on the same chip when this proves to be appropriate. ■