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AN-4140

Transformer Design Consideration for Offline Flyback Converters Using Fairchild Power Switch (FPS™)

1. Introduction

For flyback coverters, the transformer is the most important factor that determines the performance such as the efficiency, output regulation and EMI. Contrary to the normal transformer, the flyback transformer is inherently an inductor that provides energy storage, coupling and isolation for the flyback converter. In the general transformer, the current flows in both the primary and secondary winding at the same time. However, in the flyback transformer, the current flows only in the primary winding while the energy in the core is charged and in the secondary winding while the energy in the core is discharged. Usually gap is introduced between the core to increase the energy storage capacity.

This paper presents practical design considerations of transformers for off-line flyback converters employing Fairchild Power Switch (FPS). In order to give insight to the reader, practical design examples are also provided.

2. General Transformer design procedure (1)

Choose the proper core

Core type : Ferrite is the most widely used core material for commercial SMPS (Switchied mode power supply) applications. Various ferrite cores and bobbins are shown in Figure 1. The type of the core should be chosen with regard to system requirements including number of outputs, physical height, cost and so on. Table 1 shows features and typical application of various cores.

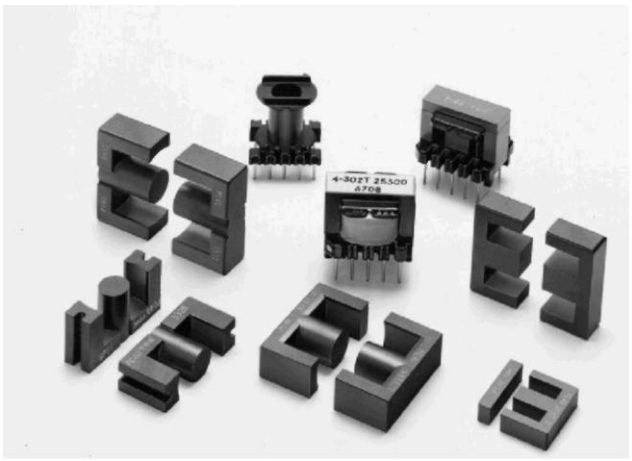


Figure 1. Ferrite core (TDK)

Core	Features	Typical Applications
EE EI	-Low cost	Aux. power Battery charger
EFD EPC	-Low profile	LCD Monitor
EER	-Large winding window area -Various bobbins for multiple output	CRT monitor, C-TV DVDP, STB
PQ	-Large cross sectional area -Relatively expensive	

Table 1. Features and typical applications of various cores

Core size: Actually, the initial selection of the core is bound to be crude since there are too many variables. One way to select the proper core is to refer to the manufacture's core selection guide. If there is no proper reference, use the table 2 as a starting point. The core recommended in table 1 is typical for the universal input range, 67kHz switching frequency and 12V single output application. When the input voltage range is 195-265 Vac (European input range) or the switching frequency is higher than 67kHz, a smaller core can be used. For an application with low voltage and/or multiple outputs, usually a larger core should be used than recommended in the table.

Output Power	EI core	EE core	EPC core	EER core
0-10W	EI12.5 EI16 EI19	EE8 EE10 EE13 EE16	EPC10 EPC13 EPC17	
10-20W	EI22	EE19	EPC19	
20-30W	EI25	EE22	EPC25	EER25.5
30-50W	EI28 EI30	EE25	EPC30	EER28
50-70W	EI35	EE30		EER28L
70-100W	EI40	EE35		EER35
100-150W	EI50	EE40		EER40 EER42
150-200W	EI60	EE50 EE60		EER49

Table 2. Core quick selection table (For universal input range, fs=67kHz and 12V single output)

Once the core type and size are determined, the following variables are obtained from the core data sheet.

- A_e : The cross-sectional area of the core (mm^2)
- A_w : Winding window area (mm^2)
- B_{sat} : Core saturation flux density (tesla)

Figure 2 shows the Ae and A_w of a core. The typical B-H characteristics of ferrite core from TDK (PC40) are shown in Figure 3. Since the saturation flux density (B_{sat}) decreases as the temperature increases, the high temperature character-istics should be considered. If there is no reference data, use B_{sat} =0.3~0.35 T.

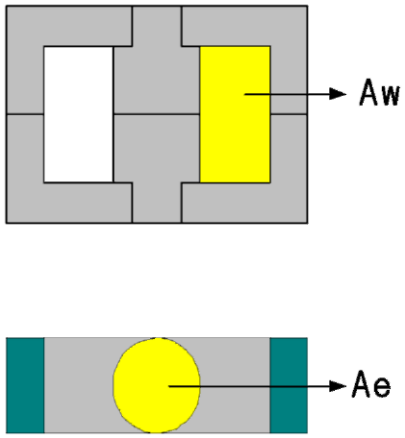
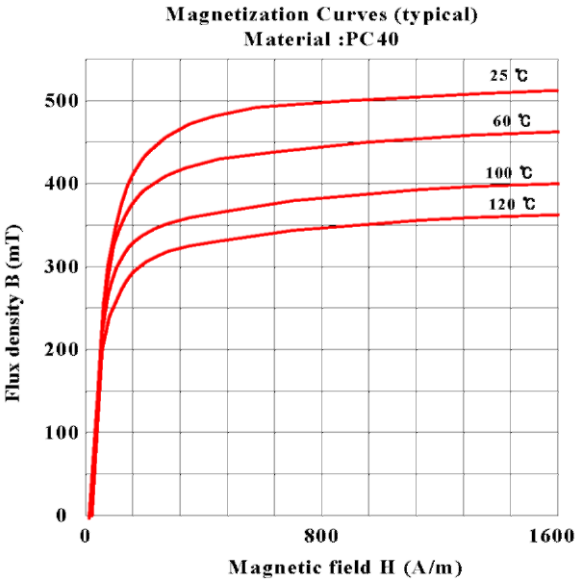


Figure 2. Window Area and Cross Sectional Area



Magnetization Curves (typical)-Magnetization Curves (typical)

Material :PC40100-Material :PC40100

Flux density B (mT)-Flux density B (mT)

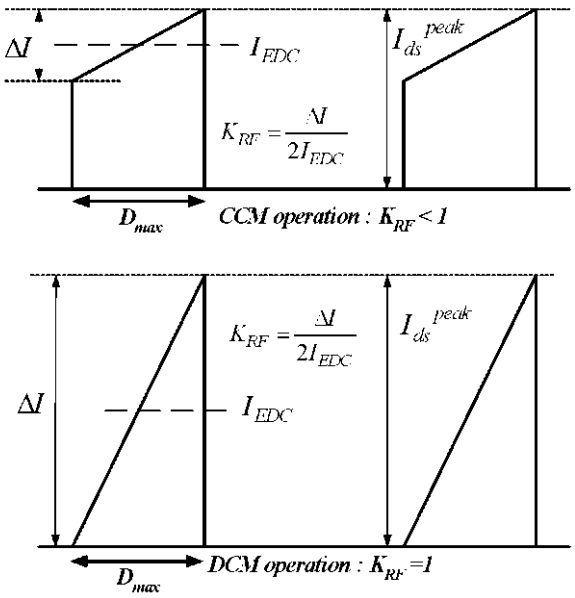
Magnetic field H (A/m)-Magnetic field H (A/m)

Figure 3. Typical B-H characteristics of ferrite core (TDK/PC40)

(2) Determine the primary side inductance (L_m) of the transformer

In order to determine the primary side inductance, the following variables should be determined first. (For a detailed design procedure, please refer to the application note AN4137.)

- P_{in} : Maximum input power
- f_s : Switching frequency of FPS device
- V_{DC}^{min} : Minimum DC link voltage
- D_{max} : Maximum duty cycle
- K_{RF} : Ripple factor, which is defined at the minimum input voltage and full load condition, as shown in Figure 4. For DCM operation, K_{RF} = 1 and for CCM operation K_{RF} < 1. The ripple factor is closely related with the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced through reducing the ripple factor, too small a ripple factor forces an increase in transformer size. Considering both efficiency and core size, it is reasonable to set K_{RF} = 0.3-0.5 for the universal input range and K_{RF} = 0.4-0.8 for the European input range. Meanwhile, in the case of low power applications below 5W where size is most critical, a relatively large ripple factor is used in order to minimize the transformer size. In that case, it is typical to set K_{RF} = 0.5-0.7 for the universal input range and K_{RF} = 1.0 for the European input range.



peak-peak

DCM operation-DCM operation

EDC-EDC

Figure 4. MOSFET Drain Current and Ripple Factor (K_{RF})

With the given variables, the primary side inductance, L_m is obtained as

$$L_m = \frac{(V_{DC}^{min} \cdot D_{max})^2}{2P_{in} f_s K_{RF}} \qquad (1)$$

min-min

max-max

where V_{DC}^{min} is the minimum DC input voltage, D_{max} is the maximum duty cycle, P_{in} is the maximum input power f_s is the switching frequency of the FPS device and K_{RF} is the ripple factor.

Once L_m is determined, the maximum peak current and RMS current of the MOSFET in normal operation are obtained as

$$I_{ds}^{peak} = I_{EDC} + \frac{\Delta I}{2} \qquad (2)$$

$$I_{ds}^{rms} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{max}}{3}} \qquad (3)$$

$$\text{where} \quad I_{EDC} = \frac{P_{in}}{V_{DC}^{min} \cdot D_{max}} \qquad (4)$$

$$\text{and} \quad \Delta I = \frac{V_{DC}^{min} D_{max}}{L_m f_s} \qquad (5)$$

rms-rms where-where and-and in-in

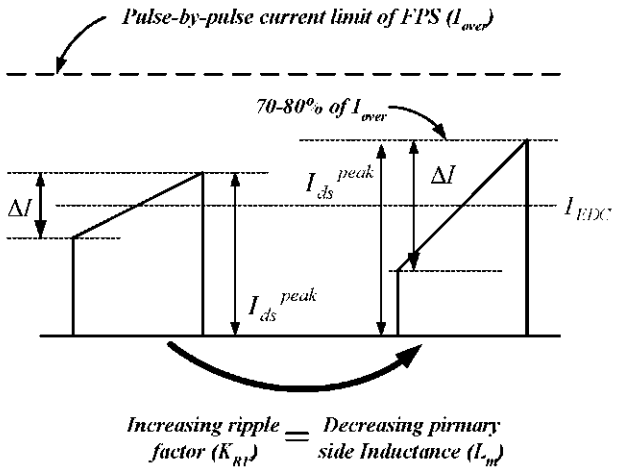
With the chosen core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by

$$N_P^{min} = \frac{L_m I_{over}}{B_{sat} A_e} \times 10^6 \quad (turns) \qquad (6)$$

tums-tums over-over sat-sat

where L_m is the primary side inductance, I_{over} is the FPS pulse-by-pulse current limit level, A_e is the cross-sectional area of the core and B_{sat} is the saturation flux density in tesla.

If the pulse-by-pulse current limit level of FPS is larger than the peak drain current of the power supply design, it may result in excessive transformer size since I_{over} is used in determining the minimum primary side turns as shown in equation (6). Therefore, it is required to choose a FPS with proper current limit specifications or to adjust the peak drain current close to I_{over} by increasing the ripple factor as shown in Figure 5. It is reasonable to design Id_s^{peak} to be 70-80% of I_{over} considering the transient response and tolerance of I_{over}.



Pulse-by-pulse current limit of FPS (I_{over})

Increasing ripple factor (K_{RF})

Decreasing pirmary side Inductance (L_m)

Figure 5. Adjustment peak drain current

(3) Determine the number of turns for each output

Figure 6 shows the simplified diagram of the transformer, whrere V_{o1} stands for the reference output that is regulated by the feedback control while $V_{o(n)}$ stands for the n-th output.

First, determine the turns ratio (n) between the primary side and the feedback controlled secondary side as a reference.

$$n = \frac{V_{R0}}{V_{o1} + V_{F1}} = \frac{N_P}{N_{s1}} \qquad (7)$$

where N_p and N_{s1} are the number of turns for primary side and reference output, respectively, V_{o1} is the output voltage and V_{F1} is the diode (D_{R1}) forward voltage drop of the reference output that is regulated by the feedback control.

Then, determine the proper integer for N_{s1} so that the resulting Np is larger than N_p^{min} obtained from equation (6).

The number of turns for the other output (n-th output) is determined as

$$N_{s(n)} = \frac{V_{o(n)} + V_{F(n)}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (8)$$

turns-turns

The number of turns for Vcc winding is determined as

$$N_a = \frac{V_{cc}^* + V_{Fa}}{V_{o1} + V_{F1}} \cdot N_{s1} \quad (turns) \qquad (9)$$

where V_{cc}* is the nominal value of the supply voltage of the FPS device, and V_{Fa} is the forward voltage drop of D_a as defined in Figure 6. Since V_{cc} increases as the output load increases, it is proper to set V_{cc}* as V_{cc} start voltage (refer to the data sheet) to avoid triggering the over voltage protection during normal operation.

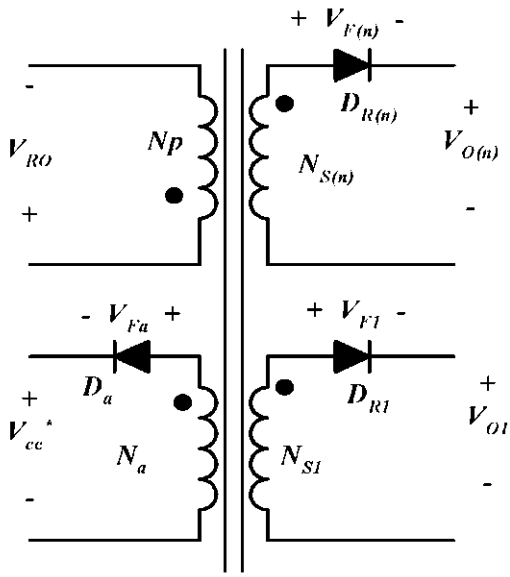


Figure 6. Simplified diagram of the transformer

Once the number of turns on the primary side have been determined, the gap length of the core is obtained through approximation as

$$G = 40\pi A_e\left(\frac{N_P{}^2}{1000L_m} - \frac{1}{A_L}\right) \quad (mm) \qquad (10)$$

where A_L is the AL-value with no gap in nH/turns^2, *Ae* is the cross sectional area of the core as shown in Figure 2, L_m is specified in equation (1) and N_p is the number of turns for the primary side of the transformer

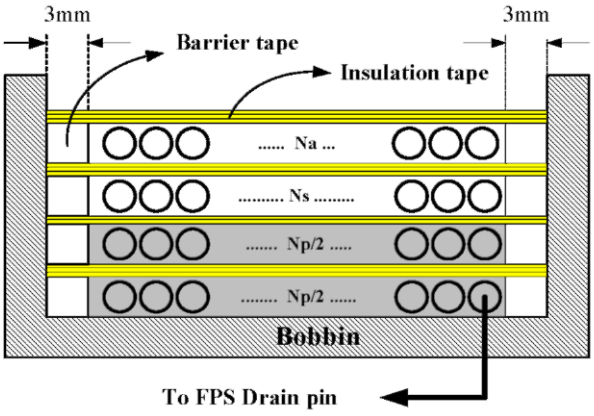
(4) Determine the wire diameter for each winding

The wire diameter is determined based on the rms current through the wire. The current density is typically 5A/mm^2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 6-10 A/mm^2 is also acceptable. Avoid using wire with a diameter larger than 1 mm to avoid severe eddy current losses as well as to make winding easier. For high current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

3. Transformer Construction Method.

(1) Winding Sequence (a)

Primary winding



Bobbin-**Bobbin**
Barrier tape-**Barrier tape**
Insulation tape-**Insulation tape**
To FPS Drain pin-**To FPS Drain pin**
Figure 7. Primary side winding

It is typical to place all the primary winding or a portion of the primary winding innermost on the bobbin. This minimizes the length of wire, reducing the conduction loss in the wire. The EMI noise radiation can be reduced, since the other windings can act as Faraday shields.

When the primary side winding has more than two layers, the innermost layer winding should start from the drain pin of FPS as shown in Figure 7. This allows the winding driven by the highest voltage to be shielded by other windings, thereby maximizing the shielding effect.

(b) Vcc winding

In general, the voltage of each winding is influenced by the voltage of the adjacent winding. The optimum placement of the Vcc winding is determined by the over voltage protection (OVP) sensitivity, the Vcc operating range and control scheme.

-**Over voltage protection (OVP) sensitivity** : When the output voltage goes above its normal operation value due to some abnormal situation, Vcc voltage also increases. FPS uses Vcc voltage to indirectly monitor the over voltage situation in the secondary side. However, a RCD snubber network acts as an another output as shown in Figure 8 and Vcc voltage is also influenced by the snubber capacitor voltage. Because the snubber voltage increases as the drain current increases, OVP of FPS can be triggered not only by the output over voltage condition, but also by the over load condition.

The sensitivity of over voltage protection is closely related to the physical distance between windings. If the Vcc winding is close to the secondary side output winding, Vcc voltage will change sensitively to the variation of the output voltage. Meanwhile, if the Vcc winding is placed close to the primary side winding, Vcc voltage will vary sensitively as the snubber capacitor voltage changes.

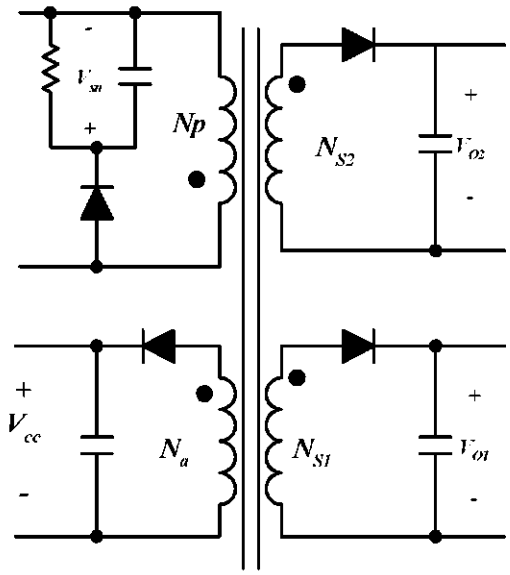
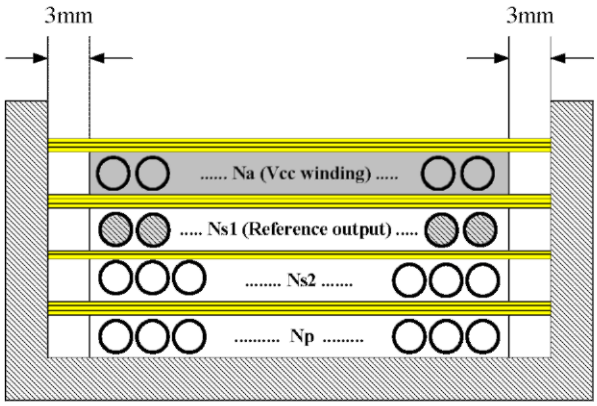


Figure 8. Primary side winding

- **Vcc operating range** : As mentioned above, Vcc voltage is influenced by the snubber capacitor voltage. Since the snubber capacitor voltage changes according to drain current, Vcc voltage can go above its operating range triggering OVP in normal operation. In that case, Vcc winding should be placed closest to the reference output winding that is regulated by feedback control and far from the primary side winding as shown in Figure 9.



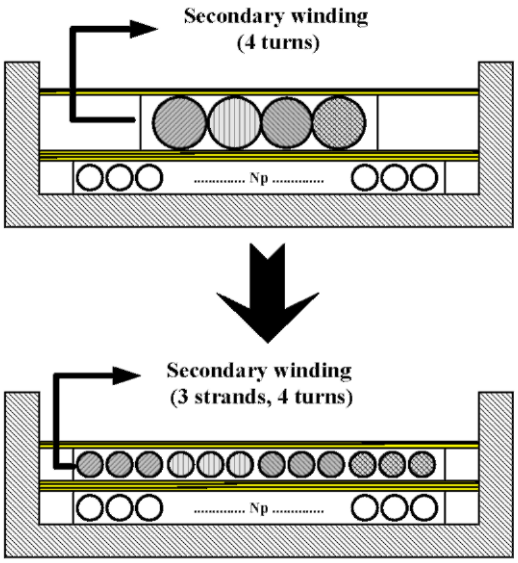
Na (Vcc winding)-Na (Vcc winding)
Ns1 (Reference output)-Ns1 (Reference output)

Figure 9. Winding sequence to reduce Vcc variation

- **Control scheme** : In the case of primary side regulation, the output voltages should follow the Vcc voltage tightly for a good output regulation. Therefore, Vcc winding should be placed close to the secondary windings to maximize the coupling of the Vcc winding with the secondary windings. Meanwhile, Vcc winding should be placed far from primary winding to minimize coupling to the primary. In the case of secondary side regulation, the Vcc winding can be placed between the primary and secondary or on the outermost position.

(c) Secondary side winding

When it comes to a transformer with multiple outputs, the highest output power winding should be placed closest to the primary side winding, to reduce leakage inductance and to maximize energy transfer efficiency. If a secondary side winding has relatively few turns, the winding should be spaced to traverse the entire width of the winding area for improved coupling. Using multiple parallel strands of wire will also help to increase the fill factor and coupling for the secondary windings with few turns as shown in Figure 10. To maximize the load regulation, the winding of the output with tight regulation requirement should be placed closest to the winding of the reference output that is regulated by the feedback control.



Secondary winding (4 turns)
Secondary winding (3 strands, 4 turns)

Figure 10. Multiple parallel strands winding

(2) Winding method

-Stacked winding on other winding: A common technique for winding multiple outputs with the same polarity sharing a common ground is to stack the secondary windings instead of winding each output winding separately, as shown in Figure 11. This approach will improve the load regulation of the stacked outputs and reduce the total number of secondary turns. The windings for the lowest voltage output provide the return and part of the winding turns for the next higher voltage output. The turns of both the lowest output and the next higher output provide turns for succeeding outputs. The wire for each output must be sized to accommodate its output current plus the sum of the output currents of all the output stacked on top of it.

-Stacked winding on other output: If a transformer has a very high voltage and low current output, the winding can be stacked on the lower voltage output as shown in Figure 12. This approach provides better regulation and reduced diode voltage stress for the stacked output. The wire and rectifier diode for each output must be sized to accommodate its output current plus the sum of the output currents of all the output stacked on top of it.

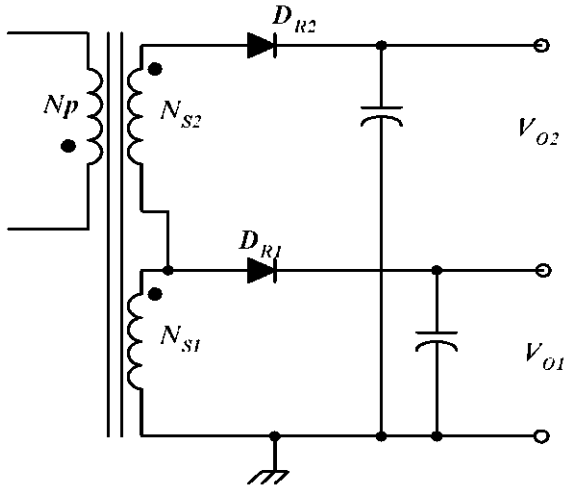


Figure 11. Stacked winding on other winding

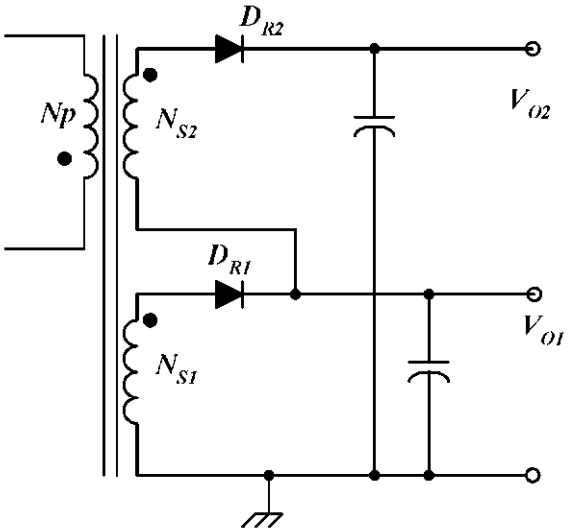


Figure 12. Stacked winding on other output

(3) Minimization of Leakage Inductance

The winding order in a transformer has a large effect on the leakage inductance. In a multiple output transformer, the secondary with the highest output power should be placed closest to the primary for the best coupling and lowest leakage. The most common and effective way to minimize the leakage inductance is a sandwich winding as shown in Figure 13.

Secondary windings with only a few turns should be spaced across the width of the bobbin window instead of being bunched together, in order to maximize coupling to the primary. Using multiple parallel strands of wire is an additional technique of increasing the fill factor and coupling of a winding with few turns as shown in Figure 10.

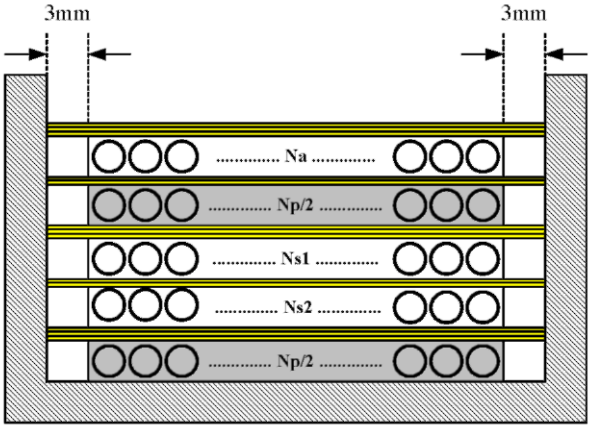
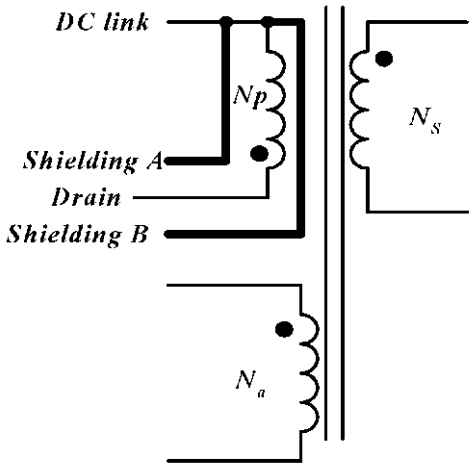


Figure 13. Sandwich winding

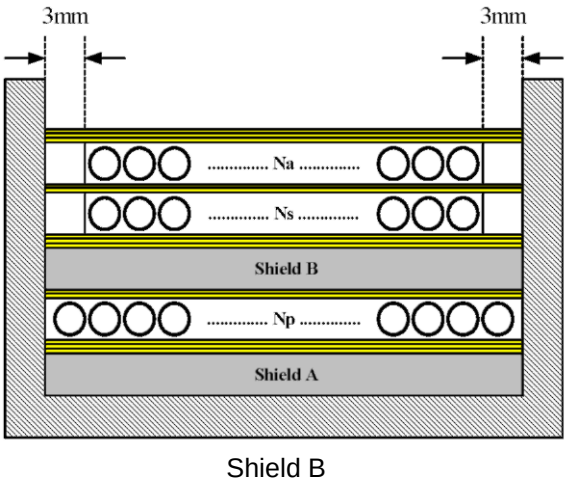
(4) Transformer shielding

A major source of common mode EMI in Switched Mode Power Supply (SMPS) is the parasitic capacitances coupled to the switching devices. The MOSFET drain voltage drives capacitive current through various parasitic capacitances. Some portion of these capacitive currents flow into the neutral line that is connected to the earth ground and observed as common mode noise. By using an electrostatic separation shield between the windings (at primary winding side, or at secondary winding side, or both), the common mode signal is effectively "shorted" to the ground and the capacitive current is reduced. When properly designed, such shielding can dramatically reduce the conducted and radiated emissions and susceptibility. By using this technique, the size of EMI filter can be reduced. The shield can be easily implemented using copper foil or tightly wound wire. The shield should be virtually grounded to a quiescent point such as primary side DC link, primary ground or secondary ground.

Figure 14 shows a shielding example, which allows the removal of the Y-capacitor that is commonly used to reduce common mode EMI. As can be seen, shields are used not only on the bottom but also on the top of the primary winding in order to cancel the coupling of parasitic capaci-tances. Figure 15 also shows the detailed shielding construction.

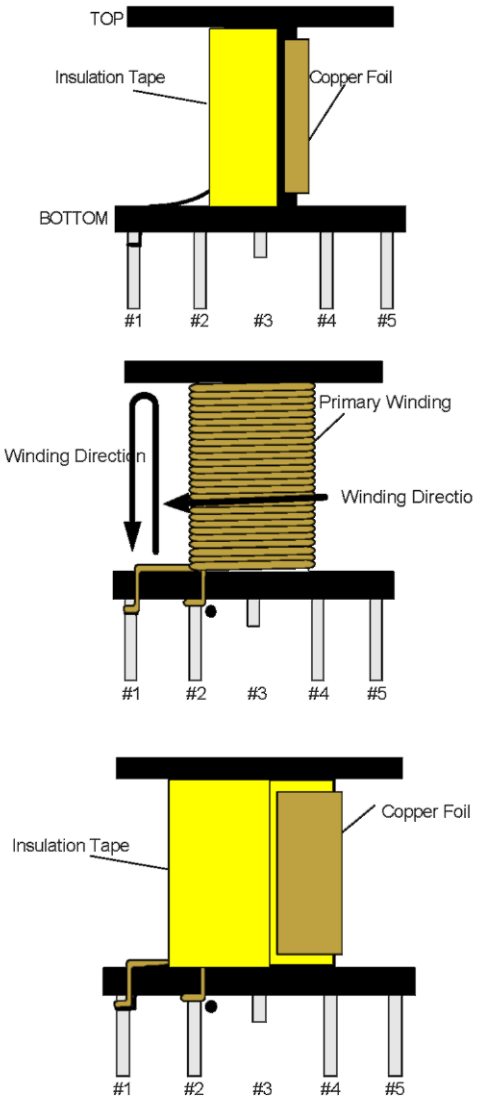


DC link-DC link Shielding A–Shielding A Drain-Drain



Shield B

Figure 14. Shielding example to remove Y-capacitor



TOP-TOP Insulation Tape-Insulation Tape Copper Foil-Copper Foil
BOTTOM-BOTTOM Primary Winding-Primary Winding
Winding Direction-Winding Direction Copper Foil-Copper Foil
Insulation Tape- Insulation Tape

Figure 15. Shielding method to remove Y-Capacitor

(5) Practical examples of transformer construction

As described in the above sections, there many factors that should be considered in determining the winding sequence and winding method. In this section some practical examples of transformer construction are presented to give a compre-hensive understanding of practical transformer construction.

a) LCD monitor SMPS example

Figure 16 shows a simplified transformer schematic for typical LCD monitor SMPS. The 5V output is for the Micro-processor and 13V output is for the inverter input of LCD back light. While 5V output is regulated with the feedback control, 13V output is determined by the transformer turns ratio and a stacked winding is usually used to maximize the regulation.

Transformer construction Example A (Figure 17) : In this example, the leakage inductance is minimized by employing a sandwich winding. The Vcc winding is placed outside to provide shielding effect. Since the Vcc winding is placed on the top half of primary winding, the coupling between the Vcc winding and 5V output winding is poor, which may require a small dummy load on the 5V output to prevent UVLO (Under Voltage Lock Out) in the no load condition.

Transformer construction Example B (Figure 18) : In this example, the leakage inductance is larger than example A, since a sandwich winding is not used. However, the Vcc winding is tightly coupled with the 5V output winding and Vcc remains its normal operation range in the no load condition. Even though this approach can prevent UVLO in no load conditions without dummy load, the power conversion efficiency might be relatively poor compared to example A due to the large leakage inductance.

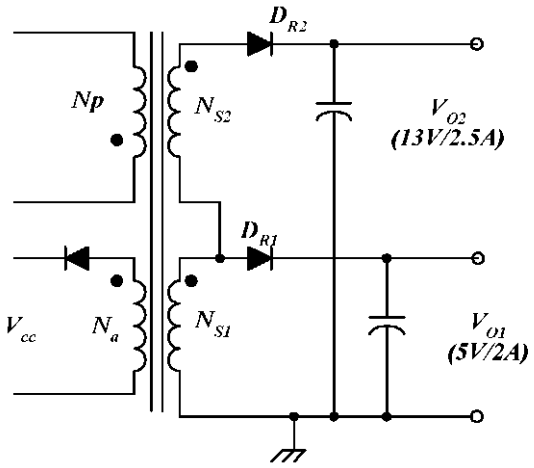


Figure 16. LCD monitor SMPS transformer example

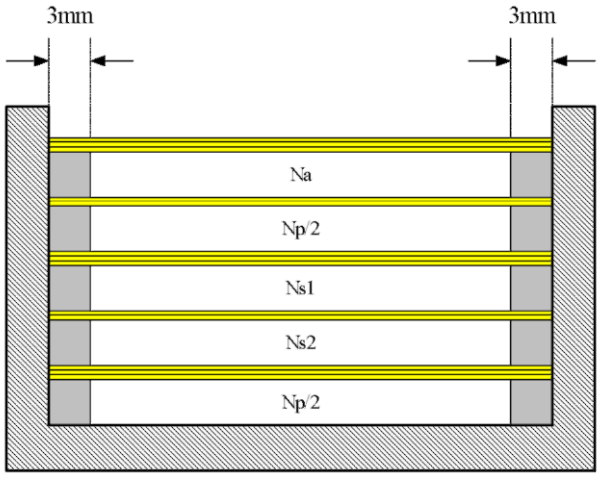


Figure 17. LCD monitor SMPS transformer construction example (A)

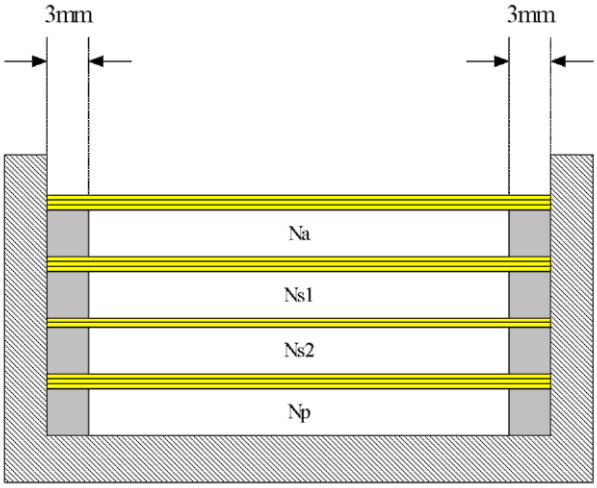


Figure 18. LCD monitor SMPS transformer construction example (B)

(b) CRT monitor SMPS example - PSR (Primary side regulation)

Figure 19 shows a simplified transformer schematic for a typical CRT monitor SMPS employing PSR (Primary side regulation). 80V and 50V outputs are the main output having high output power. Meanwhile, 5V and 6.5V outputs are auxiliary output having small output power. The 80V output winding is stacked on the 50V output to reduce the voltage stress of the rectifier diode (D_{R1}).

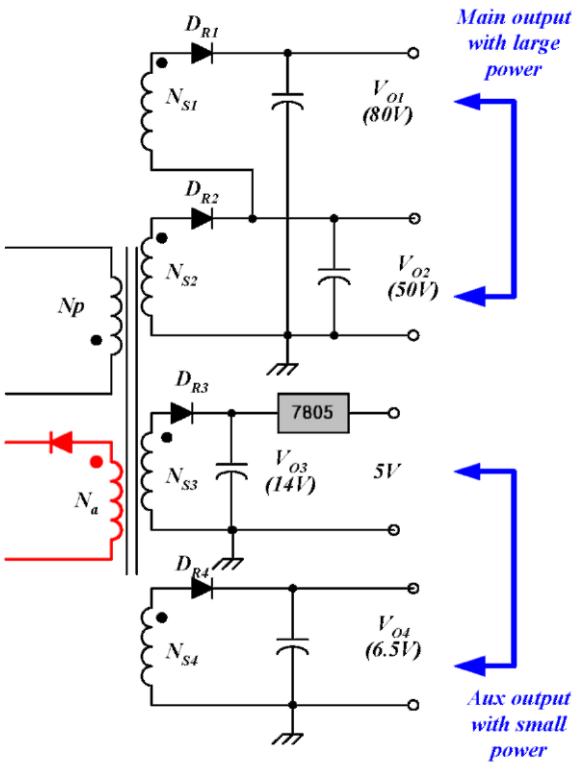


Figure 19. CRT monitor SMPS transformer example-PSR

Figure 20 shows the detailed transformer construction. In order to minimize the leakage inductance, sandwich winding is employed and the main output windings are placed closest to the primary winding. The Vcc winding is placed closest to the main output windings to provide tight regulations of the main output. The auxiliary output windings are placed outside of the primary winding to provide a shielding effect.

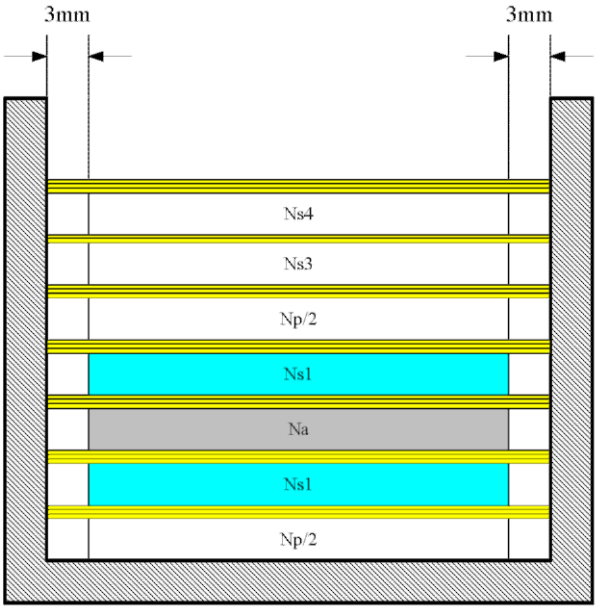


Figure 20. CRT monitor SMPS transformer construction example (PSR)

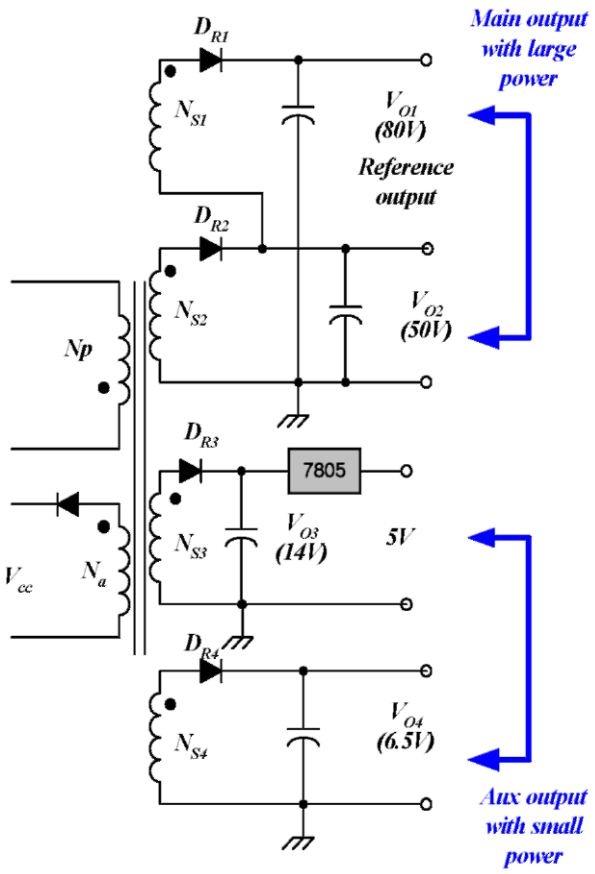


Figure 21. CRT monitor SMPS transformer example-SSR

(c) CRT monitor SMPS example - SSR (Secondary side regulation)

Figure 21 shows a simplified transformer schematic for typical CRT monitor SMPS employing SSR (Secondary side regulation). 80V and 50V outputs are the main output having high output power. Meanwhile, 5V and 6.5V outputs are auxiliary output having small output power. The 80V output winding is stacked on 50V output to reduce the voltage stress of the rectifier diode (D_{R1}). Figure 22 shows the detailed transformer construction. In order to minimize the leakage inductance, a sandwich winding is employed and the main output windings are placed closest to the primary winding. The Vcc winding is placed outermost to provide a shielding effect. The auxiliary output windings are placed between windings of the main output winding to obtain better regulation.

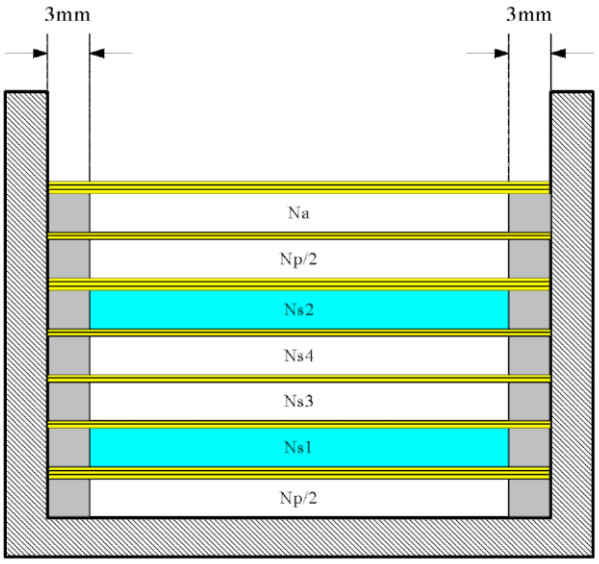


Figure 22. CRT monitor SMPS transformer construction example (SSR)

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