

# FXMA2102 I<sup>2</sup>C Translator

## AN-9718/D

### Introduction

The FXMA2102 is a high-performance voltage-level translator, or level shifter, specifically designed for I<sup>2</sup>C and SMBUS open-drain applications. It features auto-direction and can translate either side (A or B) from 1.65 V to 5.5 V.

The FXMA2102 has open-drain I/Os and requires external pull-up resistors on the four data I/O pins, as shown in Figure 1. If a pair of data I/O pins (A<sub>N</sub>/B<sub>N</sub>) is not used, both pins should be tied to GND (or both to V<sub>CC</sub>). In this case, pull-down or pull-up resistors are not required. The recommended values for the pull-up resistors (R<sub>PU</sub>) are 1 kΩ to 10 kΩ. However, depending on the total bus capacitance, the pull-up resistor value can vary to meet the maximum I<sup>2</sup>C edge rate per the I<sup>2</sup>C specification (UM10204 rev. 03, June 19, 2007). For example, the maximum rise time (30% – 70%) during fast mode (400 kbit/s) is 300 ns. So, if bus capacitance is approaching the maximum 400 pF, lower the R<sub>PU</sub> value to keep the rise time below 300 ns (Fast Mode). Section 7.1 of the I<sup>2</sup>C specification provides an excellent guideline for pull-up resistor sizing.

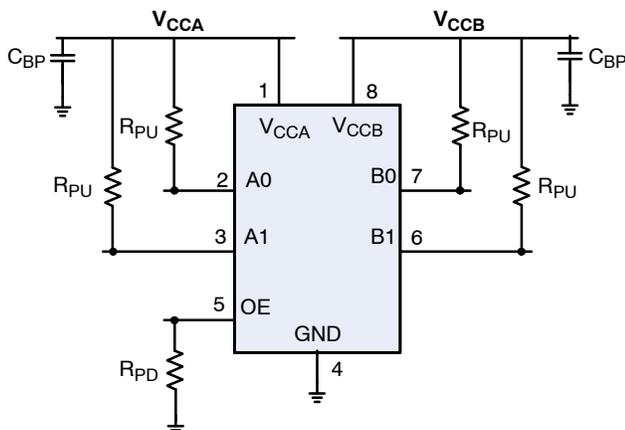


Figure 1. Application Circuit

### Theory of Operation

The FXMA2102 is designed for high-performance level shifting and buffer/repeating in an I<sup>2</sup>C application. As seen in Figure 2, each bi-directional channel contains two series N-passgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I<sup>2</sup>C application where auto-direction is a necessity.

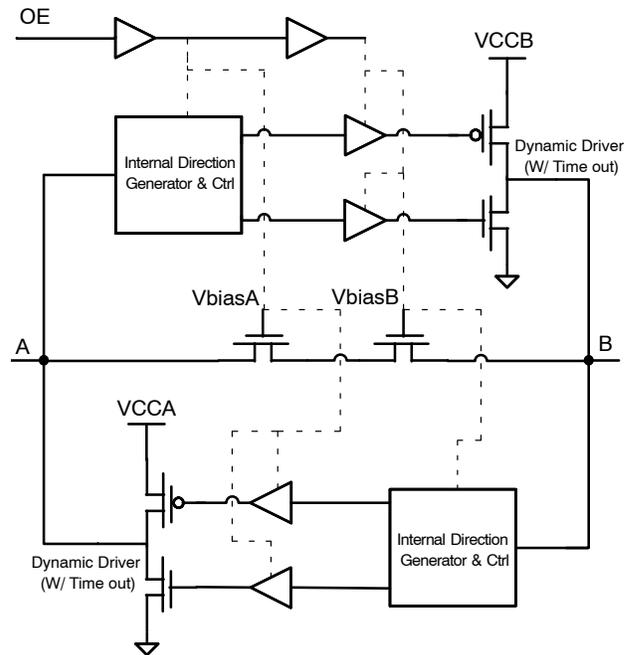


Figure 2. FXMA2102 Architecture

For example, during these three I<sup>2</sup>C protocol events:

- Clock stretching
- Slave acknowledgement: the slave's ACK bit (9<sup>th</sup> bit = 0) following a master's write bit (8<sup>th</sup> bit = 0)
- Clock synchronization and multi-master arbitration

The bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I<sup>2</sup>C translator between the master and slave in these examples, the I<sup>2</sup>C translator must change direction when both A and B ports are LOW. The N-passgates can accomplish this efficiently because, when both A and B ports are LOW, the N-passgates act as a low-resistive short between the two (A and B) ports.

Due to I<sup>2</sup>C's open-drain topology, I<sup>2</sup>C masters and slaves are not push/pull drivers. Logic LOWs are pulled down (Isink), while logic HIGHs are "let go" (tri-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant where R = R<sub>PU</sub> and C = the bus capacitance. If the FXMA2102 is attached

to the master in this example, say on the A port, and there is a slave on the B port, the N-passgates act as a low-resistive short between both ports until either of the port's  $V_{CC}/2$  thresholds are reached. After the RC time constant has reached the  $V_{CC}/2$  threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot of Figure 3. Effectively, there are two distinct slew rates to the rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports. This is because both the N-passgates are turned off. If a master or slave device pulls SCL or SDA LOW, that device's driver pulls down ( $I_{sink}$ ) SCL or SDA until the edge reaches the A or B port  $V_{CC}/2$  threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

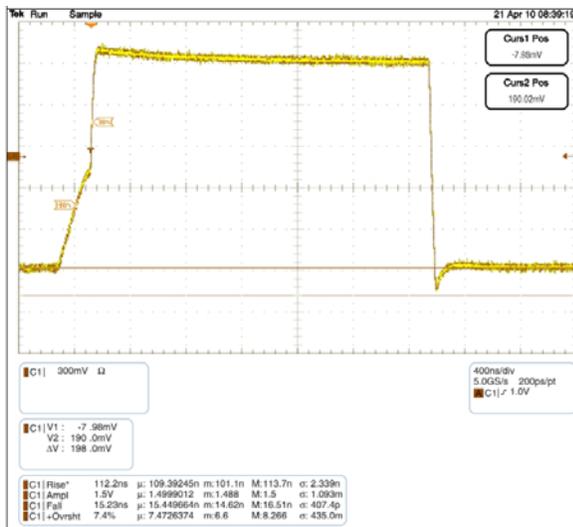


Figure 3. Waveform C: 600 pF,  $R_{PU} = 2.2 \text{ k}\Omega$

### Clock Stretching

Clock stretching allows a slave to hold SCL LOW, forcing the master to wait until the slave releases SCL. According to the I<sup>2</sup>C specification, there is not a maximum time limit for how long SCL can be held LOW by a slave; however, most

masters provide a time-out algorithm during clock stretching so the I<sup>2</sup>C bus does not hang.

Clock stretching occurs in many smart-phone applications. For example, there may be an I<sup>2</sup>C master host processor that has requested the current GPS coordinates from a GPS slave. Meanwhile, the GPS device may have stored the last GPS coordinates in an internal register from a previous master request. The master does not want the previously stored GPS coordinates. The master wants real-time GPS coordinates. This means that the GPS slave device must produce the new coordinates. This effort may take milliseconds. Therefore, the GPS slave must force the master to wait until it is ready to service the request for new GPS coordinates.

The interesting aspect of clock stretching for an I<sup>2</sup>C translator application configuration like Figure 4 is that the translator's auto-direction circuitry must change direction when both sides of SCL are LOW. The FXMA2102 tested 100% compliant during I<sup>2</sup>C clock stretching.

### Multi-Master

The I<sup>2</sup>C specification also describes protocol timing requirements for "clock synchronization and arbitration" when multiple I<sup>2</sup>C masters attempt to transmit on an idle I<sup>2</sup>C bus at the same time. The FXMA2102 has been tested and verified in a multi-master application.

### Buffer / Repeater Performance

The FXMA2102 dynamic drivers have current sourcing capability and can drive a 400 pF capacitive bus. This is beneficial when an I<sup>2</sup>C buffer/repeater is required. The I<sup>2</sup>C specification stipulates a maximum bus capacitance of 400 pF. If an I<sup>2</sup>C segment exceeds 400 pF, an I<sup>2</sup>C buffer/repeater is required to split the segment into two segments, each of which is less than 400 pF. Figure 3 is a scope shot of an FXMA2102 driving a lumped load of 600 pF. Notice the (30% - 70%) rise time is only 112 ns ( $R_{PU} = 2.2 \text{ k}\Omega$ ). This is well below the maximum rise time of 300 ns. So, not only does the FXMA2102 drive 400 pF, but it also provides headroom below the I<sup>2</sup>C specification maximum rise time of 300 ns.

### $V_{OL}$ vs. $V_{IL}$ & $I_{OL}$

The I<sup>2</sup>C specification mandates a maximum  $V_{IL}$  (assuming a minimum  $I_{OL}$  of 3 mA) of  $V_{CC} \cdot 0.3$  and a maximum  $V_{OL}$  of 0.4 V. If, for example (see Figure 4), there is a master on the A port of an I<sup>2</sup>C translator with a  $V_{CC}$  of 1.65 V and a slave on the I<sup>2</sup>C translator B port with a  $V_{CC}$  of 3.3 V, the maximum  $V_{IL}$  of the master is  $(1.65 \text{ V} \times 0.3)$  495 mV.

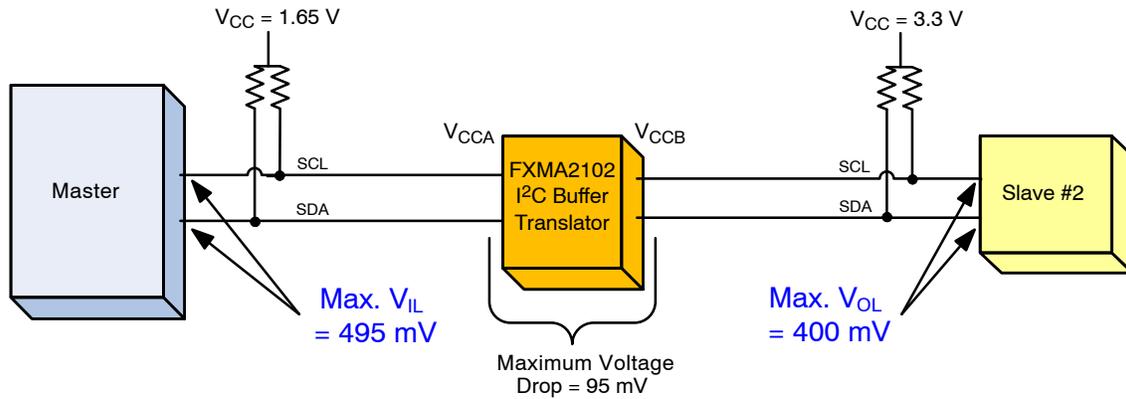


Figure 4. Clock Stretching

The slave in the Figure 4 example could legally transmit a valid logic LOW of 0.4 V to the master. If the I<sup>2</sup>C translator’s channel resistance is too high, the voltage drop across the translator could present a V<sub>IL</sub> to master > 495 mV. To complicate matters, the I<sup>2</sup>C specification states that 6 mA of I<sub>OL</sub> is recommended for bus capacitances approaching 400 pF. More I<sub>OL</sub> increases the voltage drop across the I<sup>2</sup>C translator. The I<sup>2</sup>C application benefits when I<sup>2</sup>C translators exhibit low V<sub>OL</sub> performance. Figure 5 depicts the typical FXMA2102 V<sub>OL</sub> performance, given a 0.4 V V<sub>IL</sub>.

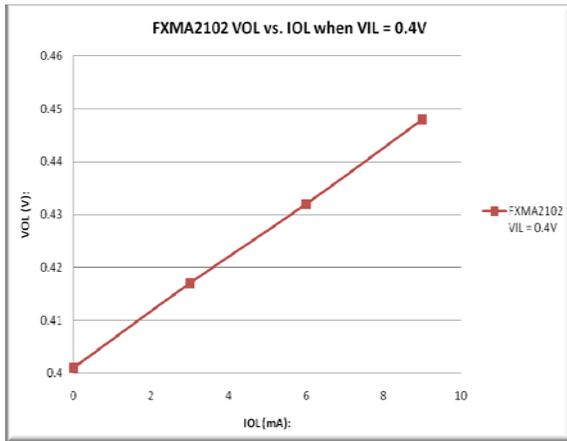


Figure 5. V<sub>OL</sub> vs. I<sub>OL</sub>

*Bus Clear*

The I<sup>2</sup>C specification defines the minimum SCL frequency of 0 Hz. Therefore, the SCL signal can legally be held LOW forever. However, this condition shuts down the I<sup>2</sup>C bus. The I<sup>2</sup>C specification refers to this condition as “Bus Clear.” In Figure 6, if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMA2102 passes the SCL stuck-LOW condition from slave 2 to slave 1 as well as the master. However, if the OE pin of the FXMA2102 is pulled LOW (disabled), both ports (A and B) of are in tri-state. This results in the FXMA2102 isolating slave #2 from the master and slave #1, allowing full communication between master and slave #1.

*Either V<sub>CC</sub> to GND*

If, in an application such as Figure 6, slave #2 is a camera that is suddenly removed from the I<sup>2</sup>C bus, resulting in V<sub>CCB</sub> transitioning from a valid V<sub>CC</sub> (1.65 V – 5.5 V) to 0 V, the FXMA2102 automatically forces SCL and SDA on both its A and B ports into tri-state. Once V<sub>CCB</sub> reaches 0 V, there is full I<sup>2</sup>C communication between the master and slave #1.

**I<sup>2</sup>C Bus Isolation**

FXMA2102 supports I<sup>2</sup>C bus isolation for these conditions:

- Bus isolation in the event of bus clear.
- Bus isolation in the event of either V<sub>CC</sub> going to ground.

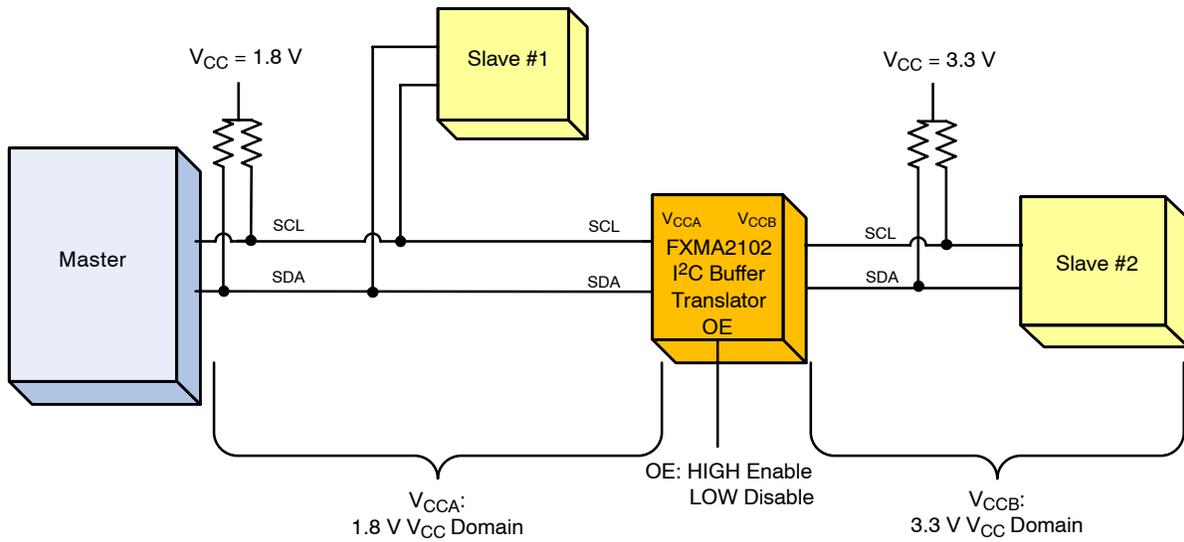


Figure 6. Bus Clear

**Power-Good Voltage**

Typically, if  $V_{CCA}$  or  $V_{CCB}$  are below 600 mV, the I<sup>2</sup>C signals (SDA and SCL) are tri-state on both the FXMA2102 A port and B port. OE is tied to  $V_{CCA}$ .

Typically, if  $V_{CCA}$  and  $V_{CCB}$  are above 600 mV, the I<sup>2</sup>C signals (SDA and SCL) are active on both the FXMA2102 A port and B port. OE is tied to  $V_{CCA}$ .

**Parallel I<sup>2</sup>C Voltage Segments**

Smart-phone applications are driving demand for a variety of mobile IC devices like accelerometers,

gyroscopes, compasses, GPS, proximity sensors, and temperature sensors. Many of these devices communicate with the mobile host processor via I<sup>2</sup>C, while most of these devices do not share a common  $V_{CC}$ . Therefore, to maintain proper I<sup>2</sup>C communication, the smart-phone architect must segment these individual I<sup>2</sup>C sensors into parallel voltage segments/domains where their respective  $V_{CC}$ s agree. Figure 7 illustrates this concept.

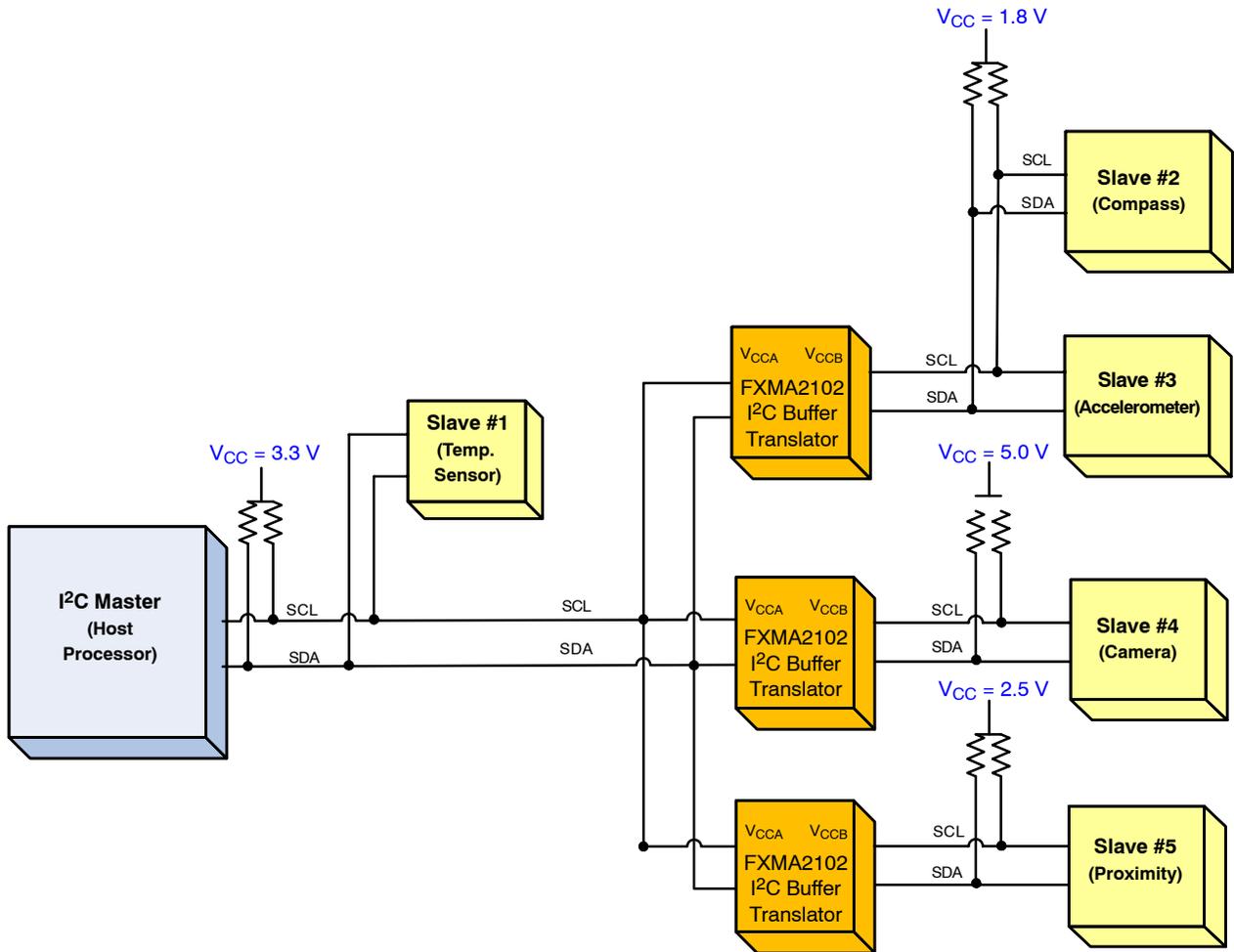


Figure 7. Three V<sub>CC</sub> Domain Segments in Parallel

Figure 7 depicts a hypothetical example of I<sup>2</sup>C V<sub>CC</sub> domain segmentation typical of today’s mobile smart-phone architectures. At the physical layer, multiple I<sup>2</sup>C voltage translators are placed in parallel to resolve V<sub>CC</sub> disagreement. Figure 7 illustrates three V<sub>CC</sub> domain segments in parallel, each of which is electrically connected to the V<sub>CCB</sub> sides of each I<sup>2</sup>C translator.

- I<sup>2</sup>C V<sub>CC</sub> Domain Segment #1: Slave #2 and Slave #3 at 1.8 V
- I<sup>2</sup>C V<sub>CC</sub> Domain Segment #2: Slave #4 at 5.0 V

- I<sup>2</sup>C V<sub>CC</sub> Domain Segment #3: Slave #2 at 2.5 V  
Meanwhile, the I<sup>2</sup>C master and slave #1 represent a fourth V<sub>CC</sub> domain segment at 3.3 V on the V<sub>CCA</sub> sides of the three I<sup>2</sup>C translators.

**RELATED DEVICES AND DATASHEETS**

onsemi offers other voltage level translators suitable for I<sup>2</sup>C-Bus and SMBus applications. Table 1 below shows the configurations that are available.

Table 1.

Device / Datasheet	Number of Channels	Integrated I/O Pull-Ups
<a href="#">FXMA2102</a>	2	n/a
<a href="#">FXMAR2102</a>	2	10 kΩ
<a href="#">FXMA2104</a>	4	n/a
<a href="#">FXMAR2104</a>	4	10 kΩ
NL5X4002 (Notes 1 and 2)	2	10 kΩ
NL5X4E02 (Note 1)	2	n/a

1. Please contact onsemi for more information.  
2. AEC-Q100 Qualified devices available.

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