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Designing a LED Driver Controlled by the NCL30486/88

AND90120/D

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APPLICATION NOTE

Description

This paper describes the key steps to design a LED driver controlled by the NCL30486/88. It gives hints on the components selection to obtain a good constant−voltage and constant−current regulation.

The process is illustrated by a practical 20−W, universal main application:

- Maximum output power: 20 W
- Input voltage range: 90 to 305 V rms
- Output voltage range: 20 to 40 V dc
- Output current: 500 mA

Introduction

The NCL30486 [1] and NCL30488 [2] are power−factor−corrected controllers with primary side constant voltage (CV) and constant current (CC) Control suitable for flyback, buck−boost or SEPIC. The NCL30486 is housed in an SOIC 10 package and provides analog dimming of the output current with two dedicated dimming control input pins ADIM and PDIM. The NCL30488 is housed in an SOIC 8 package and targets high−performance LED drivers. These controllers integrate a proprietary circuit for power factor correction and constant current control allowing achieving a power factor above 0.95 with a total harmonic distortion below 10% for universal mains input. The output current and the output voltage regulation are typically within ±2% for an input voltage varying from 85 V rms to 305 V rms. The current−mode, quasi−resonant architecture of these controllers optimizes the efficiency by turning on the MOSFET when the drain−source voltage is minimal (valley). The valley lockout and frequency foldback circuitry maintains high−efficiency performance in dimmed conditions or in light load during constant− voltage regulation.

In addition, the circuit contains a set of powerful protections to ensure a robust LED driver design [1]:

- Output Over Voltage Protection
- Cycle−by−cycle Peak Current Limit
- Winding and Output Diode Short Circuit Protection
- Output Short Circuit Protection
- V_{CC} pin Over Voltage Protection
- Floating/Short Pin Detection: the circuit can detect most of these situations. That is of great help to pass safety tests.

MAXIMUM DUTY−RATIO

The NCL30486 / 88 offer a board range of options. Among them, there are four selectable reference voltages for the constant current regulation: V_{REF} = 333 mV, V_{REF} = 250 mV, V_{REF} = 200 mV, V_{REF} = 143 mV. The reference voltage selection directly sets the duty−ratio limit. The 200 mV and 143 mV reference are suitable for boost converter operation.

Table 1 shows the output voltage range relationship as a function of the minimum input voltage for all voltage references options.

For V_{REF} = 333 mV, the duty−ratio is limited to 50% at the top of the lowest line sinusoid. For V_{REF} = 250 mV, the duty−ratio is limited to 64% at the top of the lowest line sinusoid.

Table 1. OUTPUT VOLTAGE RANGE OF CONVERTER

V_{REF}	Maximum Duty−Ratio at $V_{inLL,rms}$	Output Voltage Range for Non−isolated Converters (Note 1)	Output Voltage Range for Boost Converters (Note 1)	Output Voltage Range for Flyback Converters (Note 1)
333 mV	50%	$V_{out} + V_f \le \sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 2.1\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le \frac{n_s}{n_p}\sqrt{2}\ V_{inLL,rms}$
250 mV	64%	$V_{out} + V_f \le 1.8\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 2.8\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 1.8\frac{n_s}{n_p}\sqrt{2}\ V_{inLL,rms}$
200 mV	71%	$V_{out} + V_f \le 2.5\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 3.5\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 2.5\frac{n_s}{n_p}\sqrt{2}\ V_{inLL,rms}$
143 mV	79.6%	$V_{out} + V_f \le 3.9\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 4.9\sqrt{2}\ V_{inLL,rms}$	$V_{out} + V_f \le 3.9\frac{n_s}{n_p}\sqrt{2}\ V_{inLL,rms}$

1. $V_{inLL,rms}$ is the lowest line rms voltage (e.g. 85 V rms), V_f is the output diode forward voltage.

PRIMARY SIDE CONSTANT VOLTAGE OPERATION

In primary−side constant−voltage regulation, the output voltage is sensed via the auxiliary winding. Indeed, the auxiliary winding provides an image of the output voltage during the off−time of the power MOSFET. By sampling the auxiliary voltage knee (which represents the end of the core demagnetization) the controller is able to accurately control the output voltage.

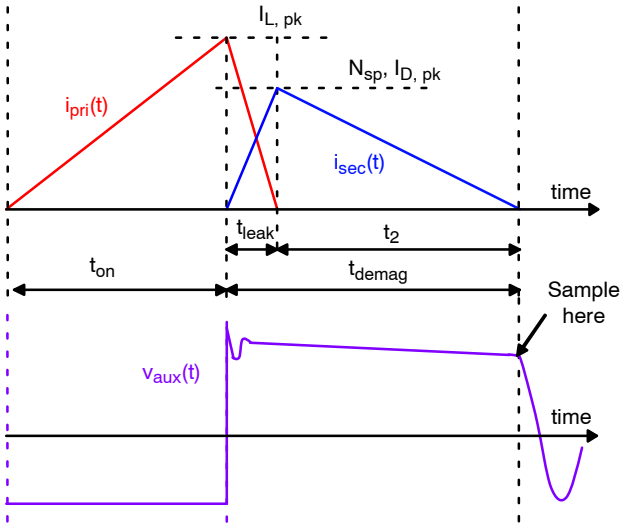

Figure 1. Idealized Waveforms of a Flyback Converter in DCM

Figure 1 illustrates the idealized waveforms of a flyback converter operated in discontinuous conduction mode (DCM). When the secondary current becomes null, the auxiliary winding voltage is sampled on ZCD pin:

$$V_{ZCD} = \frac{R_{ZCDL}}{R_{ZCDU} + R_{ZCDL}} \times \frac{N_{ap}}{N_{sp}} \times V_{out} \qquad \text{(eq. 1)}$$

Where:

- N_{ap} the auxiliary to primary turns ratio: $N_{ap} = N_a / N_p$ with N_a and N_p being respectively the auxiliary and primary turns,
- N_{sp} is the secondary to primary turns ratio: $N_{sp} = N_s / N_p$ with N_s being respectively the secondary turns,
- R_{ZCDU} is the upper resistor of the voltage divider at ZCD pin,
- R_{ZCDL} is the lower resistor of the voltage divider at ZCD pin.

The sampled voltage is applied to the negative input terminal of the operational transconductance amplifier (OTA) and compared to the internal precise reference voltage $V_{REF(CV)}$ (Figure 2). A voltage feedback V_{COMP} is then generated through the external components placed at the OTA output. This V_{COMP} is then internally used to modulate the reference voltage of the PFC loop. The reference voltage is modulated from 0% to 100% of V_{REF} to regulate the output voltage. The relationship between V_{COMP} and the internal current setpoint V_{REFX} is given by(Eq. 2):

$$V_{REFX} = 0.323\, V_{COMP} - 0.2907 \qquad \text{(eq. 2)}$$

The resistor divider (R_{ZCDU}, R_{ZCDL}) from the auxiliary winding to the ZCD pin selects the output voltage nominal value:

$$V_{REF(CV)} = \frac{R_{ZCDL}}{R_{ZCDU} + R_{ZCDL}} \times \frac{N_{ap}}{N_{sp}} \times V_{out} \qquad \text{(eq. 3)}$$

There are several ways to calculate R_{ZCDU} and R_{ZCDL}. To decrease the resistor divider current consumption and keep the *RC* time constant at ZCD pin small, it is better to choose R_{ZCDU} in the range of 10 kΩ to 82 kΩ..

Then R_{ZCDL} value can be calculated with:

$$R_{ZCDL} = \frac{R_{ZCDU} \times V_{REF(CV)}}{\frac{N_{ap}}{N_{sp}} \times V_{out} - V_{REF(CV)}} \qquad \text{(eq. 4)}$$

For the 20−W LED driver board, a 43−kΩ R_{ZCDU} resistance was chosen. Thus, R_{ZCDL} value is:

$$R_{ZCDL} = \frac{43k \times 3.5}{\frac{0.25}{0.469}\, 40 - 3.5} = 8.44\ k\Omega \qquad \text{(eq. 5)}$$

Finally, an 8.2−kΩ resistor was chosen for R_{ZCDL}.

The power factor correction operation induces larges variations of the MOSFET off−time. Particularly around the input voltage zero crossing, the demagnetization time is very small and the auxiliary winding voltage cannot be sampled correctly. For this reason, the sampling is disabled whenever the input sine waveform is below 50 V at low line or bellow 105 V at high line. There a 5−V hysteresis on the comparators. In the same way, the sampling is disabled during the ZCD blanking to avoid false reading output voltage caused by the leakage inductance at the power switch turn off. Thus, the power supply designer must ensure that $t_{demag} > 2$ µs when V_{in} is above 55 V for heavy to medium output load and $t_{demag} > 1.3$ µs for light load conditions.

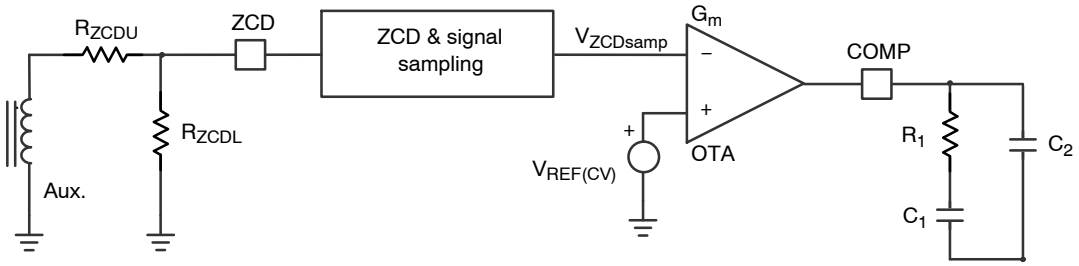

Figure 2. Constant Voltage Feedback Circuit

TRANSFORMER SELECTION FOR GOOD CV REGULATION

The application note AND9714 [2] details how to select the turns ratio and primary inductance for the NCL30386/88.

COMP PIN

The COMP pin is the output of the OTA used for the constant voltage regulation. Figure 2 shows the recommended compensation scheme. The components R_1, C_1 and C_2 form a type 2 compensator (an origin pole plus a pole / zero pair) with the OTA. The application note AND9714 [2] describe in details how to calculate the values of these components. It is also possible to use the Mathcad® spreadsheet [3] to calculate automatically R_1, C_1 and C_2.

HV PIN

The HV pin senses the input voltage for the power factor correction circuit and for the line over voltage protection. This pin also provides the current to charge V_{CC} capacitor at startup.

At high line (above 305 V rms) the power dissipated by the HV startup in case of fault becomes high. Indeed, in case of fault, the NCL30486/88 is directly supplied by the HV rail. The current flowing through the HV startup will heat the controller. It is highly recommended adding enough copper around the controller to decrease the thermal resistance $R_{\theta JA}$ of the controller.

Adding a minimum pad area of 215 mm^2 of 35 μm copper (1 oz) drops the $R_{\theta JA}$ to around 120°C/W (no air flow, $R_{\theta JA}$ measured at ADIM pin).

The PCB layout shown in Figure 3 is a layout example to achieve low $R_{\theta JA}$. The various SMD components connected to the pins of the controllers are placed on the bottom side of the board (red color for bottom side copper). Small copper pads are drawn around ADIM, GND and HV pin:

- GND pad: 7 mm
- ADIM pad: 6 mm^2
- HV pad: 3 mm^2

A ground plane of approximately 10 mm*20 mm is placed on the top side (blue color) and connected to GND pin of the controller.

3 additional via placed under the controller help evacuating the heat.

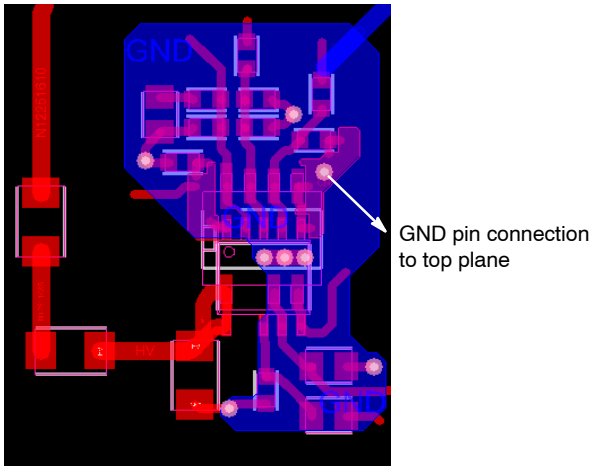

Figure 3. PCB Layout Example

A resistor R_{HV} can also be placed in series with HV pin to decrease the power dissipation. This resistor cannot be high because the controller uses the HV pin voltage information for the regulation of the output current. When the HV current source is on, there is a voltage drop on the HV pin if a resistor is used. If there is a too big difference between the real input voltage and the voltage read by the controller on the HV pin, the output current will overshoot during startup, if the controller fails to start in one attempt.

In the same way, for controller versions having the line over voltage protection (line OVP), the voltage drop at HV pin generated by the resistor could release the protection prematurely.

To avoid all these potential problems, we recommend having R_{HV} between 1 kΩ to 3.3 kΩ when using version A controllers. In version B, the line OVP timer has been extended and the voltage drop generated by R_{HV} when the HV current source turns on is ignored by the controller algorithm. Thus, higher resistors values can be used, such as 10 kΩ for example.

HV Startup Power Dissipation Calculation

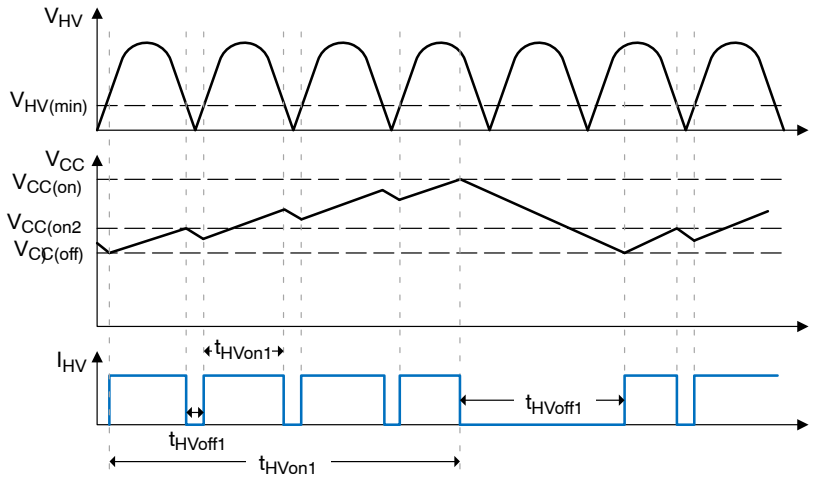

Figure 4. HV Startup Waveforms

When the voltage on HV pin is below $V_{HV(min)}$, the HV startup does not deliver current. The current drawn by the HV startup is $I_{HV(start2)}$ + I_{CC1} (parameters from NCL30486/NCL30488 datasheets).

$$\frac{t_{HVoff1}}{2} = \frac{1}{2\pi F_{line}} \sin^{-1}\left(\frac{V_{HVmin} + R_{HV} I_{HV}}{\sqrt{2}\, V_{in,\,rms}}\right) \quad \text{(eq. 6)}$$

$$t_{HVon1} = \frac{1}{2F_{line}} - t_{HVoff1} \quad \text{(eq. 7)}$$

Where:

- F_{line} is the mains frequency (50 Hz or 60 Hz),
- $V_{in,\,rms}$ is the rms value of the input voltage,
- I_{HV} is the current drawn by the HV startup: $I_{HV} = I_{HV(start2)} + I_{CC1}$.

We can then calculate V_{CC} capacitor voltage increase and decrease per half line cycle:

$$\Delta V_{CC,\,inc} = \frac{I_{HV(start2)}\, t_{HVon1}}{C_{VCC}} \quad \text{(eq. 8)}$$

$$\Delta V_{CC,\,dec} = \frac{I_{HV(start2)}\, t_{HVoff1}}{C_{VCC}} \quad \text{(eq. 9)}$$

HV Startup Junction Temperature Calculation

To calculate the junction temperature increase of the controller, we need the steady state thermal resistance of the controller $R_{\theta JA}$ which depends on anything the controller is attached to: PCB size, copper area, airflow.

And deduce the time needed to charge VCC capacitor t_{HVon2} and its discharge duration t_{HVoff2}:

$$t_{HHVon2} = \frac{1}{2F_{line}}\left(\frac{V_{CCon} - V_{CCoff}}{\Delta V_{CC,\,inc} - \Delta V_{CC,\,dec}}\right) \quad \text{(eq. 10)}$$

$$t_{HHVoff2} = \frac{C_{VCC}\left(V_{CCon} - V_{CCoff}\right)}{I_{CC1}} \quad \text{(eq. 11)}$$

The power dissipated by the HV startup over one half line cycle is:

$$P_{HVpeak} = 2F_{line} \int_{0.5t_{HVoff1}}^{0.5t_{HVoff1} + t_{HVon1}} I_{HV}\left(\sqrt{2}V_{in,\,rms}\, \sin(2\pi F_{line} t) - R_{HV} I_{HV}\right) dt \quad \text{(eq. 12)}$$

The average power dissipated by the HV startup is:

$$P_{HV,\,avg} = \frac{t_{HVon2}}{t_{HVon2} + t_{HVoff2}}\, P_{HV,\,peak} \quad \text{(eq. 13)}$$

We also need the thermal transient response $R(t)$ of the package. This transient response is specific of the controller die in the package.

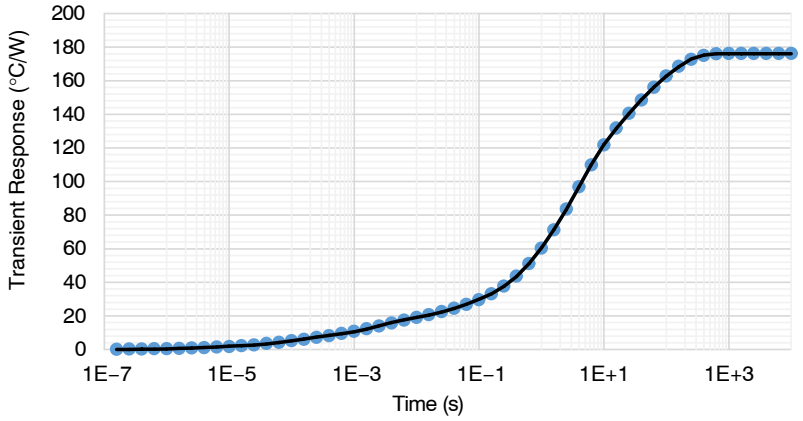

Figure 5. R(t) Curve of NCL30486

Roughly:
- for a 25−ms V_{CC} capacitor charging duration (t_{HVon2} = 25 ms for C_{VCC} = 10 μF), $R(t)$ = 21°C/W
- for a 50−ms for a 25−ms V_{CC} capacitor charging duration (t_{HVon2} = 50 ms for C_{VCC} = 22 μF), $R(t)$ = 28°C/W

Finally, the junction temperature at the HV startup device can be calculated with:

$$\Delta T_j = R_{\theta JA} P_{HV,\,avg} + \left(P_{HV,\,peak} - P_{HV,\,avg}\right) R(t) \quad \text{(eq. 14)}$$

$$T_j = T_A + \Delta T_j \quad \text{(eq. 15)}$$

V_{CC} Capacitor

The selection of V_{CC} capacitor value is covered in the application note AND9714 [2].

In addition, as shown by the R(t) curve above, V_{CC} capacitor must not be too big to avoid increasing the junction temperature of the controller in case of fault at high input voltage (above 305 V rms).

Thus, for application requiring input voltages above 325 V rms, we recommend to keep V_{CC} capacitor between 4.7 μF to 22 μF.

STANDBY MODE (NCL3048X B)

In order to decrease the power consumption of the converter when no output load is connected to its output, the NCL30486/88 B versions features a standby mode.

In standby mode, the current consumption of the controller is reduced to I_{CC4} (1.7 mA typ.) The peak current is frozen to a fixed value $V_{CS(STBY)}$ (27% or below of V_{ILIMIT}) and the controller adjust the switching frequency, more specifically the dead−time (DT) to keep the output voltage regulated (pink curve in Figure 6). The regulation of V_{out} is based on COMP pin voltage varying between 700 mV to 913 mV. Standby mode is entered if V_{COMP} < 895 mV, V_{COMP} decreasing and exit if V_{COMP} > 913 mV, V_{COMP} increasing.

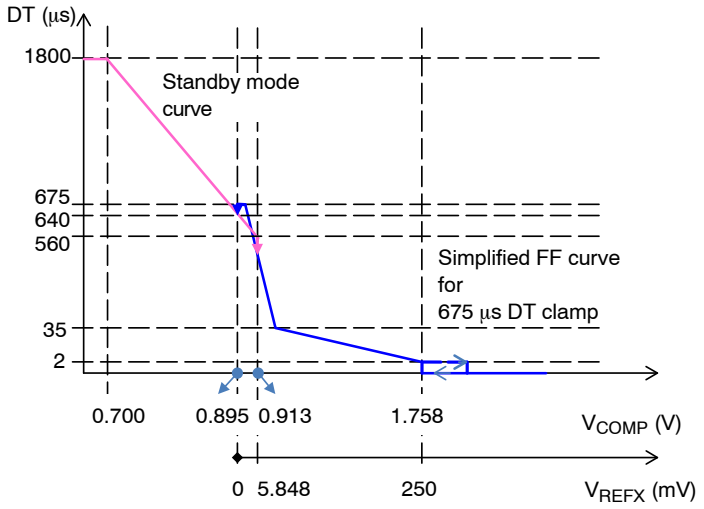

Figure 6. Dead−time Setpoint As a Function of V_{COMP} for 675 μs Dead−time Clamp

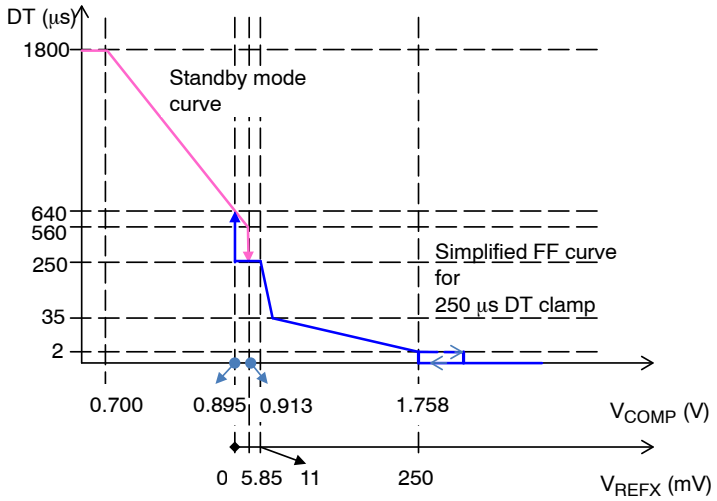

Figure 7. Dead−time Setpoint As a Function of V_{COMP} for 250 μs Dead−time Clamp

DIMMING WITH THE NCL30486

The NCL30486 features 2 dimming pins for an improved dimming control: ADIM and PDIM pin.

Dimming with ADIM

The ADIM pin receives an analog signal varying from $V_{ADIM100}$ to $V_{ADIM(MIN)}$ and translate this signal to vary the reference voltage for constant current regulation from 100% V_{REF} to $V_{DIM(clamp)}$. There are 4 options for the minimum dimming value $V_{DIM(clamp)}$:

- $V_{DIM(clamp)} = 0\% V_{REF}$ (meaning there is no clamp)
- $V_{DIM(clamp)} = 1\% V_{REF}$
- $V_{DIM(clamp)} = 5\% V_{REF}$
- $V_{DIM(clamp)} = 8\% V_{REF}$

The NCL30486 also features an option to select the dimming curve shape:

- For linear dimming, select L option
- For square dimming, select S option

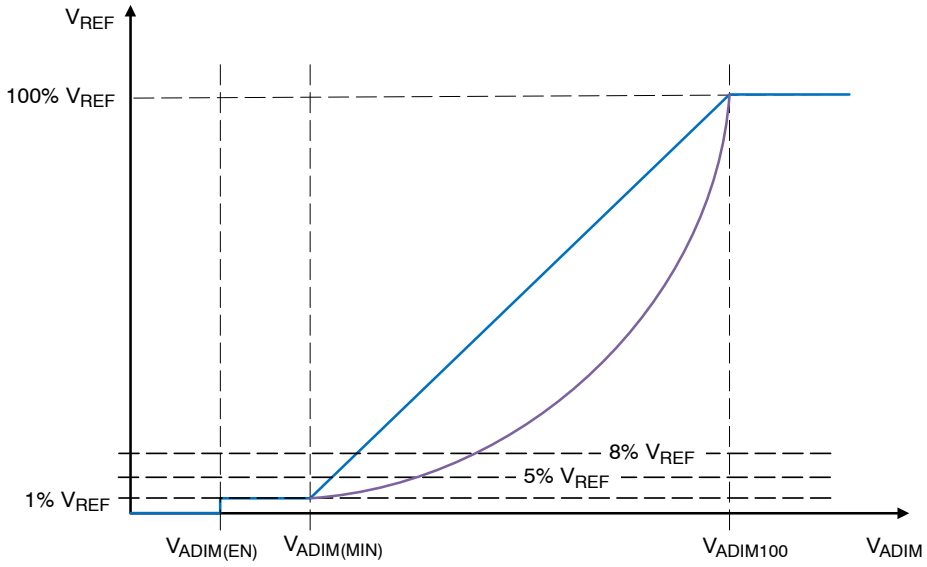

Figure 8. NCL30486 Dimming Curves Options

Dimming with PDIM

The PDIM pin receives a pulse width modulated (PWM) signal and measures its duty ratio. The duty ratio is then directly applied as the output current setpoint. For example, if the duty ratio of the PWM signal is 10%, then we have V_{REFX} = 10% V_{REF}. More precisely, the controller extracts the duty cycle by measuring the current inside PDIM pin which is directly the optocoupler collector current.

At startup, if the PDIM pin is left open, the controller delivers 100% of I_{out}. If the pin is pulled down or if the low state duration of the PWM signal is less than 10 μs, the controller is disabled.

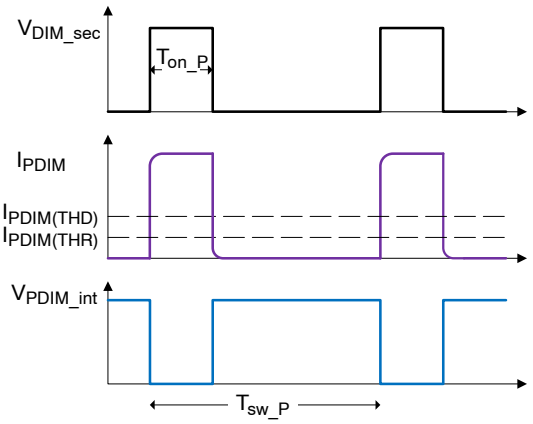

Figure 9. PDIM Signals

Please note that for PDIM pin, the output current is varied in an analog way even if the dimming signal is digital.

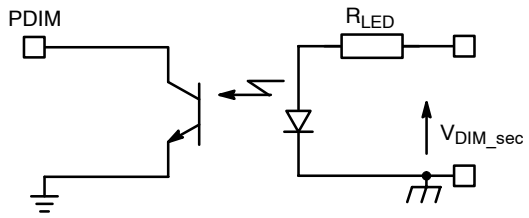

Figure 10. Optocoupler on PDIM Pin

For a good dimming resolution, it is recommended to use dimming signal frequency between 200 Hz to 333 Hz.

Figure 8 shows the signal applied on the optocoupler LED in black, the current in PDIM in purple and the internal dimming signal V_{PDIM_int}. Practically, the internal dimming signal is inverted, with respect to the signal applied on the optocoupler LED, so the controller actually measures the off−time of the PWM signal. The internal V_{REFX} setpoint is:

$$V_{REFX} = 1 - \frac{T_{on\_P}}{T_{SW\_P}} \qquad \text{(eq. 16)}$$

For correct measurement of the dimming signal duty−cycle, the current drawn from PDIM in must be above $I_{PDIM(THD)}$.

With PDIM, the output current varies between 0 to 100% if the dimming duty−cycle varies from 0% to 93%. The NCL30486 set 100% of output current when the duty−cycle of the signal applied on PDIM is above 93%. Figure 11 shows the dimming curve with PDIM for a 20−W LED driver where the maximum output current is 500 mA.

PDIM Dimming Frequency

For good dimming accuracy and low flicker, the PWM dimming frequency must be below 1 kHz. The best results are obtained with a dimming frequency around 250 Hz. The NCL30486B incorporates digital circuitry achieving very low flicker. The short−term flicker severity is typically equal or below 0.3 for the whole dimming range.

R_{LED} Setting

For a correct detection of the rising edge and falling edge of the PWM dimming signal, the current drawn out of PDIM must be above $I_{PDIM(THD)}$. Given that the optocoupler current transfer ratio drops with temperature and aging, it is better to set the collector current high, such that at 25°C ambient temperature, the collector current is near the current capability limit of PDIM. PDIM pin feature a cascode circuit for connecting the optocoupler transistor. Its current capability is typically 1.2 mA.

If we set 500 μA as the target collector current at 25°C, we can calculate R_{LED} with:

$$R_{LED} = CTR \frac{V_{DIM\_sec} - V_{opto\_LED}}{I_{opto\_C}} \qquad \text{(eq. 17)}$$

Where:

- I_{opto_C} is the target collector current at 25°C: 500 μA,
- V_{opto_LED} is the forward drop voltage of the optocoupler LED: $V_{opto\_LED} \approx 0.9$ to 1 V,
- CTR is the current transfer ratio of the optocoupler.

It is important to note that in case of fault, the optocoupler current will be supplied directly from the HV startup and this will increase the power dissipation of the controller at high line.

PDIM Pin Capacitor / Resistor

As the controller reads the optocoupler collector current through PDIM pin, adding a capacitor on this pin will divert a part of the optocoupler current. Thus, it is recommended to keep the capacitor on PDIM pin small (if the power supply designer really wants to use one). The PDIM capacitor must not exceed 100 pF. In the same way, adding an *RC* filter on PDIM pin will delay the rising and falling edge detection of the dimming signal, resulting in a less−precise dimming setpoint, particularly at low dimming. Thus, if a *RC* filter must be used on this pin, it is recommended to keep its time constant small (less than 1 μs).

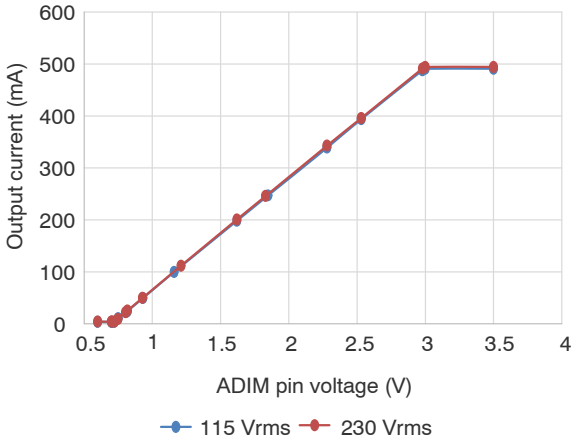

Figure 11. Output Current Dimming with ADIM, 20−W LED Driver

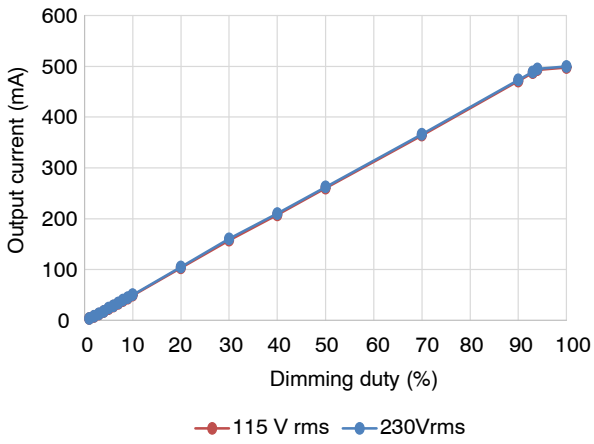

Figure 12. Output Current Dimming with PDIM, 20−W LED Driver

DIMMING CV MODE (OR ANOTHER STANDBY MODE)

The dimming CV mode allows supplying a microcontroller connected to a secondary winding of the flyback transformer (multiple secondary) at min dimming. In dimming CV mode, the controller operates in constant voltage mode with a new setpoint is lower than that of the normal constant voltage mode. This mode is entered when $V_{ADIM} < V_{DIM(EN)}$ or when the on−time (internal) of PDIM signal is below 10 μs during 15 ms. In this mode, a current source (I_{ZCDdim}) is applied on ZCD pin during the demagnetization time t_{demag} only in order to force the controller to regulate the output voltage to a lower setpoint. This new setpoint is adjusted by selecting the ZCD resistors.

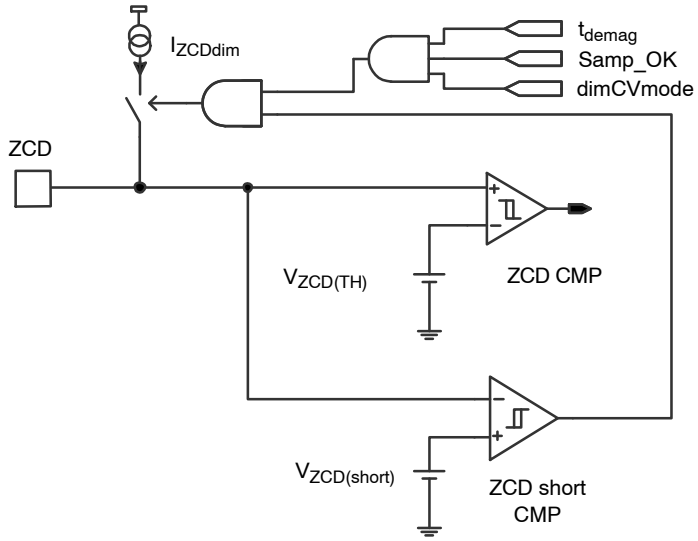

Figure 13. ZCD Pin Current Source for Dimming CV Mode

The ZCD pin resistors for dim CV mode output voltage setpoint can be calculated as follows:

$$R_{ZCDL} = \frac{V_{REFCV}\frac{N_{ap}}{N_{sp}}\left(V_{out,\,max} - V_{out,\,dimCV}\right)}{I_{ZCDdim}\left(\frac{N_{ap}}{N_{sp}}V_{out,\,max} - V_{REFCV}\right)} \quad \text{(eq. 18)}$$

$$R_{ZCDU} = R_{ZCDL}\frac{\left(\frac{N_{ap}}{N_{sp}}V_{out,\,max} - 1\right)}{V_{REFCV}} \quad \text{(eq. 19)}$$

Where:

I_{ZCDdim} is the current out of ZCD pin in dim CV mode (170 μA typ.),

$V_{out,max}$ is the output voltage in constant voltage mode when dim CV mode is off,

$V_{out,dimCV}$ is the output voltage setpoin in dim CV mode: $V_{out,dimCV} < V_{out,max}$

If we choose 22 V as the target output voltage in dim CV mode ($V_{out,dimCV}$ = 22 V), with $V_{out,max}$ = 40 V:

$$R_{ZCDL} = \frac{3.5 \times \frac{0.25}{0.469}(40 - 22)}{170 \times 10^{-6}\left(\frac{0.25}{0.469}\,40 - 3.5\right)} = 11.08\ k\Omega \quad \text{(eq. 20)}$$

$$R_{ZCDU} = 11080\frac{\left(\frac{0.25}{0.469}\,40 - 1\right)}{3.5} = 56.44\ k\Omega \quad \text{(eq. 21)}$$

During dimCV mode, V_{REFX} excursion is limited to the dimming clamp value by default:

- 1% V_{REF} if the dimming clamp is 0% or 1%
- 5% V_{REF} if the dimming clamp is at 5%
- 8% V_{REF} if the dimming clamp is at 8%

In order to increase the power delivered by the converter in dim CV mode, there is a programmable option to limit V_{REFX} excursion to twice the dimming clamp value. In this case:

- 2% V_{REF} if the dimming clamp is 0% or 1%
- 10% V_{REF} if the dimming clamp is at 5%
- 16% V_{REF} if the dimming clamp is at 8%

The dimming CV mode is available on NCL30486 B version only.

PROTECTIONS

The NCL30486/88 circuit contains a set of powerful protections to ensure a robust LED driver design:

- Output Over Voltage Protection (slow OVP, fast OVP)
- Winding and Output Diode Short Circuit Protection
- Output Short Circuit Protection
- V_{CC} pin Over Voltage Protection
- Floating/Short Pin Detection

For detailed operation of these protections, the power supply designer can refer to the application note AND9714 [2].

CONCLUSION

This application note has shown the steps to design a LED driver controlled by the NCL30486 and the NCL30488, A and B versions. This new family of controllers provides a very good regulation of the output current / voltage from the primary side of a flyback controller while maintaining a good power factor with low total harmonic distortion. For more information about the performances of these controllers, refer to [5] and [6].

REFERENCES

[1] NCL30486 Datasheet, NCL30488 Datasheet, http://www.onsemi.com/

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[3] NCL3048x Compensation spreadsheet, https://www.onsemi.com/support/design−resources/tools?rpn=NCL30486

[4] AND9200, 4 Key Steps to Design a NCL30088−Controlled LED Driver, Joel Turchi, http://www.onsemi.com/pub/Collateral/AND9200−D.PDF

[5] NCL30486LED1GEVB User Manual Microsoft Word – NCL30486LED1GEVB User Manual 31Jan20 (onsemi.com)

[6] AND90015, Secondary Side Regulated LED Driver with the NCL30488 AND90015 – Secondary Side Regulated LED Driver with the NCL30488)onsemi.com)

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