

NIS(V)3071 PCB Design on Thermal Performance Considerations

AND90246/D

Introduction

The design of PCB thermal properties are important factors for designing in any eFuse, including the NIS(V)3071 which can deliver up to 10 A of continuous current per device. There are two modes of operation of the eFuse to consider when designing the PCB thermals, the soft start turn on period and the steady state operating conditions. During soft start turn on the short-term power dissipation on the e-Fuse can be up to several tens of Watts and the steady state operation can be several Watts. This document will describe the performance advantages of using multi layer PCBs to dissipate heat from the device by comparing four and two layer boards. Figure 1 shows a two layer PCB and Figure 2 shows a four layer PCB with the same area of 2000 sqmm.

A comparison of the thermal parameters of both PCBs under the same conditions is described below. The linear temperature curve of the ESD structure on the FAULT pin was used to measure the junction temperature. The device is driven at an input voltage $V_{in} = 12\text{ V}$ with no load, at which the temperature characterization of the ESD structures on both measured boards were performed with a current of 1 mA while sweeping the temperature using Temptronic X-Stream 4300. The circuit diagram for this temperature characterization is shown in Figure 3. Temp. Characterization Setup.

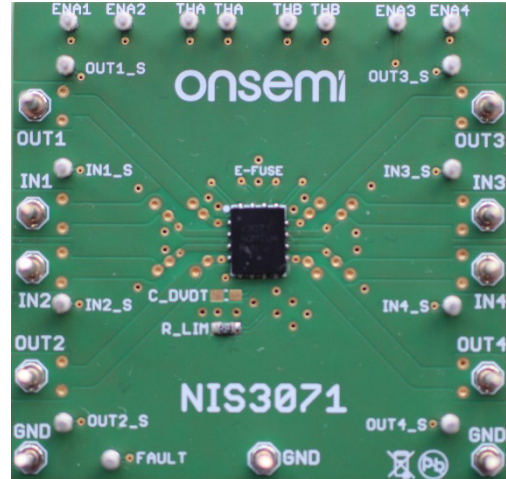


Figure 1. Two Layer PCB

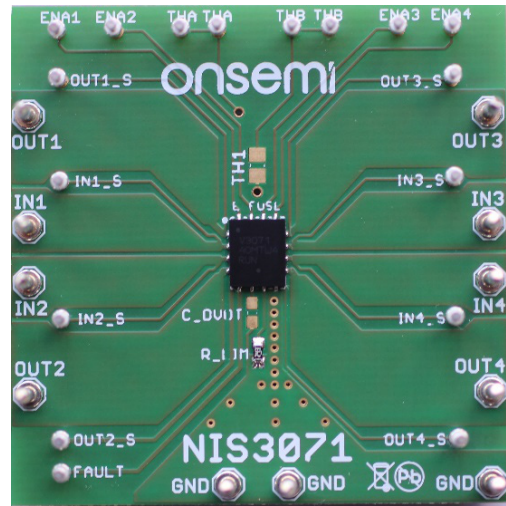


Figure 2. Four Layer PCB

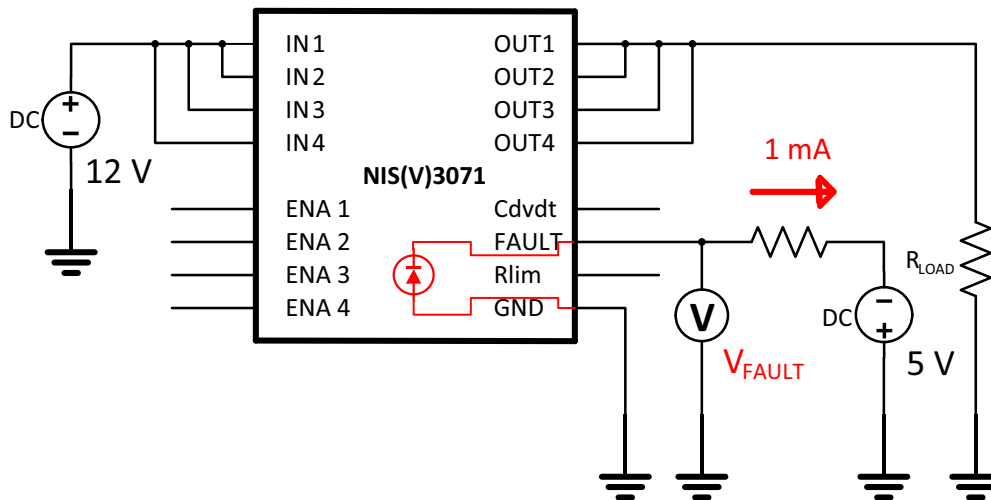


Figure 3. Temp. Characterization Setup

The voltage on both tested boards of the ESD structure in the temperature range from 30°C to 150°C is shown in the graph Figure 4. Thermal Characterization.

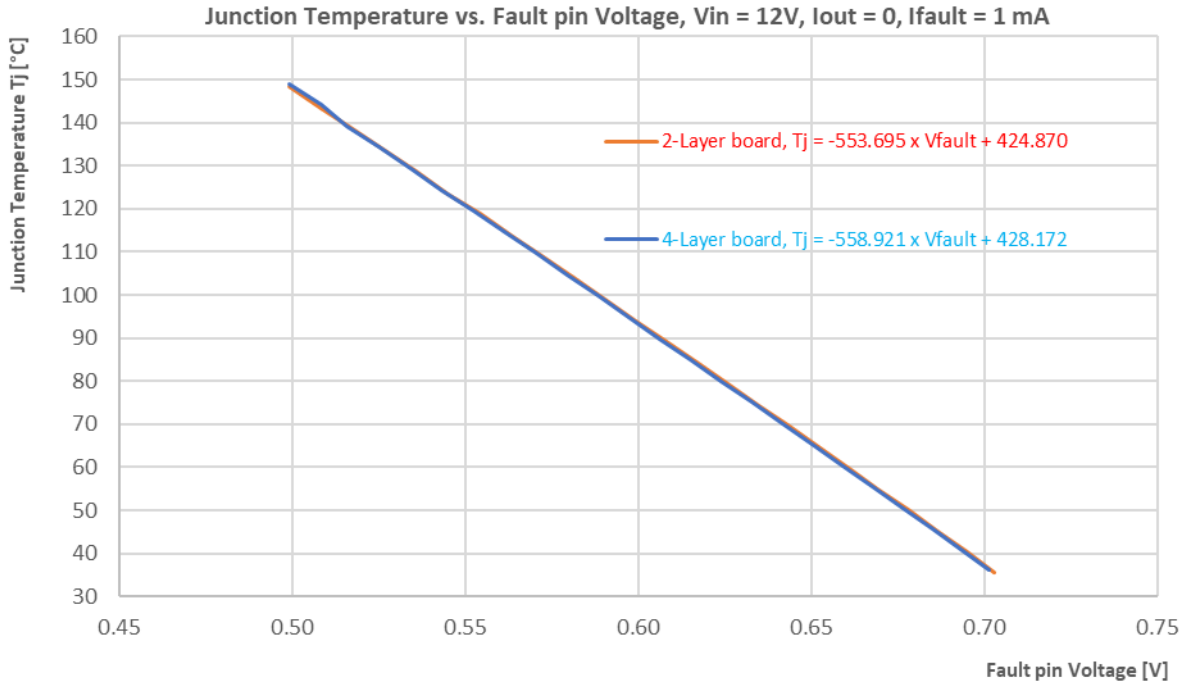


Figure 4. Thermal Characterization

With a supply voltage of $V_{in} = 12\text{ V}$, the output current of all four channels connected in parallel was set so that the power dissipation on both tested eFuse PCBs is set to exactly 1 W.

Table 1. shows the voltage on the ESD structure of the FAULT pin at the same current through this structure of 1 mA for both tested PCBs. From these voltages, the

Junction Temperature on each board is calculated according to the formulas shown in Figure 4. The measurement was taken under natural air convection at the ambient temperature of $T_a = 23^\circ\text{C}$. The values of Junction to Ambient Thermal Resistance (R_{thja}) for two-layer and four-layer PCB are given by the equation below.

$$R_{thja} = (T_j - T_a) / P_d \text{ [}^\circ\text{C/W]}$$

Table 1.

Board	V_{in} [V]	I_{out} [A]	$V_{in}-V_{out}$ [mV]	R_{dson} [mΩ]	P_d [W]	$-V_{fault}$ [mV]	T_j [°C]	T_a [°C]	R_{thja} [°C/W]
4-Layer	12.00	6.84	149.22	21.82	1.02	636.16	72.61	23.04	48.57
2-Layer	12.00	6.09	165.11	27.09	1.01	615.16	84.26	23.18	60.71

Figure 5. Thermal camera shows the temperature distribution for both compared PCBs. A four-layer PCB has a 12 °C/W lower thermal resistance than a two-layer PCB with the same area. The temperature T_j can also be calculated from the change in R_{dson} , but the

characterization of this dependence at an output current of around 6 A is complicated by self-heating and the dependence of R_{dson} on temperature vs. the output current is not linear.

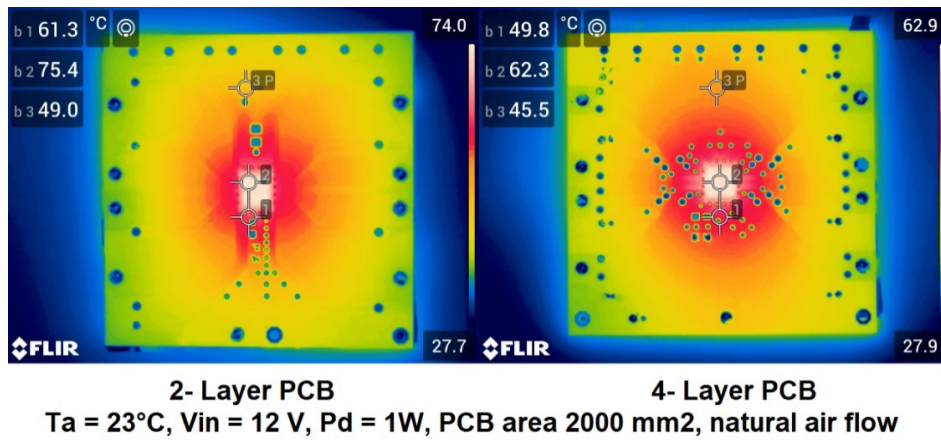


Figure 5. Thermal Camera

In the appendix is a complete description and stack up of both PCBs compared above.

Solderability Guidelines

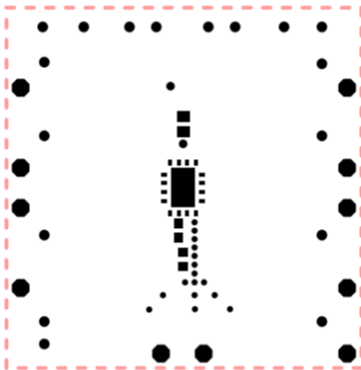
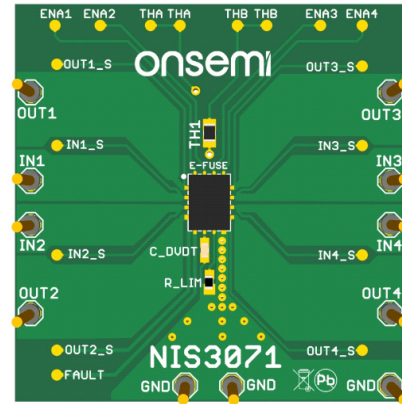
When soldering the NIV3071 device, we recommend following IPC-7527 stencil and soldering guidelines. In

certain applications where rigid multi-layer PCBs are required it is recommended to use a high reliability solder paste. The high reliability solder paste will help ensure the mechanical integrity of the solder joint during board level reliability temperature cycling tests.

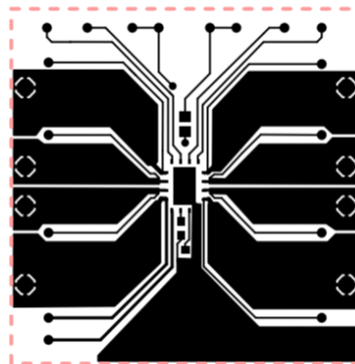
APPENDIX

Two Layer PCB Design

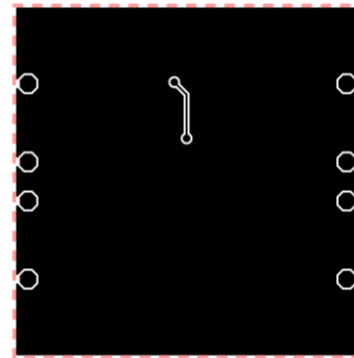
Cu layer	Material	Thick [μm]	
	Solder mask	20	1
L1	Copper	35+25 Plt	2
	Rigid laminate	1430	
L2	Copper	35+25 Plt	3
	Solder mask	20	4



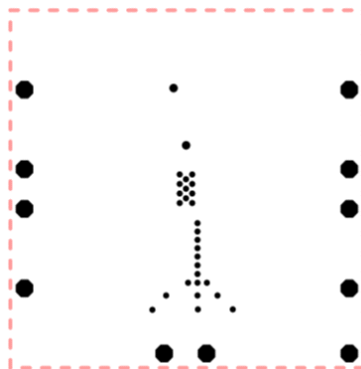
1. Top Solder mask



2. Copper L1



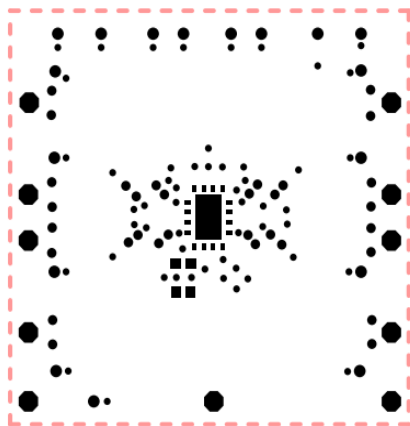
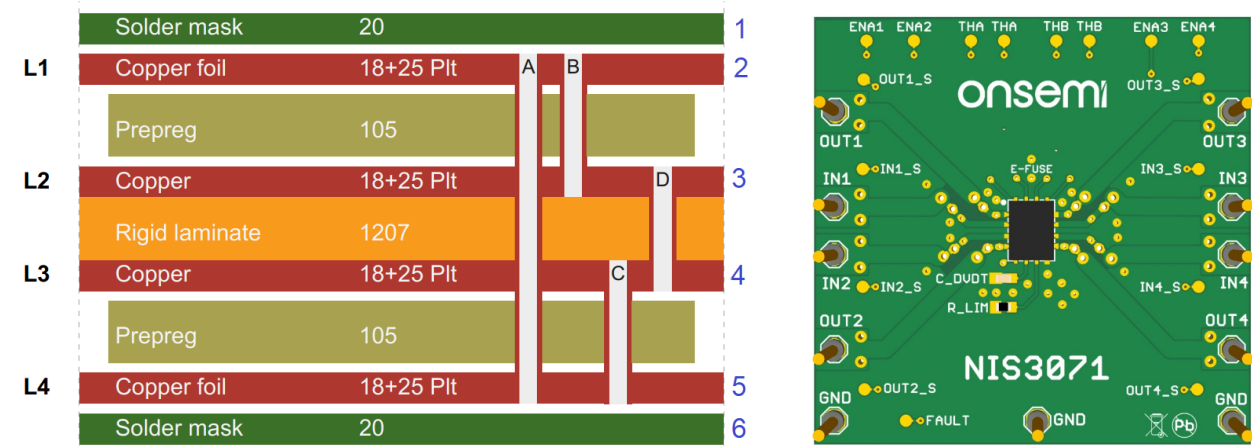
3. Copper L2



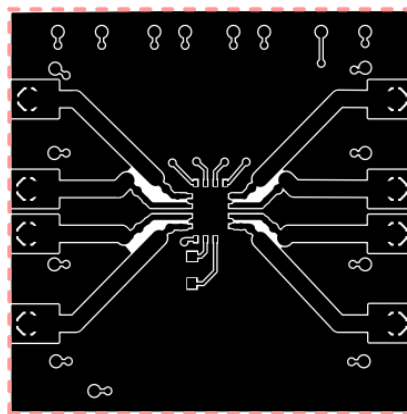
4. Bottom Solder mask

Figure 6. Two Layer PCB Design

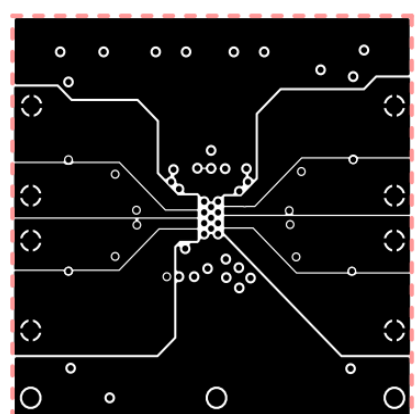
Four Layer PCB Design



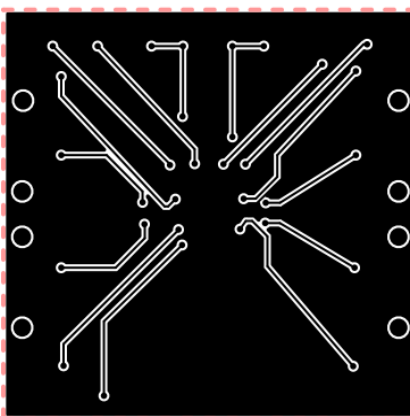
1. Top Solder mask



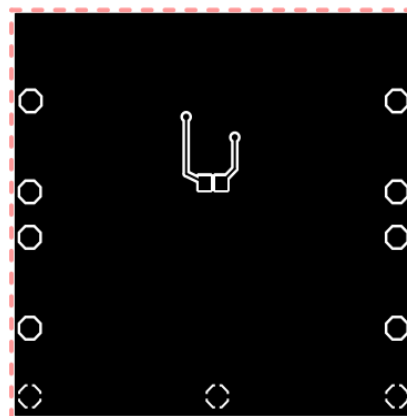
2. Copper L1



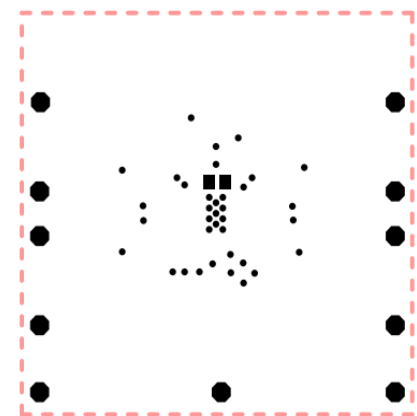
3. Copper L2



4. Copper L3



5. Copper L4



6. Bottom Solder mask

Figure 7. Four Layer PCB Design

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