Enabling Zero Volt Drive Capability for EliteSiC AND90255/D

Abstract

Silicon carbide (SiC) devices have become popular for power electronics world applications due to the increasing demand for efficiency driven by mobility electrification and renewable energy. These applications require power semiconductors capable of operating at higher frequencies with minimized losses. Compared to Silicon−based technologies such as IGBT or Super−Junction, SiC MOSFET offers remarkable advantages such as lower specific drain−source on resistance ($R_{DS(on)}$) per area, higher breakdown voltages, reduced switching losses, optimized reverse recovery body diodes, and lower gate charges. The relationship between the threshold voltage (V_{th}) and specific $R_{DS(on)}$ per area (Rsp) is particularly significant for planar MOSFET structures: this relationship imposes practical limitations on achieving the desired high value of V_{th} to ensure competitive $R_{DS(on)}$. The relatively low V_{th} is often seen as a potential risk for parasitic gate turn−on and subsequent punch−through damage, especially considering the extremely low capacitances achieved through the latest SiC MOSFET planar technology. To address this risk, SiC planar manufacturers often recommend utilizing negative turn off driving techniques. This application note examines the implications of driving **onsemi** SiC MOSFETs with a unipolar gate voltage (0 V/+18 V). The study investigates the relationship between device parameters such as capacitances and threshold voltage and the occurrence of parasitic turn on through simulations and experimental test setups. The objective is to address system concerns and establish safe operating conditions for this type of operation.

Introduction

SiC devices have many benefits over their silicon counterparts, namely lower $R_{DS(on)}$, device capacitances, and reverse recovery charge. Lower device capacitances give rise to higher dV/dt values. However, high dV/dt can cause unwanted turn on of SiC MOSFET devices within bridge topologies [1]−[6], such as the half bridge leg shown in Figure 1. When one device turns on, the dV/dt imposed on the complimentary device causes the Miller capacitance to discharge into the gate which may cause a false turn on if the induced voltage on the gate is higher than the threshold voltage of the MOSFET. The severity of the parasitic turn on depends mainly on Miller capacitance C_{gd}, C_{gs}/C_{gd} ratio, drain voltage slew rate dV_{ds}/dt and total gate resistance as shown in equation 1.

$$V_{gs} = R_g C_{gd} \frac{dV_{ds}}{dt} \left(1 - e^{\frac{-t}{R_g(C_{gd}+C_{gs})}}\right) \quad \text{(eq. 1)}$$

Where R_g is the total gate loop resistance, capacitance C_{gd} and C_{gs} are the device internal capacitances, and dV_{ds} /dt is the slew rate of the drain−to−source voltage.

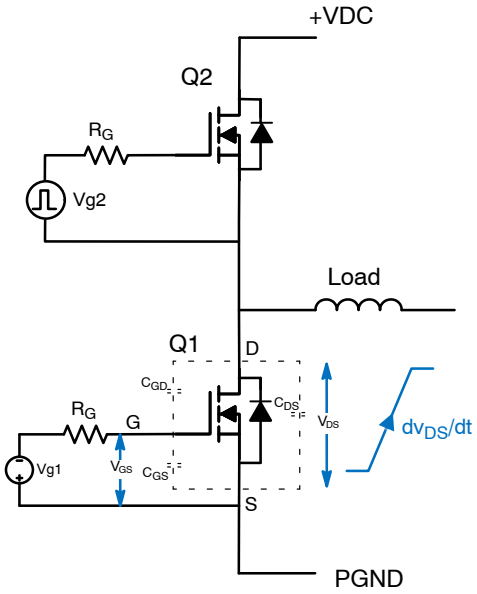

Figure 1. Half−Bridge Configuration

Basically, the high transition rate (dV_{ds}/dt) of drain to source voltage induces a current in the device capacitance C_{gd} which elevates the gate to source voltage (V_{gs}) of the device. As can be seen from equation 2, i_{Cgd} current depends on C_{gd} value and dV/dt value. Since C_{gd} is a device parameter (which cannot be reduced externally), dV/dt is the only variable in this equation can be controlled.

$$i_{C_{gd}} = C_{gd} \frac{dV_{C_{gd}}}{dt} \quad \text{(eq. 2)}$$

Parasitic turn on can be also caused by large parasitic printed circuit board (PCB) inductances of the gate loop and the main power loop which may cause significant oscillation in the device's gate to source voltage and drain−to source voltage (V_{ds}). Figure 2 shows the equivalent circuit of the MOSFET for switching behavior analysis. V_{driver} represents the gate driver, R_{g_ext} is the external gate resistor, R_{g_int} is the internal gate resistor of the device, C_{gd}, C_{gs} and C_{ds} are the device parasitic capacitances and L_S is the total

source parasitic inductance of the device and the PCB. Supply voltage of the gate driver and R_{g_ext} are the main parameters that can be tuned to overcome parasitic turn on issues.

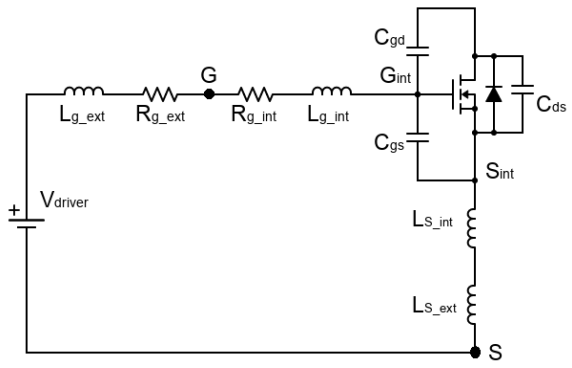

Figure 2. MOSFET Switching Equivalent Circuit

On the other hand, internal source inductance (L_{S_int}) and external source inductance (L_{S_ext}) can also affect the gate source voltage behavior, especially in 3−pin devices. 3−pin devices share the source pin for the main drain current and the gate driver current [3], [4]. Since the source pin of the device might be exposed to high di/dt values, an induced voltage can be observed on the source pin and gate−source voltage. Equation 3 gives the formula for the induced voltage caused by di/dt.

$$V_{L_S} = L_S \times \frac{di_{L_S}}{dt} \quad \text{(eq. 3)}$$

As can be seen from equation 3, di/dt and source inductance affect the induced voltage. Thus, the lower L_S ($L_{S\_int} + L_{S\_ext}$), the lower V_{LS}. Note that when drain current is decreasing (as during turn off), V_{LS} has a negative polarity which increases the net gate−source voltage applied by V_{driver}, tending to keep the device on. L_S consists of two stray inductances: L_{S_int} and L_{S_ext}. The use of a device package with a Kelvin source connection helps to deliver a more stable source signal of the device (Kelvin source) to the gate of the SiC MOSFET since it provides separated path for gate current and there is no voltage drop caused by rapid changes in drain current [5].

Application (The Half Bridge Topology Simulation)

In this section simulation results produced using Simetrix [6], are given for the half bridge circuit with constant duty cycle around 50%. The V_{gs}, V_{ds}, V_{gs_int}, channel current, and body diode current of both the high side and the low side MOSFETs are measured. Where,

- *Vgs* is gate to source voltage of MOSFET measured from the pins of the device
- *Vds* is drain to source voltage of MOSFET measured from the pins of the device
- *Vgs_int* is internal gate to source voltage of MOSFET measured from the dies of the device
- *Channel current* is the current of the device that flows through device's channel, and it is measured from the die of the device
- *Body diode current* is the die current that flows through body diode of the device
- *High Side MOSFET* is the MOSFET that its source pin is connected to drain of other MOSFET
- *Low Side MOSFET* is the MOSFET that its source pin is connected to ground.

Simulated waveforms are taken from Simetrix for various gate resistor values. The test conditions for the half bridge topology are set as follows:

- Vin = 800 V
- Rg = 4.7 Ω − 25 Ω
- Vgs_on = +18 V
- Vgs_off = 0 V, −3 V
- Load current = 20 A − 40 A
- Duty Cycle = 48.7%
- Frequency = 100 kHz

Figure 3 shows the Simetrix schematic representation of circuit with 4.7 Ω on and off gate resistors. The NVBG040N120M3S from **onsemi**'s EliteSiC M3S portfolio is used as switching device for simulations. NVBG040N120M3S is 1200 V device with 40 mΩ $R_{DS(on)}$ value [7].

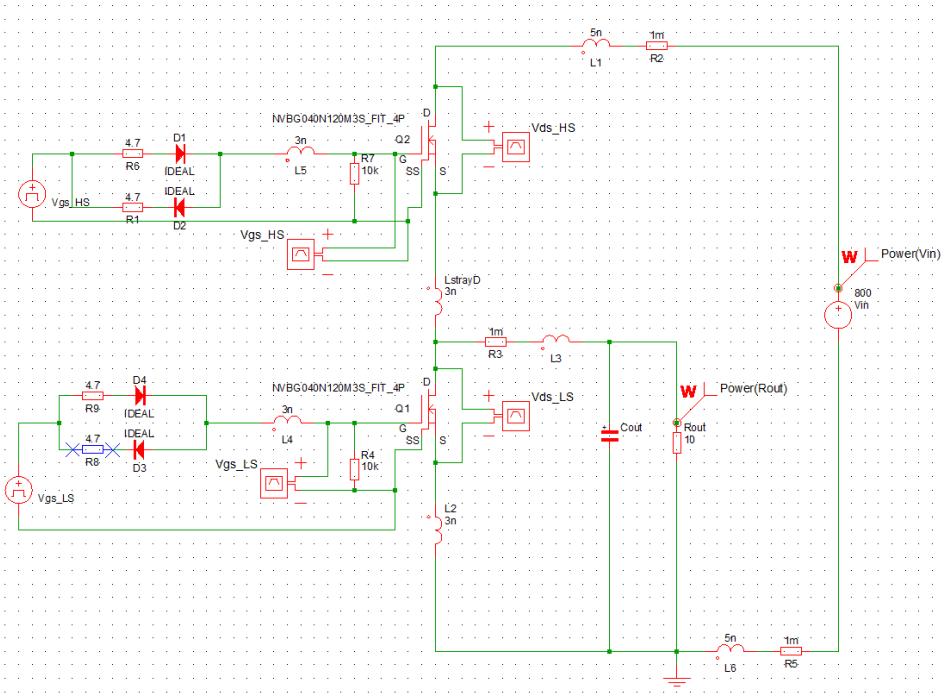

Figure 3. Simetrix Schematic of the Half Bridge Converter

During drain to source voltage V_{ds} transitions, there is a possibility of parasitic turn on of the switching device due to high dV_{ds}/dt. Figure 4 illustrates the impact of parasitic turn on of the low side MOSFET when it should remain off. This simulation result was obtained using 4.7 Ω on and off gate resistors as in the schematic shown in Figure 3.

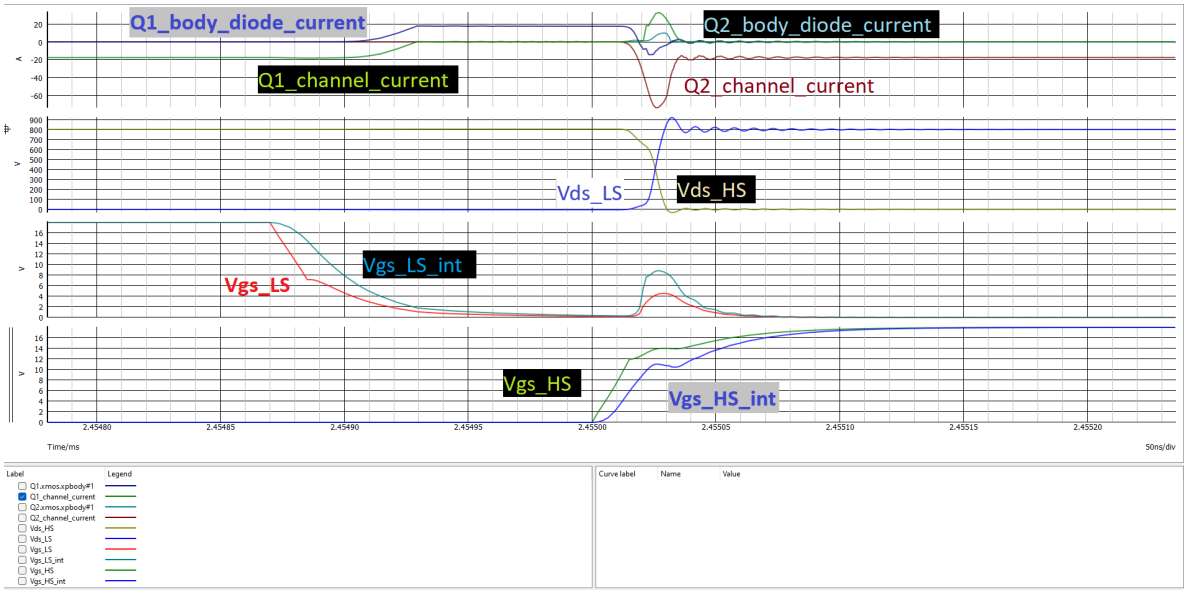

Figure 4. Parasitic Turn−On Issue of Low Side MOSFET on the Half−Bridge Converter

It can be seen from Figure 4 that V_{gs} of the low side MOSFET increases when V_{ds} of low side switching device starts ramping up. This is because the fast rate dV_{ds}/dt induces a current through C_{gd} according to equation 2. The flowing current passes through both C_{gd} and C_{gs}, creating a voltage divider effect between C_{gd} and C_{gs}, and causes gate voltage rise. Therefore, it's essential to take into account the C_{gs}/C_{gd} ratio for parasitic turn on (PTO) considerations in addition to dV_{ds}/dt, R_{g_int} and R_{g_ext}. This unwanted increase of V_{gs_LS} due to i_{Cgd} current opens the channel of low side MOSFET to conduct current as seen from Figure 4. It needs to be pointed out that the V_{gs_int} value of the low side MOSFET is higher than V_{gs} during the time V_{ds} is changing. This phenomenon can be explained as follows: The current

i_{Cgd} leads to V_{gs} voltage increase and this increased V_{gs} discharges through internal and external gate resistors so that the external V_{gs} is lower than V_{gs_int} during PTO.

On the other hand, when low side MOSFET is turning on and high side MOSFET is turning off, there is no such parasitic turn on issue because the gate will be pulled down to negative value due to negative dV_{ds}/dt (Figure 5). It is important to ensure that this negative voltage does not exceed the recommended maximum voltage rating provided by the manufacturer, which is −8 V for the present example. Exceeding this limit can result in increased stress on the oxide electric field, ultimately leading to a shortened lifespan of the device [8], [9].

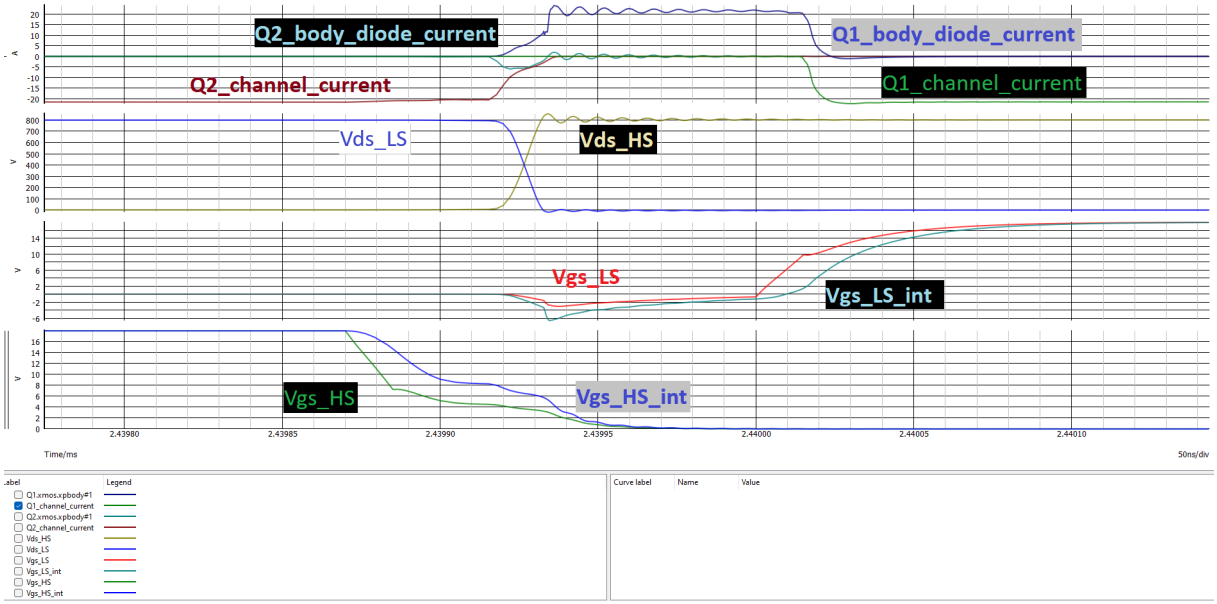

Figure 5. High Side MOSFET Turning Off Transition of the Half−Bridge Converter

Additionally, second illustration is also provided with 25 Ω gate resistor. The purpose of the larger R_{g_ext} is to achieve a lower dV_{ds}/dt which, according to equation 1, results in lower i_{Cgd}. It is expected that the difference between V_{gs_int} and V_{gs} with 25 Ω gate resistor compared to 4.7 Ω gate resistor will be lower due to lower i_{Cgd}. Figure 6 and Figure 7 show the results for this condition for both switch transitions.

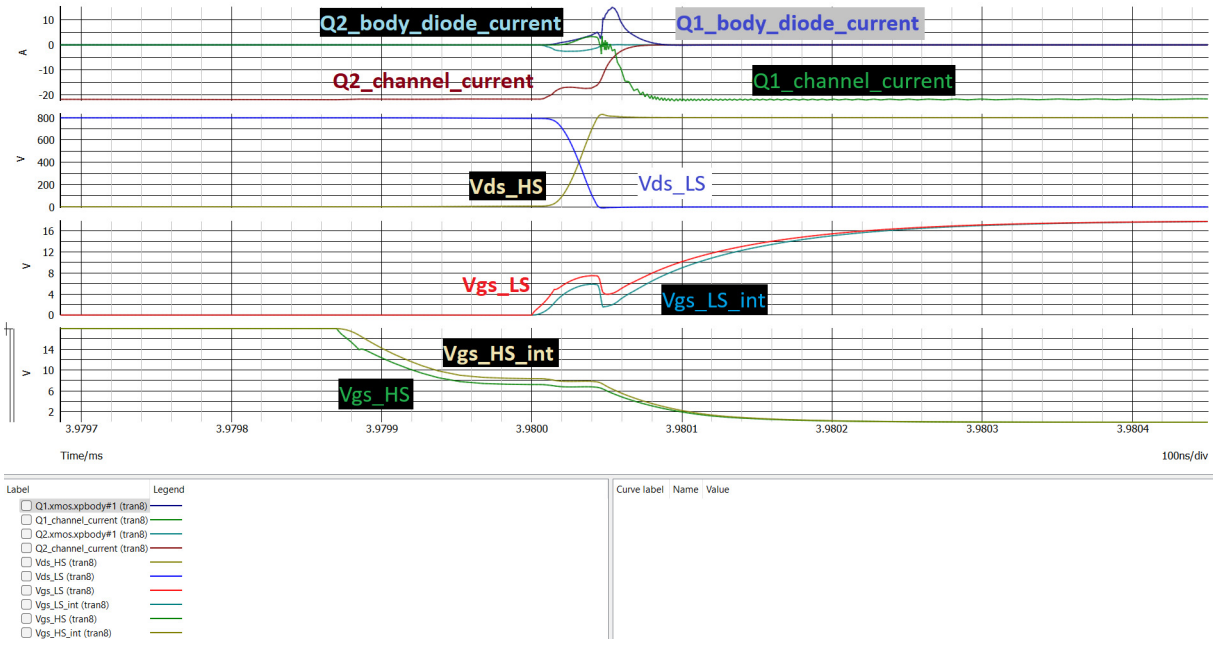

Figure 6. Turning On of Low Side with 25 Ω Gate Resistor for the Half−Bridge Converter

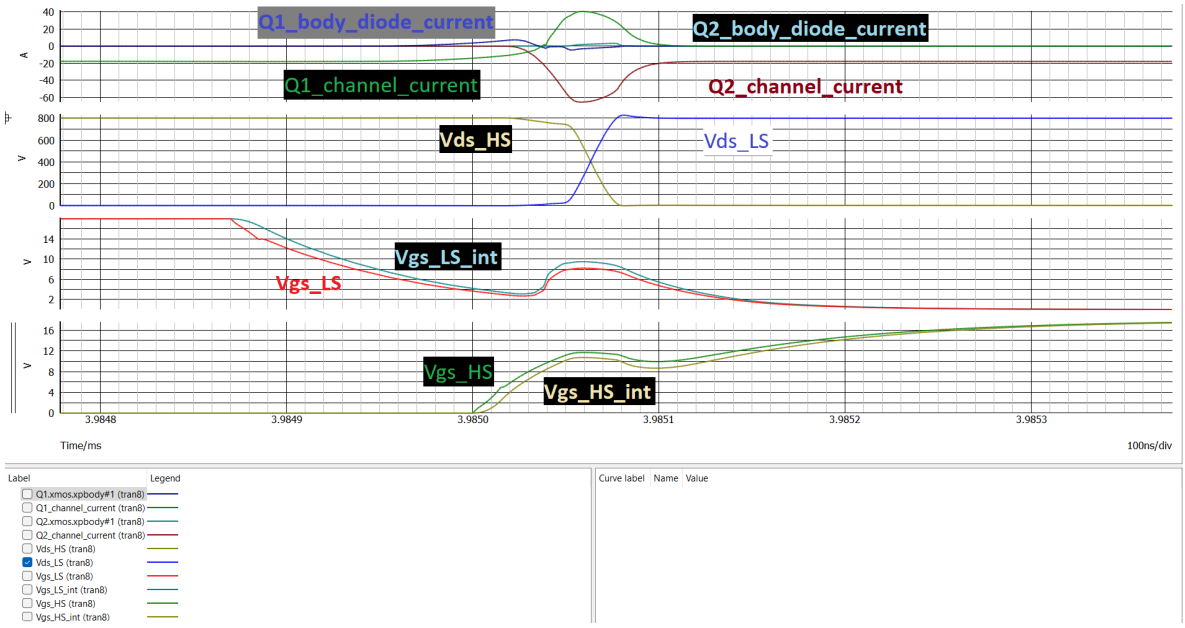

Figure 7. Turning On of High Side with 25 Ω Gate Resistor for the Half−Bridge Converter

According to the simulation results presented in Figure 4 and Figure 7, parasitic turn on happens with the 4.7 Ω and 25 Ω gate resistors cases but 25 Ω gate circuit has less channel current and less V_{gs_int} of LS device peak voltage due to lower dV_{ds}/dt. It can be concluded that by choosing a suitably high gate resistor value parasitic turn on can be eliminated. However, since dV_{ds}/dt will be lower with higher gate resistor value, switching losses will be higher as a penalty. Reverse recovery current of the body diode of a related MOSFET leads to higher dV_{ds}/dt so reverse recovery current is another parameter that affects dV_{ds}/dt value of the switching device in addition to gate resistor value [10]. Thus, it needs to be pointed out that reverse recovery charge of body diode plays a crucial role on parasitic turn on phenomenon in addition to its importance for switching loss.

Table 1 is prepared by using two different gate resistors (4.7 Ω and 10 Ω) and two different turn off driving voltage (0 V and −3 V) with different arrangements to show the effect of gate resistor and turn off driving voltage on efficiency of the system, dV_{ds}/dt and presence of parasitic turn on for the half bridge converter.

Based on the results shown in Figure 5, it is observed that in the case of soft switching, specifically zero voltage switching, there is an absence of parasitic turn on phenomenon. Soft switching occurs when the high side MOSFET turns off and the low side one turns on in the case of a half bridge converter that is shown in Figure 3. In this transition period, there is a flow of current through the body diode during the dead time and related SiC MOSFET turns on with body diode voltage drop, that is almost zero, on it.

Table 1. EFFECT OF GATE RESISTOR VALUE ON EFFICIENCY, DVDS/DT AND PARASITIC TURN ON OF THE HALF BRIDGE CONVERTER

Parameters					
Rg_off (Ω)	Rg_on (Ω)	Efficiency (%)	dV_{ds}/dt of Low Side MOSFET's V_{ds} Rising Edge (V/ns)	Parasitic Turn On	Turn Off Driving Voltage (Vgs_off)
4.7	4.7	98.11	74.78	Present	0 V
4.7	4.7	98.3	77.24	Present	−3 V
4.7	10	98.03	60.52	Present	0 V
4.7	10	98.10	60.42	Present*	−3 V

*Peak current value of PTO is smaller compared to 0 V turn off driving case with same Rg values.

Experimental Verification

A simple experiment using double pulse circuit, Figure 8 is used to analyze the crosstalk phenomenon. In the experiment, it is assumed that one device is switching while the other device is held in the off state using V_{gs_off} 0 V or −3 V. For simplicity, to measure the switch current a 50 mΩ current shunt is used in series with the lower device. Therefore, to study the crosstalk effect on the upper device, we considered the lower device is switching on/off and the upper device (DUT) is held off. Since we do not have access to measure the internal channel current of the MOSFET to confirm the event of parasitic turn on, we can observe the

difference in the drain current (I_D) waveform of the switching device and gate voltage (V_{gs}) of the turn off device. The subsequent discussion will be focused on the PTO event since it is more important than the negative spike when unipolar gate bias is used to turn off the device. It should be noted that all tests presented here are done at room temperature. The impact of high temperature has been discussed in [11].

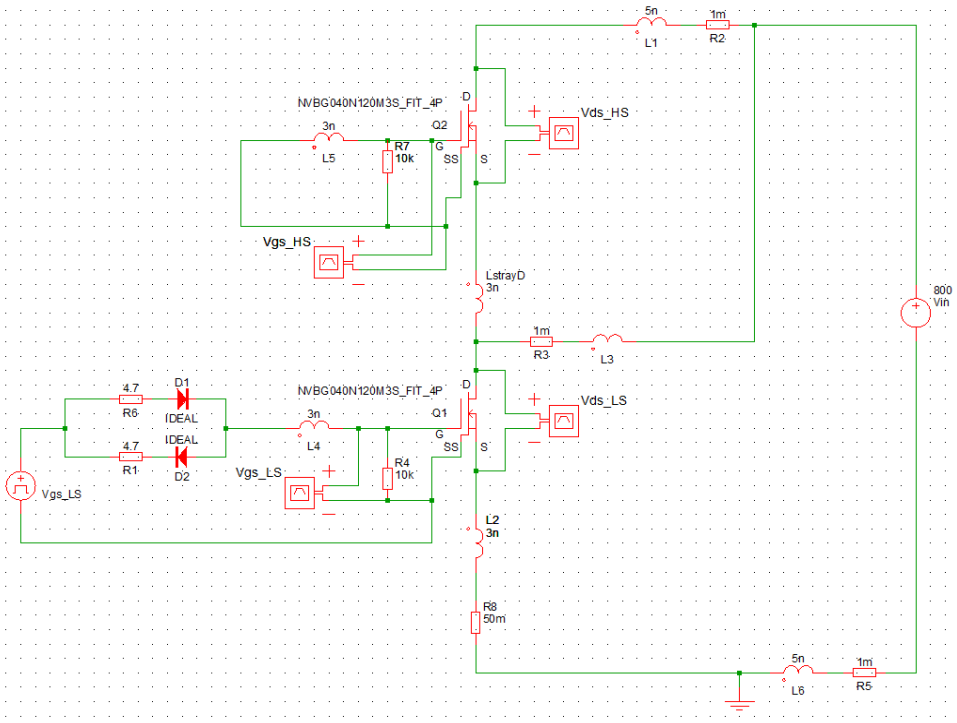

Figure 8. Double Pulse Test Schematic

In the experiment **onsemi** SiC MOSFET NVBG040N120M3S and gate driver NCV57000 are used. NVBG040N120M3S features the latest generation of **onsemi** SiC MOSFET which is designed for fast switching application such as on−board charger (OBC). The gate driver NCV57000 features high current 6 A sink/source current, active clamp and Desat protection. The active clamp function is considered as one of the effective techniques to mitigate the PTO event. In the experiment, the active clamp is also enabled or disabled to check its effectiveness. In all test result, the input bus voltage is V_{DS} = 800 V and the scope setting is a s follows:

- CH1: VGS_LS (6 V/div)
- CH2: VDS_LS (300 V/div)
- CH3: VSD_HS (300 V/div)
- CH4: ID (20 A−40 A/div)
- CH5: VGS_HS (6 V/div). The MATH function is used to calculate the switching energy.

Figure 9−12 shows the result where both devices have $R_{g\_on/off}$ = 4.7/4.7 Ω. Figure 9 shows comparison of the switching waveforms for I_D = 40 A, V_{gs} = 0/18 V (unipolar) versus −3/+18 V (bipolar), and active clamp function enabled. As it can be seen that when V_{gs} = 0/18 V, a positive spike (4.5 V peak) appears on its gate and the drain current waveform has slightly larger Q_{rr} which indicates that there is possible parasitic turn on. It is more obvious at lower current due to larger Q_{rr} as shown in Figure 10 for I_D = 10 A. It should be noted that the gate voltage measured externally is lower than the internal gate voltage the die sees due to voltage drop in the device internal parasitic resistance, Figure 2. Therefore, the actual gate voltage spike is greater than 4.5 V which is higher than the threshold voltage (V_{th}) of the device (2.9 V typical).

When the active clamp is disabled even larger Q_{rr} can be observed in Figure 11 when V_{gs} = 0/+18 V. The voltage spike on the gate reaches to 7.76 V which high enough to turn on the high side device. In this case turn on loss (Eon) is increased from 460 μJ to 500 μJ. If the turn off resistor of the high side device is increased R_{g_off} = 10 Ω larger Q_{rr} and Eon = 560 μJ can be observed as depicted in Figure 12. The larger the gate resistor, the larger the losses and vice versa.

In general, for a fixed gate resistor, switching losses increased with unipolar gate voltage (0/18 V) compared to bipolar (−3/18 V) mainly due to an increase in turn off loss (Eoff) as shown in Figure 13. This is expected as turning off the device with 0 V means slower switching speed, but this can be rectified by decreasing the turn off gate resistor to switch the device faster. However, switching faster at turn off will increase the negative spike on V_{gs}.

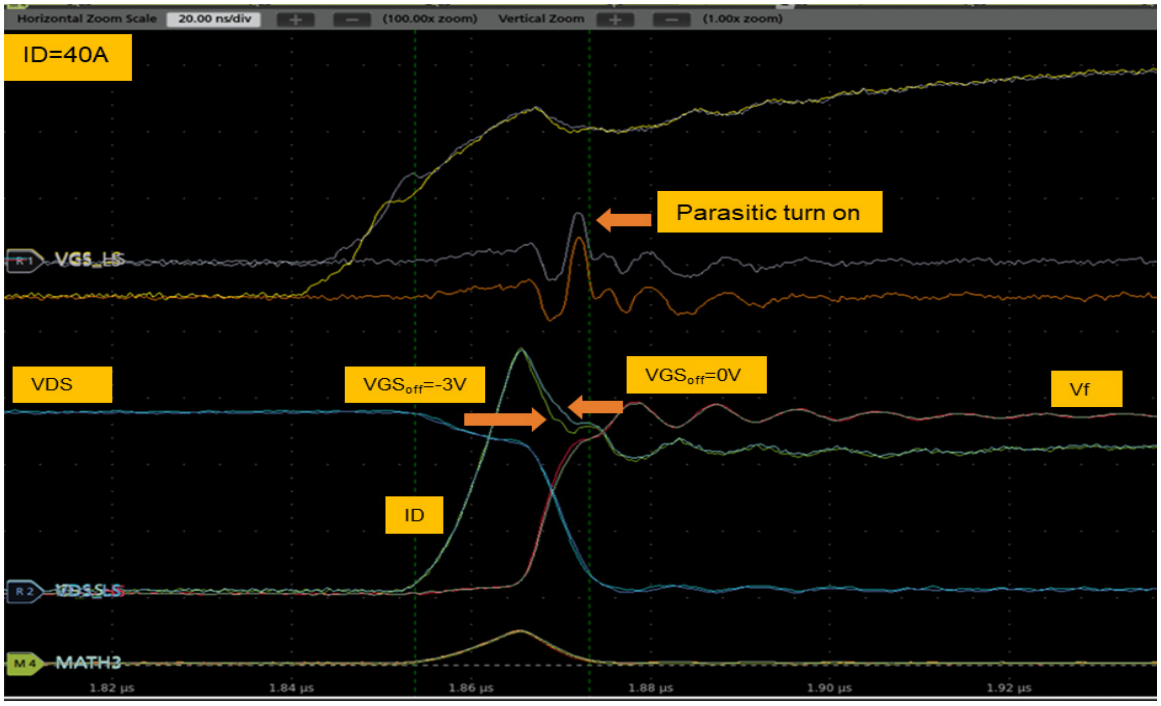

Figure 9. Switching Waveforms V_{gs_off} = 0 V vs. −3 V, I_D = 40 A (20 A/div), $R_{g\_on/off}$ = 4.7/4.7 Ω (Both Devices). Active Clamp Function Enabled

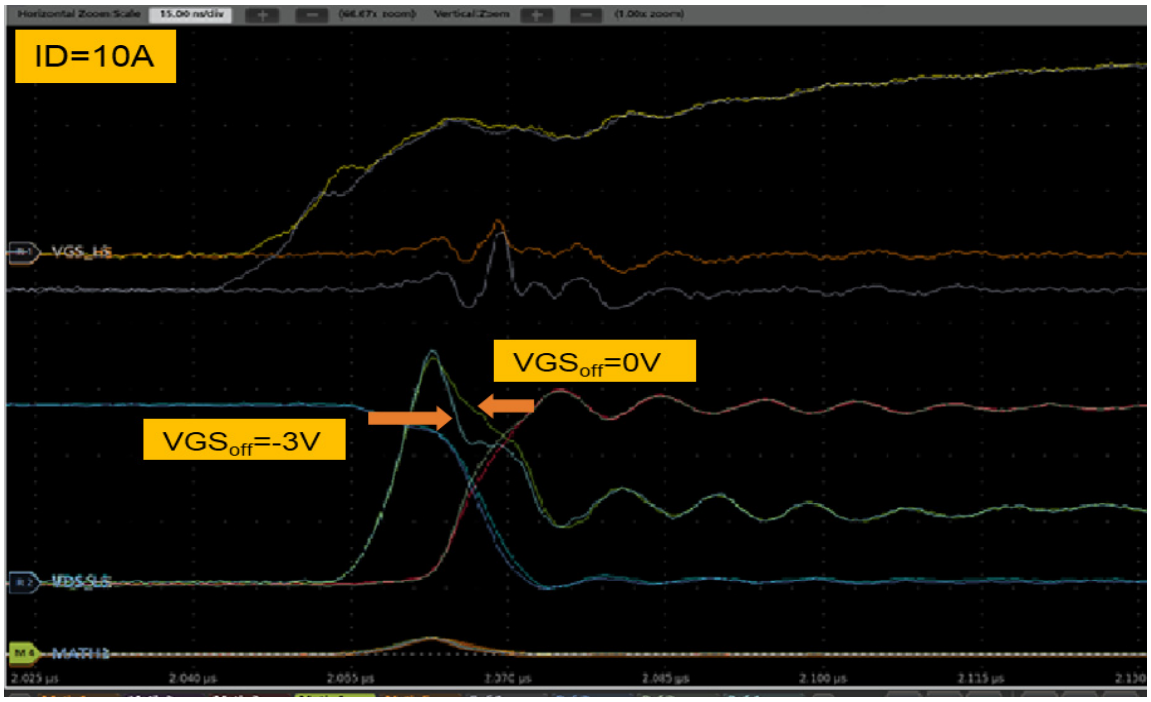

Figure 10. Switching Waveforms V_{gs_off} = 0 V vs. −3 V, I_D = 10 A (10 A/div), $R_{g\_on/off}$ = 4.7/4.7 Ω (Both Devices). Active Clamp Function Enabled

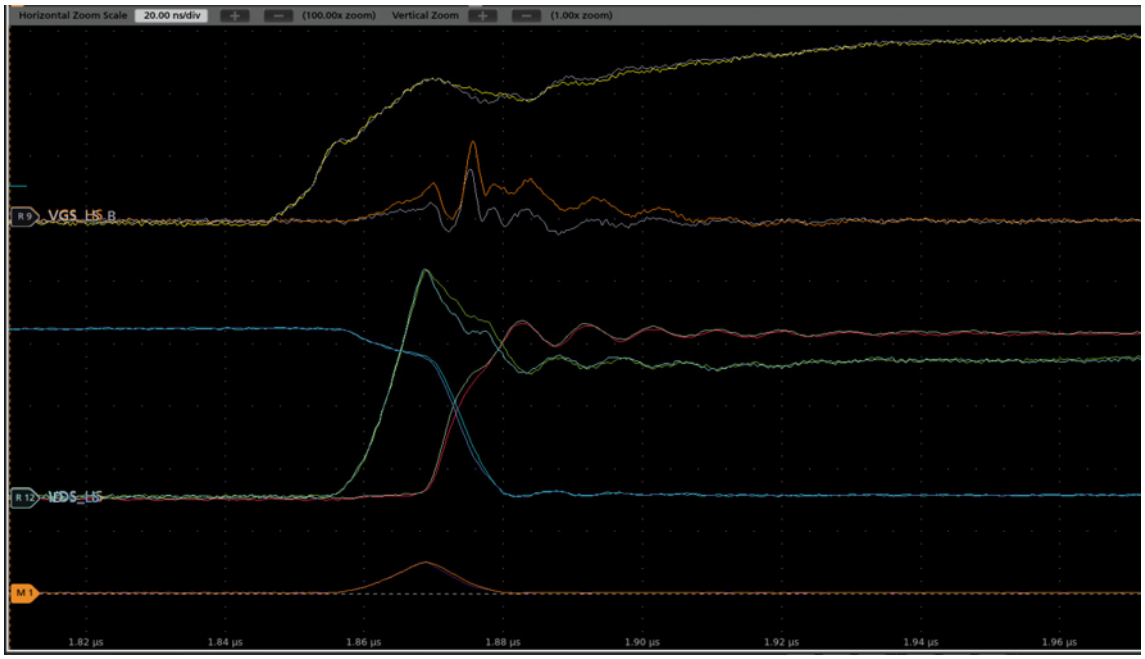

Figure 11. Switching Waveforms V_{gs_off} = 0 V, I_D = 40 A, $R_{g\_on/off}$ = 4.7/4.7 Ω (Both Devices), with and without Active Clamp

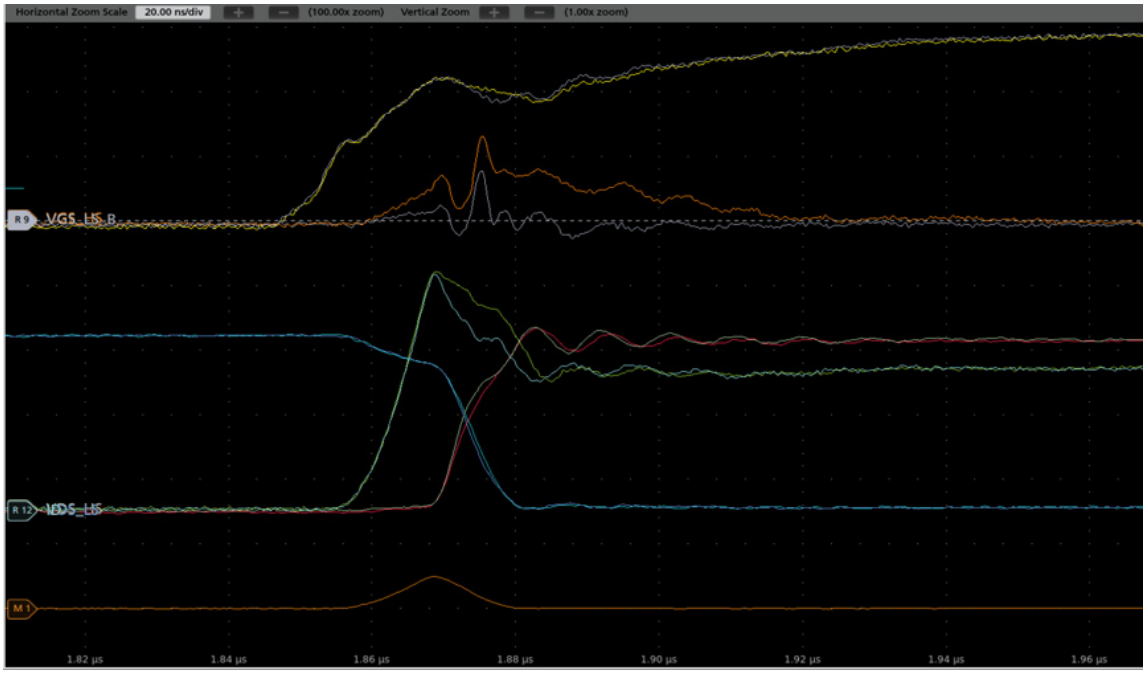

Figure 12. Switching Waveforms V_{gs_off} = 0 V, I_D = 40 A, $R_{g\_on/off}$ = 4.7/4.7 Ω (LS) and 10 Ω (HS), with and without Active Clamp

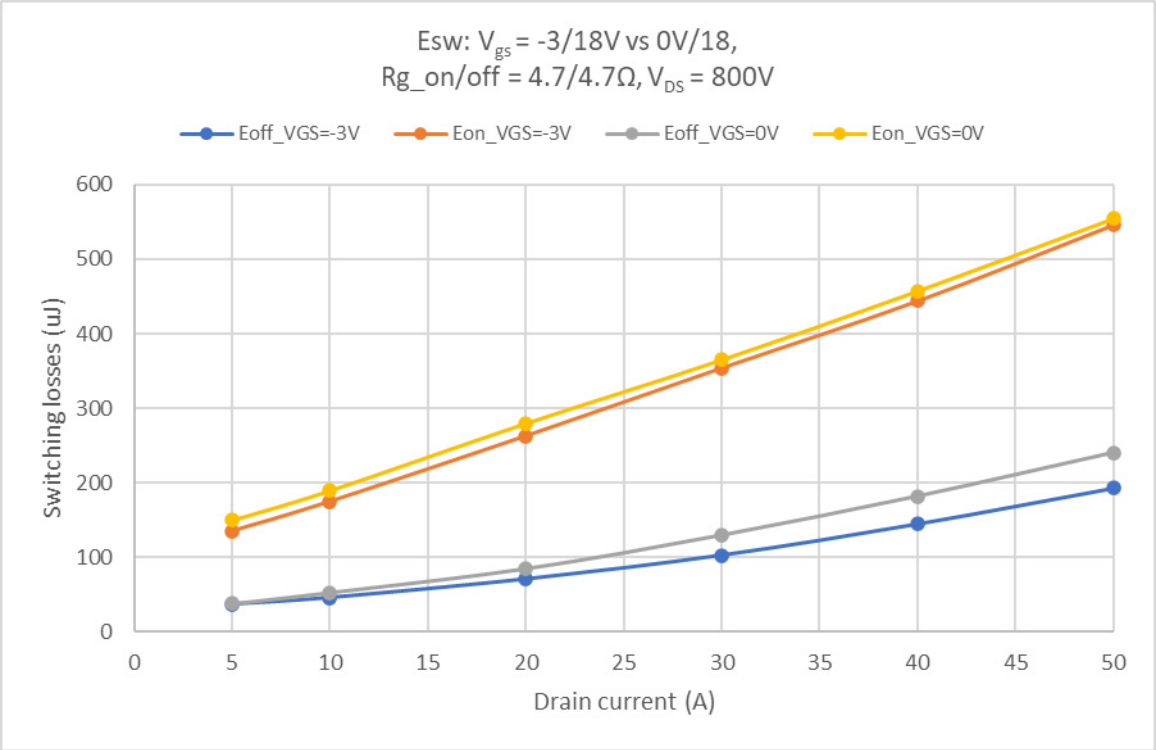

Figure 13. Switching Losses Comparison V_{gs_off} = 0 V vs. −3 V, with $R_{g\_on/off}$ = 4.7/4.7 Ω. With and without Active Clamp

To mitigate the parasitic turn on, along with active clamp function, the turn on gate resistor can be tuned to reduce the dV_{ds}/dt. This concept is demonstrated in Figure 14−17 which is performed with active clamp enabled. With active clamp function enabled the turn off gate resistor can be reduced just enough to avoid larger negative stress on the gate voltage which might affects the gate reliability and Electromagnetic Interference (EMI) compliance. As it can be seen for $R_{g\_on/off}$ = 10/4.7 or $R_{g\_on/off}$ = 10/2.35 all switching waveforms almost aligned even for low current and there is minimum loss increment when V_{gs} = 0/18 V is used compared to −3/18 V. Table 2 compares the switching speed of the device with V_{gs_off} 0 V versus −3 V. It can be noted that for R_g = 4.7 Ω, there is 10 μJ increase in Eon while Eoff increased by 37 μJ. The dV_{ds}/dt is slightly lower when V_{gs_off} = 0 V. When R_{g_on} increases to 10 Ω, Eon increased by 166 μJ and dV_{ds}/dt drops to approximately 85 V/ns and no severe parasitic turn on is observed.

Table 2. SWITCHING PARAMETERS FOR I_D = 40 A

I_D (A)	Rg_on (Ω)	Rg_off (Ω)	Vgs_off (V)	dv/dt Rising (V/ns)	dv/dt Falling (V/ns)	di/dt (A/ns)	Eon (μJ)	Eoff (μJ)
40	4.7	4.7	−3	129	103	7.137	444	146
40	4.7	4.7	0	120	95.74	7.133	456	182
40	10	4.7	−3	89.29	45.82	4.745	611	146
40	10	4.7	0	50	46	4.6	622	182

Without active clamp the turn on resistor must be larger than that with active clamp and vice versa for the turn off resistor which can be set to zero to avoid the PTO, but this will generate larger negative spike. Figure 17 show the result without active clamp. As it can be seen in Figure 17, if turn off gate resistor R_{g_off} = 4.7 Ω, the turn on resistor has to increase R_{g_on} = 20 Ω to avoid the PTO. However, with higher R_{g_on} the switching losses will increase. Lower R_{g_on} value can be selected if we reduce R_{g_off} just enough to avoid PTO and reduce switching losses.

Finally, Figure 18 shows the switching losses with V_{gs} = 0/18 V, R_{g_off} = 2.35 Ω and R_{g_on} = 4.7 Ω versus 10 Ω. In the range of 5−40 A, there is 10% average increase in Eon (Eon is 10% higher with 10 Ω compared to R_{g_on} = 4.7 Ω case). In typical OBC application (7.2 kW − 22 kW), the current range is typically between

10−30 A. So, a 10% increase in Eon loss can be considered acceptable. R_{g_off} can be reduced when V_{gs_off} = 0 V in order to boost the efficiency of the converter but this may cause higher common mode noise and as result failing to comply with EMI standard. Therefore, a tradeoff has to be made between efficiency and EMI.

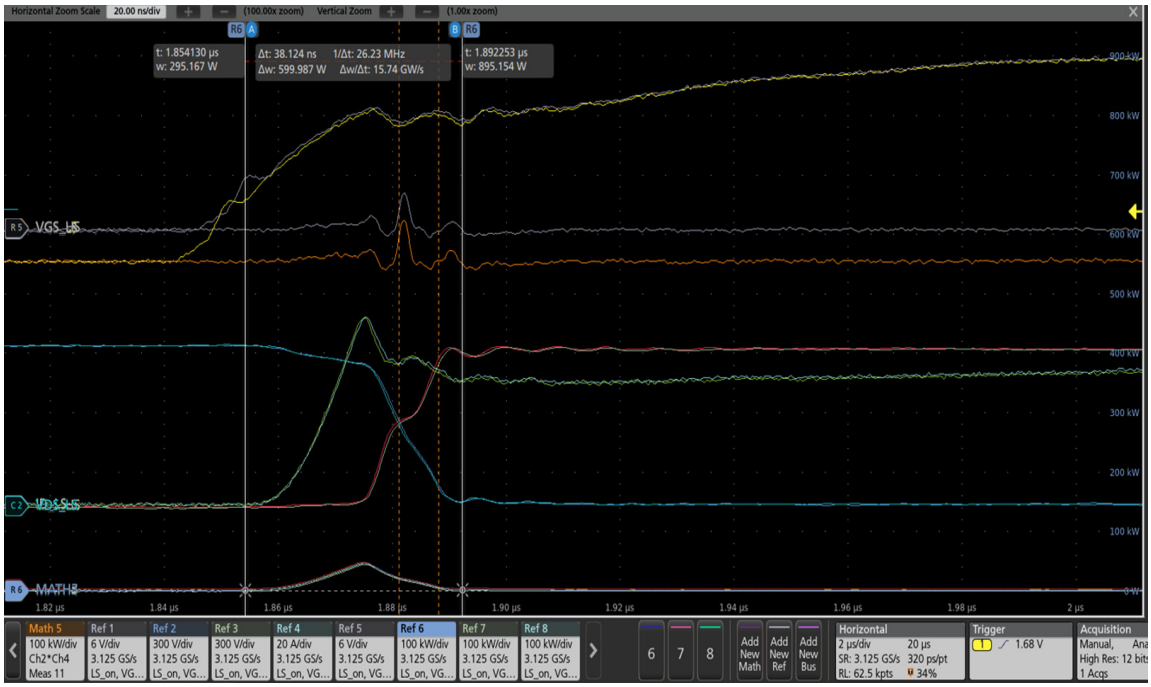

Figure 14. Switching Waveforms Comparison V_{gs_off} = 0 V vs. −3 V, I_D = 40 A, $R_{g\_on/off}$ = 4.7/4.7 Ω, V_{ds} = 800 V

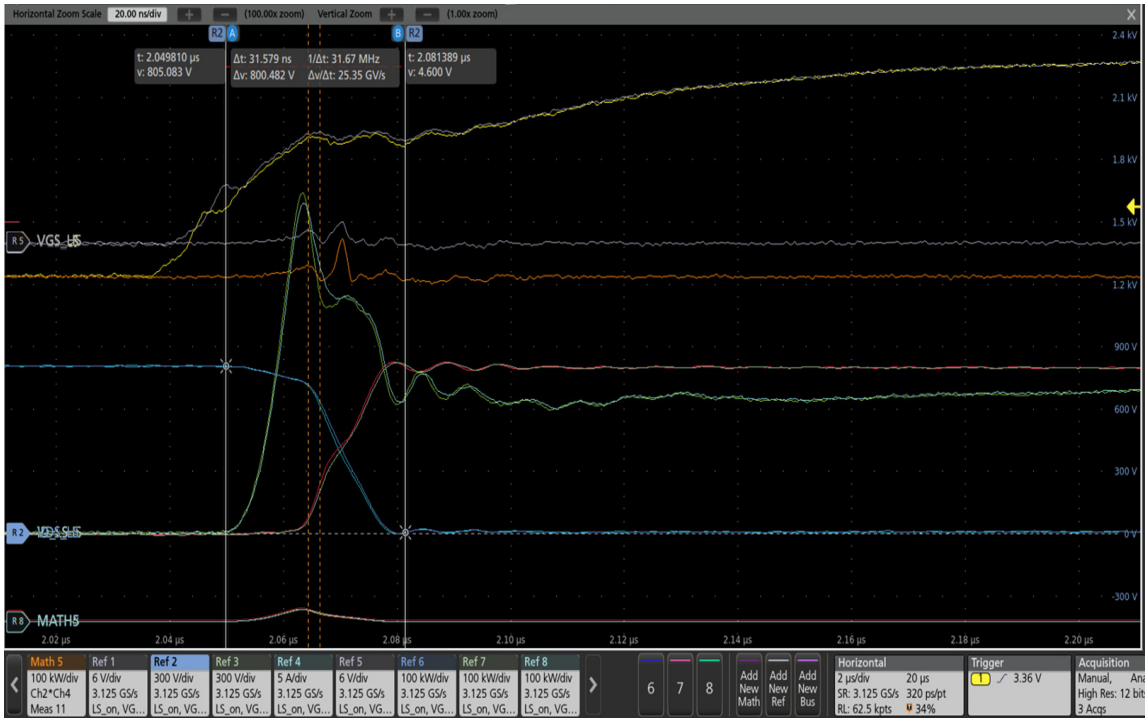

Figure 15. Switching Waveforms Comparison V_{gs_off} = 0 V vs. −3 V, I_D = 10 A, $R_{g\_on/off}$ = 4.7/4.7 Ω, V_{ds} = 800 V

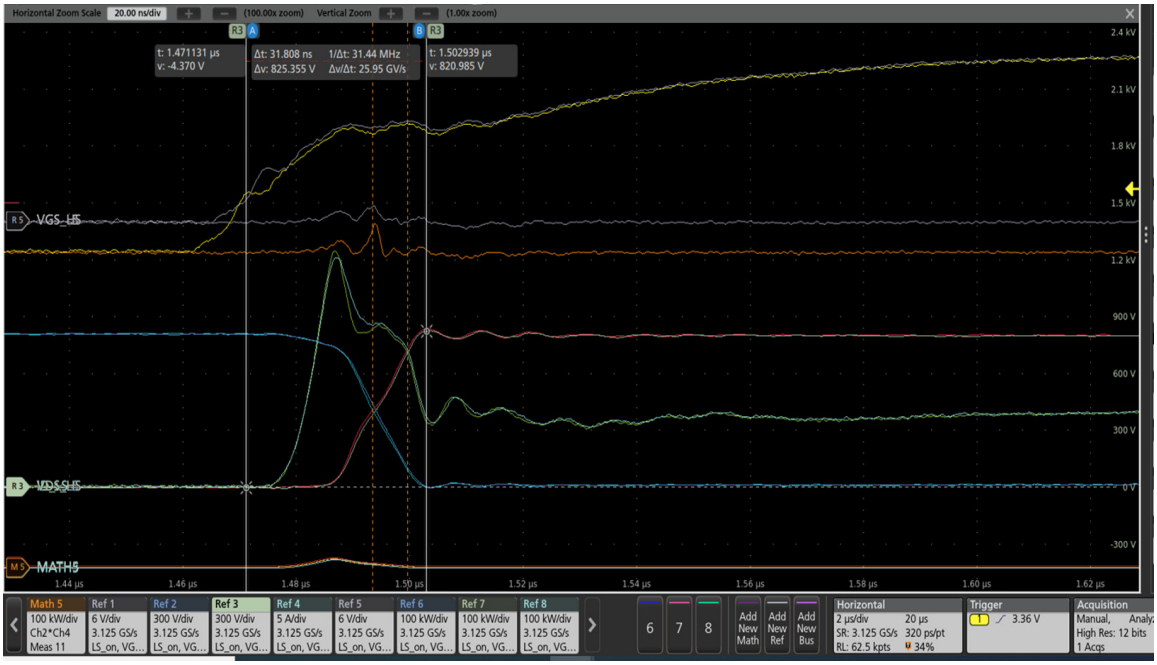

Figure 16. Switching Waveforms Comparison V_{gs_off} = 0 V vs. −3 V, I_D = 40 A, $R_{g\_on/off}$ = 10/4.7 Ω, V_{ds} = 800 V

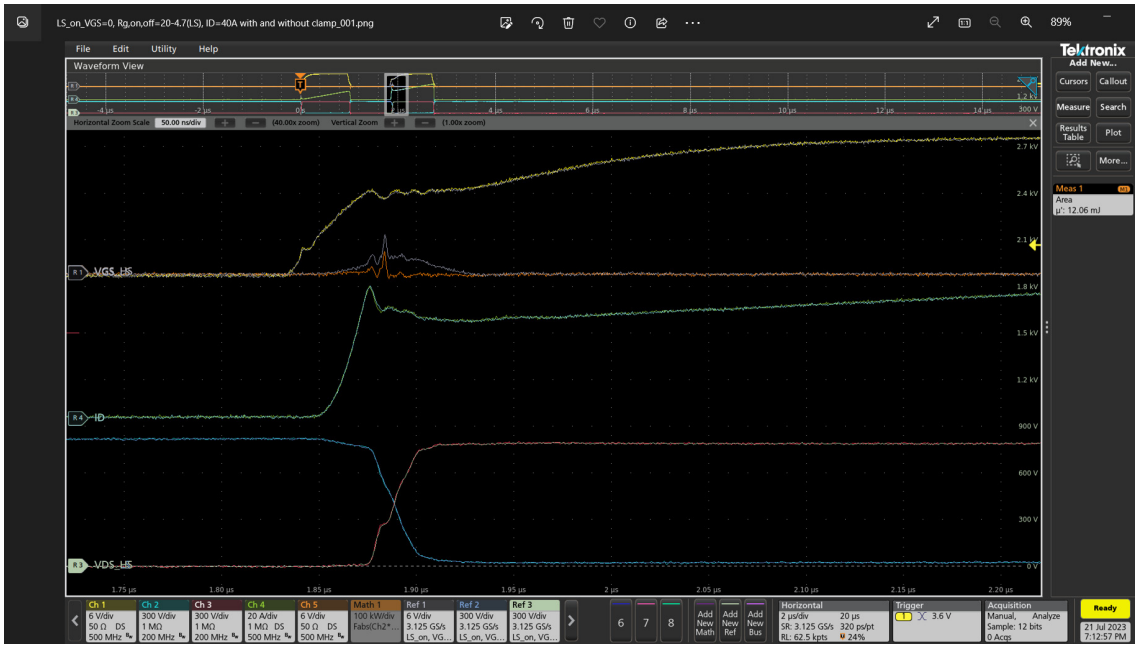

Figure 17. Without Active Clamp, V_{gs_off} = 0 V, R_{g_on} of Low Side Increased to 20 and R_{g_off} = 4.7/4.7 Ω to Reduce dv/dt and Prevent PTO

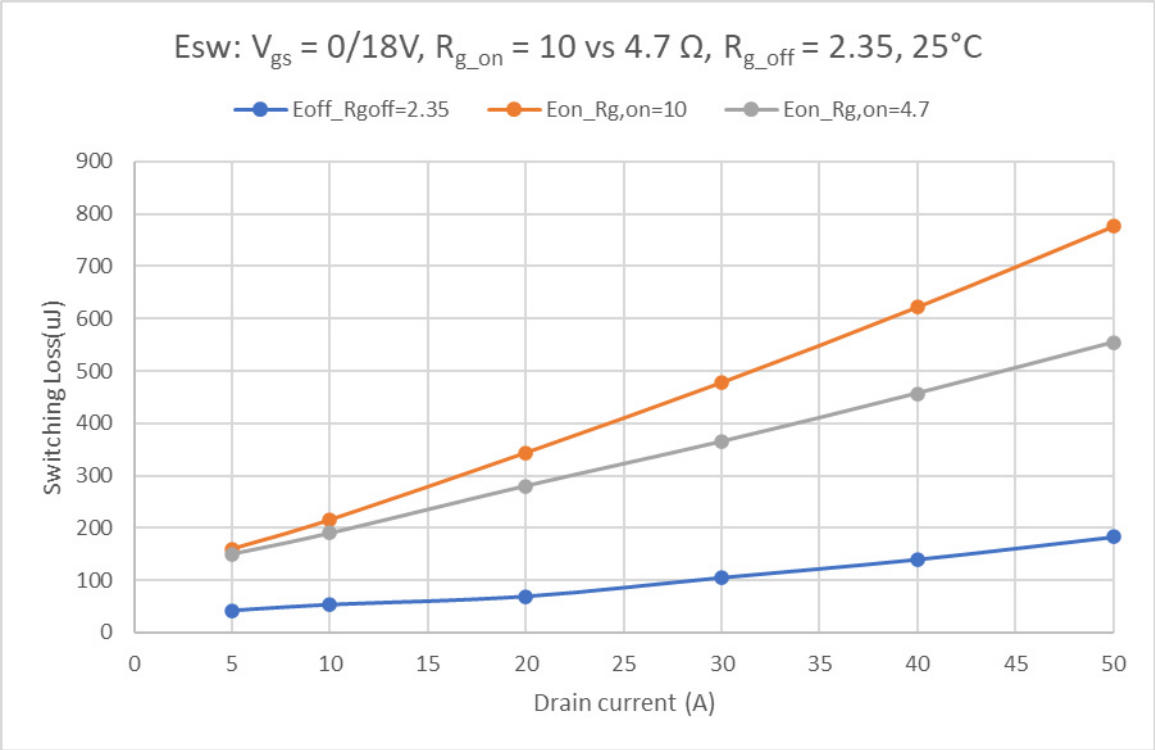

Figure 18. Switching Losses Comparison V_{gs} = 0 V/18 V, with R_{g_on} = 4.7 Ω vs. 10 Ω. With Active Clamp Enabled

Conclusion

This paper discusses mainly the ability to drive **onsemi**'s SiC MOSFETs with unipolar gate to source voltage (0 V/+18 V) and its impact on system efficiency. Due to the fast switching speed and low threshold voltage of SiC MOSFET a crosstalk between power devices in a half bridge configuration becomes a concern especially when it turns off with Vgs_off = 0 V. When one device turns on, the dV_{ds}/dt imposed on the complimentary device causes Miller capacitance to discharge into the gate which may cause a parasitic turn on if the induced voltage on the gate is high enough. The severity of the crosstalk depends mainly on Miller capacitance C_{gd}, switching rate dV_{ds}/dt, C_{gs}/C_{gd} ratio and total gate resistance (R_{g_ext} + R_{g_int}). In this paper the issue of parasitic turn on and its impact on switching losses are studied using simulation and hardware test setups. To prevent the parasitic turn on, the turn on gate resistor must be increased to reduce the dV_{ds}/dt and Miller capacitance effect or V_{gs_off} must have a sufficiently high value. For example, based on the test results, R_{g_on} = 10 Ω is good compromise between switching losses and potential for PTO. When V_{gs_off} = 0 V is used, it is also recommended to reduce R_{g_off} to enable discharge of V_{gs} during times when PTO may occur.

Active Miller clamp helps to mitigate the PTO effect on switching losses, but tuning the $R_{g\_on/off}$ to control the dV_{ds}/dt is also necessary to prevent the PTO completely for the case of V_{gs_off} = 0 V. If no active clamp is used, R_{g_off} must be minimum to reduce the need to increase R_{g_on} to mitigate PTO while keeping low switching losses. R_{g_off} = 0 Ω is equivalent to an active clamp function.

Ultimately, from practical perspective, it is feasible to drive **onsemi**'s SiC MOSFETs with V_{gs_off} = 0 V even when experiencing dV_{ds}/dt = 50 V/ns. However, assuming proper PCB design, the designer must consider the tradeoffs between the target efficiency, reliability and EMI compliance. A gate driver with active clamp is highly recommended when unipolar gate voltage is used. Finally, driving the SiC MOSFET with sufficient negative turn off voltage is recommended to eliminate PTO and reach higher system efficiency.

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